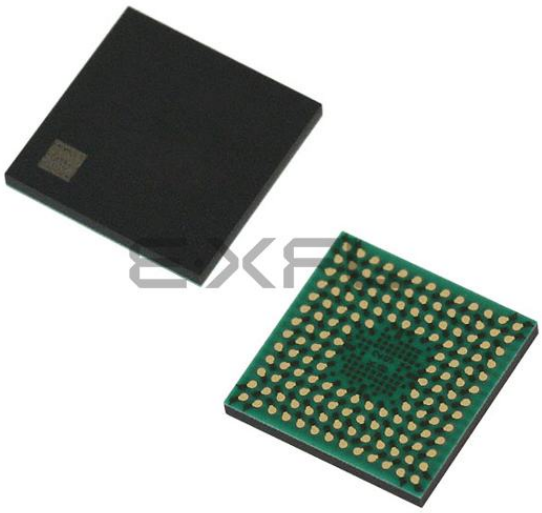

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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
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Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
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Supplier Device Package	145-TFLGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f61665n50lgv

4.3.2 Reset Control/Status Register (RSTCSR)

RSTCSR controls an internal reset signal generated by the watchdog timer and selects the internal reset signal type. RSTCSR is initialized to H'1F by a pin reset or a deep software standby reset, but not by the internal reset signal generated by a WDT overflow.

Bit	7	6	5	4	3	2	1	0
Bit name	WOVF	RSTE	—	—	—	—	—	—
Initial value:	0	0	0	1	1	1	1	1
R/W:	R/(W)*	R/W	R/W	R	R	R	R	R

Note: * Only 0 can be written to clear the flag.

Bit	Bit Name	Initial Value	R/W	Description
7	WOVF	0	R/(W)*	Watchdog Timer Overflow Flag This bit is set when TCNT overflows in watchdog timer mode, but not set in interval timer mode. Only 0 can be written to. [Setting condition] When TCNT overflows (H'FF → H'00) in watchdog timer mode. [Clearing condition] When this bit is read as 1 and then written by 0.
6	RSTE	0	R/W	Reset Enable Selects whether or not the LSI internal state is reset by a TCNT overflow in watchdog timer mode. 0: Internal state is not reset when TCNT overflows. (Although this LSI internal state is not reset, TCNT and TCSR of the WDT are reset.) 1: Internal state is reset when TCNT overflows.
5	—	0	R/W	Reserved Although this bit is readable/writable, operation is not affected by this bit.
4 to 0	—	1	R	Reserved These are read-only bits but cannot be modified.

Note: * Only 0 can be written to clear the flag.

(3) Refresh and All-Module Clock Stop Mode

This LSI is entered in all-module clock stop mode by the following operation: Stop the clocks of all on-chip peripheral modules by setting the ACSE bit in MSTPCR to 1 (MSTPCRA, MSTPCRB = H'FFFFFFFF) or run only the 8-bit timer (MSTPCRA, MSTPCRB = H'F[C to F]FFFFFF), then execute the SLEEP instruction to enter the sleep mode.

In all-module clock stop mode, clocks for the bus controller and I/O ports are stopped. Since the clock for the bus controller is stopped, a CBR refresh cycle cannot be performed. When external DRAM is used and the contents of the DRAM in sleep mode should be held, clear the ACSE bit in MSTPCE to 0.

For details, see section 28.2.2, Module Stop Control Registers A and B (MSTPCRA and MSTPCRB).

9.10.13 DRAM Interface and Single Address Transfer by DMAC and EXDMAC

When fast-page mode (BE = 1) is set for the DRAM space, either fast-page access or full access can be selected, by the setting of bits DDS and EDDS in DRAMCR, for the single address transfer by the DMAC or EXDMAC where the DRAM space is specified as the transfer source or destination. At the same time, the output timings of the $\overline{\text{DACK}}$, $\overline{\text{EDACK}}$ and BS signals are changed. When BE = 0, full access to the DRAM space is performed by single address transfer regardless of the setting of bits DDS and EDDS. However, the output timing of the $\overline{\text{DACK}}$, $\overline{\text{EDACK}}$ and BS signals can be changed by the setting of bits DDS and EDDS.

The assertion timing of the $\overline{\text{DACK}}$ and $\overline{\text{EDACK}}$ signal can be changed by bits DKC and EDKC in BCR1.

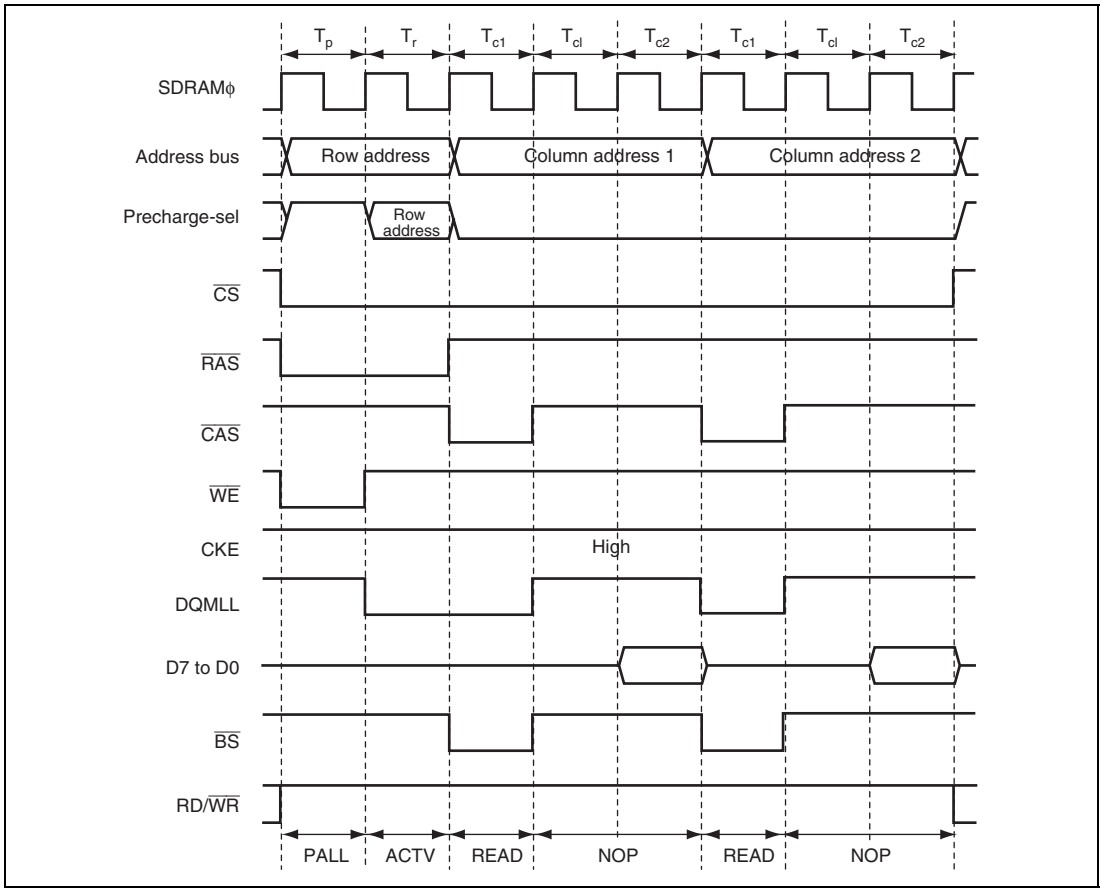


Figure 9.73 Word Read Timing in 8-Bit Access Space (BE = 1, RCDM = 0, CAS Latency = 2)

9.15.2 Write Data Buffer Function for Peripheral Modules

This LSI has a write data buffer function for the peripheral module access. Using the write data buffer function enables peripheral module writes and on-chip memory or external access to be executed in parallel. The write data buffer function is made available by setting the PWDBE bit in BCR2 to 1. For details on the on-chip peripheral module registers, see table 9.34, Number of Access Cycles for Registers of On-Chip Peripheral Modules in section 9.14, Internal Bus.

Figure 9.105 shows an example of the timing when the write data buffer function is used. When this function is used, if an internal I/O register write continues for two cycles or longer and then there is an on-chip RAM, an on-chip ROM, or an external access, internal I/O register write only is performed in the first two cycles. However, from the next cycle onward an internal memory or an external access and internal I/O register write are executed in parallel rather than waiting until it ends.

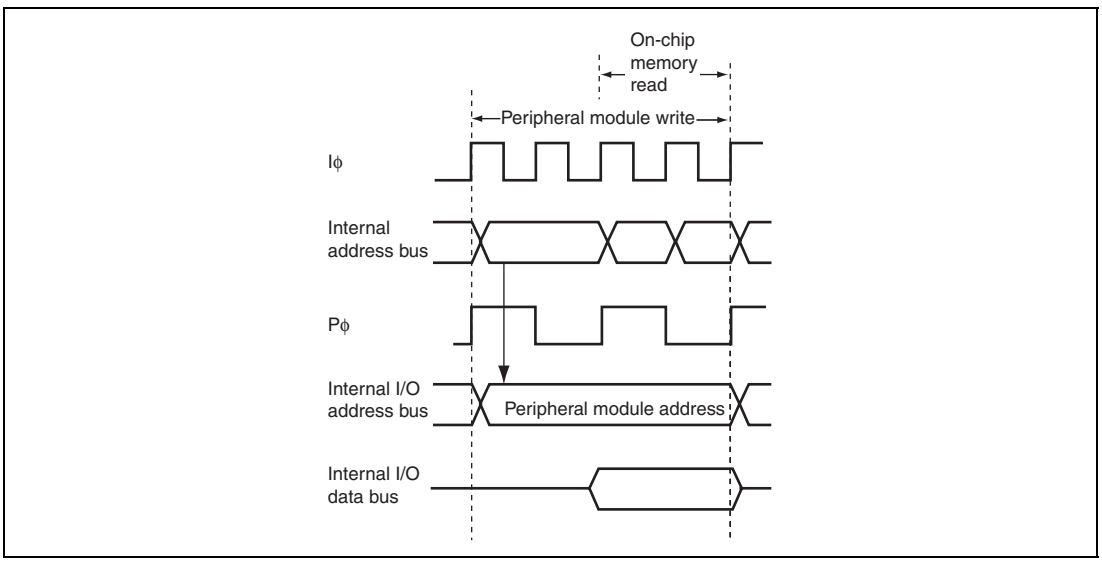


Figure 9.105 Example of Timing when Peripheral Module Write Data Buffer Function is Used

(3) $\overline{\text{EDREQ}}$ Pin Low Level Activation Timing

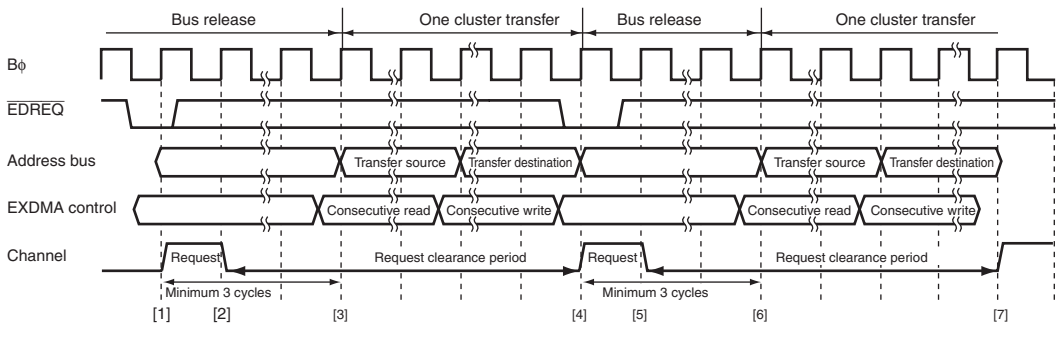
Figure 11.63 shows an example of cluster transfer mode transfer activated by the $\overline{\text{EDREQ}}$ pin low level.

$\overline{\text{EDREQ}}$ pin sampling is performed in each cycle starting at the next rise of Bϕ after the end of the DTE bit write cycle.

When a low level is sampled at the $\overline{\text{EDREQ}}$ pin while acceptance of a transfer request via the $\overline{\text{EDREQ}}$ pin is possible, the request is held within the EXDMAC. Then when activation is initiated within the EXDMAC, the request is cleared. At the end of the last cluster write cycle, acceptance resumes and $\overline{\text{EDREQ}}$ pin low level sampling is performed again. This sequence of operations is repeated until the end of the transfer.

When NRD bit = 0 in EDMDR, acceptance resumes at the end of the last cluster write cycle and $\overline{\text{EDREQ}}$ pin low level sampling is performed again. This sequence of operations is repeated until the end of the transfer.

When NRD bit = 1 in EDMDR, acceptance resumes after one cycle from the end of the last cluster write cycle, and $\overline{\text{EDREQ}}$ pin low level sampling is performed again. This sequence of operations is repeated until the end of the transfer.



[1] Acceptance after transfer enabling; $\overline{\text{EDREQ}}$ pin low level is sampled at rise of Bϕ, and request is held.
[2] [5] Request is cleared at the end of next bus cycle, and activation is started in EXDMAC.
[3] [6] EXDMA cycle stars.
[4] [7] Acceptance is resumed after completion of wite cycle.
(As in [1], EDREQ pin low level is sampled at rise of Bϕ, and request is held.)

Figure 11.63 Example of Cluster Transfer Mode Transfer Activated by $\overline{\text{EDREQ}}$ Pin Low Level

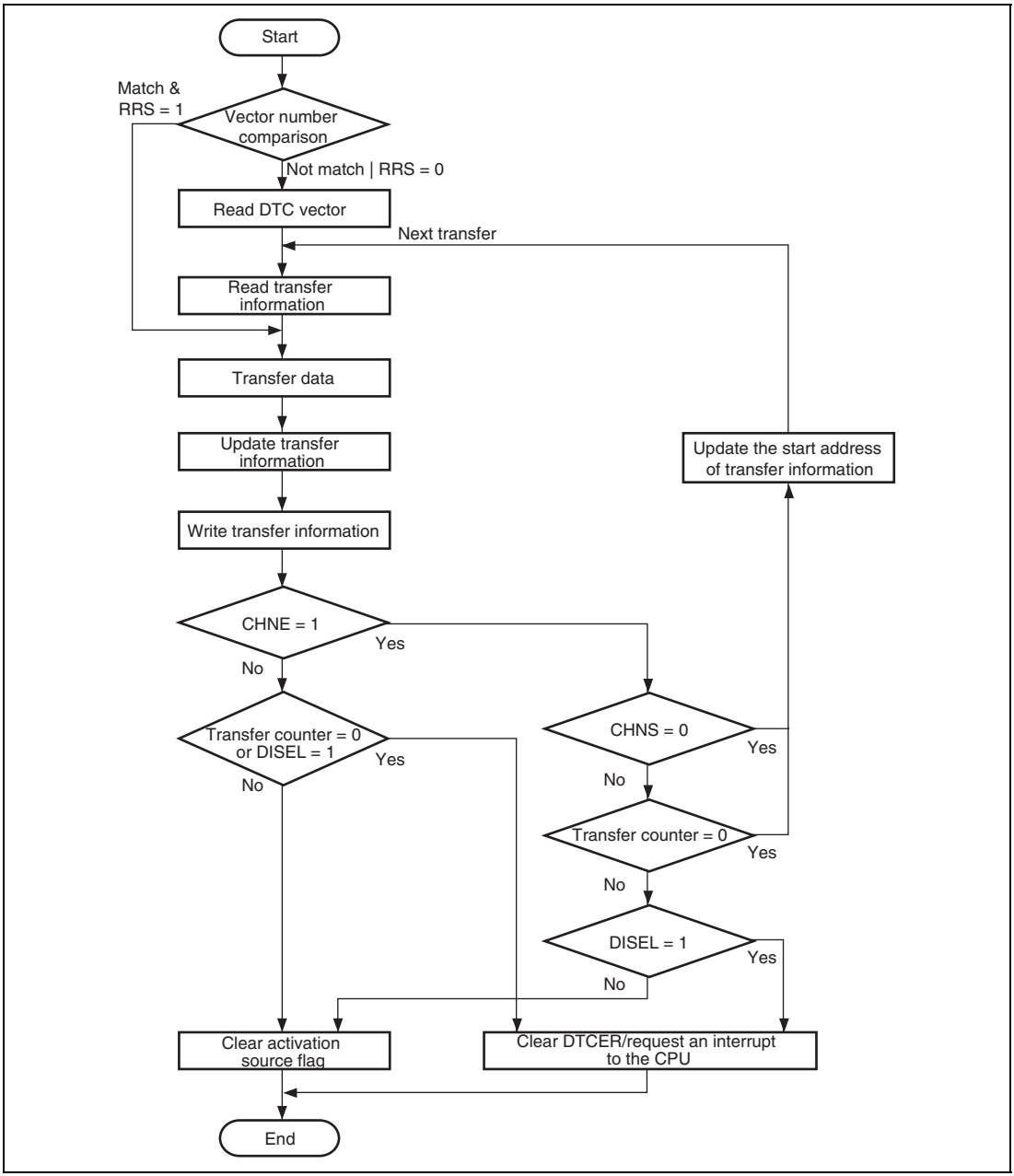


Figure 12.4 Flowchart of DTC Operation

Port		Output Specification Signal Name	Output Signal Name	Signal Selection Register Settings	Peripheral Module Settings
PA	1	$\overline{\text{BACK}}$_OE	$\overline{\text{BACK}}$		SYSCR.EXPE = 1,BCR1.BRLE = 1
		(RD/$\overline{\text{WR}}$-A)_OE	RD/$\overline{\text{WR}}$	PFCR2.RDWRS = 0	SYSCR.EXPE = 1, PFCR2.RDWRE = 1 or SRAMCR.BCSELn = 1
	0	$\overline{\text{BSA}}$_OE	$\overline{\text{BS}}$	PFCR2.BSS = 0	SYSCR.EXPE = 1, PFCR2.BSE = 1
		$\overline{\text{BREQO}}$_OE	$\overline{\text{BREQO}}$		SYSCR.EXPE = 1, BCR1.BRLE = 1, BCR1.BREQOE = 1
PB	7	SDRAMϕ_OE	SDRAMϕ		MDCR.MDS7 = 1
	6	(RD/$\overline{\text{WR}}$)-B_OE	RD/$\overline{\text{WR}}$	PFCR2.RDWRS = 1	SYSCR.EXPE=1, PFCR2.RDWRE = 1 or ASRAMCR.BCSELn = 1
		$\overline{\text{CS6D}}$_OE	$\overline{\text{CS6}}$	PFCR1.CS6S[A,B] = 11	SYSCR.EXPE = 1, PFCR0.CS6E = 1
	5	$\overline{\text{CKE}}$_OE	CKE		SYSCR.EXPE = 1, DRAMCR.DRAME = 1, DRAMCR.DTYPE = 1, DRAMCR.OEE = 1
		$\overline{\text{OE}}$_OE	$\overline{\text{OE}}$		SYSCR.EXPE = 1, DRAMCR.DRAME = 1, DRAMCR.DTYPE = 0, DRAMCR.OEE = 1
		$\overline{\text{CS5D}}$_OE	$\overline{\text{CS5}}$	PFCR1.CS5S[A,B] = 11	SYSCR.EXPE = 1, PFCR0.CS5E = 1
	4	$\overline{\text{WE}}$_OE	$\overline{\text{WE}}$		SYSCR.EXPE = 1, DRAMCR.DRAME = 1
		$\overline{\text{CS4B}}$_OE	$\overline{\text{CS4}}$	PFCR1.CS4S[A,B] = 01	SYSCR.EXPE = 1, PFCR0.CS4E = 1
	3	$\overline{\text{CAS}}$_OE	$\overline{\text{CAS}}$		SYSCR.EXPE = 1, DRAMCR.DRAME = 1, DRAMCR.DTYPE = 1
		$\overline{\text{CS3}}$_OE	$\overline{\text{CS3}}$		SYSCR.EXPE = 1, PFCR0.CS3E = 1
		$\overline{\text{CS7A}}$_OE	$\overline{\text{CS7}}$	PFCR1.CS7S[A,B] = 00	SYSCR.EXPE = 1, PFCR0.CS7E = 1
	2	$\overline{\text{RAS}}$_OE	$\overline{\text{RAS}}$		SYSCR.EXPE = 1, DRAMCR.DRAME = 1
		$\overline{\text{CS2A}}$_OE	$\overline{\text{CS2}}$	PFCR2.CS2S = 0	SYSCR.EXPE = 1, PFCR0.CS2E = 1
		$\overline{\text{CS6A}}$_OE	$\overline{\text{CS6}}$	PFCR1.CS6S[A,B] = 00	SYSCR.EXPE = 1, PFCR0.CS6E = 1

13.3.10 Port Function Control Register B (PFCRB)

PFCRB selects the LVD interrupt*, and the input pins for IRQ11 to IRQ8.

Bit	7	6	5	4	3	2	1	0
Bit Name	—	ITS14*	—	—	ITS11	ITS10	ITS9	ITS8
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Supported only by the H8SX/1665M Group.

- H8SX/1665 Group

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.

- H8SX/1665M Group

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R/W	Reserved This bit is always read as 0. The write value should always be 0.
6	ITS14	0	R/W	LVD Interrupt Select This bit allows or prohibits LVD interrupt. 0: Prohibits LVD interrupt 1: Allows LVD interrupt
5, 4	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
3	ITS11	0	R/W	$\overline{\text{IRQ11}}$ Pin Select Selects an input pin for $\overline{\text{IRQ11}}$. 0: Selects pin P23 as $\overline{\text{IRQ11}}$-A input 1: Selects pin P63 as $\overline{\text{IRQ11}}$-B input

Item	Channel 0	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
DMAC activation	TGRA_0 compare match or input capture	TGRA_1 compare match or input capture	TGRA_2 compare match or input capture	TGRA_3 compare match or input capture	TGRA_4 compare match or input capture	TGRA_5 compare match or input capture
A/D conversion start trigger	TGRA_0 compare match or input capture	TGRA_1 compare match or input capture	TGRA_2 compare match or input capture	TGRA_3 compare match or input capture	TGRA_4 compare match or input capture	TGRA_5 compare match or input capture
PPG trigger	TGRA_0/ TGRB_0 compare match or input capture	TGRA_1/ TGRB_1 compare match or input capture	TGRA_2/ TGRB_2 compare match or input capture	TGRA_3/ TGRB_3 compare match or input capture	—	—
Interrupt sources	5 sources	4 sources	4 sources	5 sources	4 sources	4 sources
	Compare match or input capture 0A	Compare match or input capture 1A	Compare match or input capture 2A	Compare match or input capture 3A	Compare match or input capture 4A	Compare match or input capture 5A
	Compare match or input capture 0B	Compare match or input capture 1B	Compare match or input capture 2B	Compare match or input capture 3B	Compare match or input capture 4B	Compare match or input capture 5B
	Compare match or input capture 0C			Compare match or input capture 3C		
	Compare match or input capture 0D			Compare match or input capture 3D		
	Overflow	Overflow	Overflow	Overflow	Overflow	Overflow
		Underflow	Underflow		Underflow	Underflow

[Legend]

O: Possible

—: Not possible

(2) Examples of Phase Counting Mode Operation

In phase counting mode, TCNT counts up or down according to the phase difference between two external clocks. There are four modes, according to the count conditions.

(a) Phase counting mode 1

Figure 14.26 shows an example of phase counting mode 1 operation, and table 14.34 summarizes the TCNT up/down-count conditions.

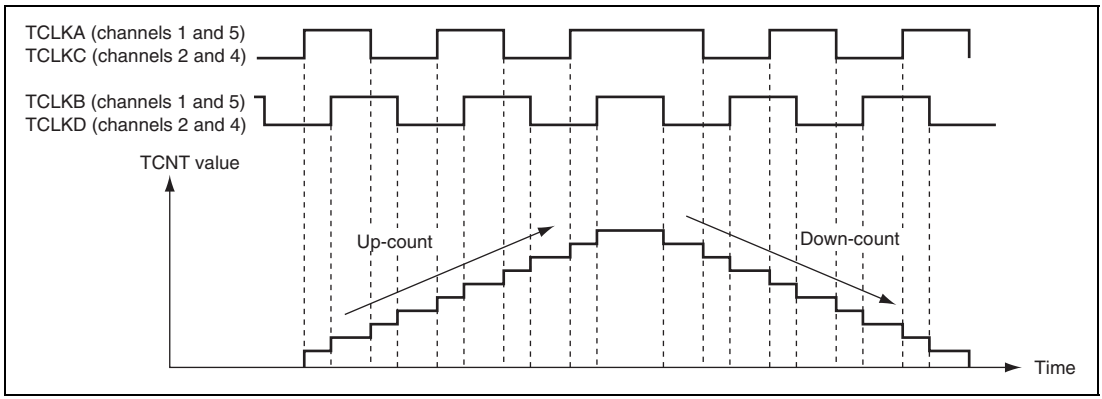


Figure 14.26 Example of Phase Counting Mode 1 Operation

Table 14.34 Up/Down-Count Conditions in Phase Counting Mode 1

TCLKA (Channels 1 and 5) TCLKC (Channels 2 and 4)	TCLKB (Channels 1 and 5) TCLKD (Channels 2 and 4)	Operation
High level	↑	Up-count
Low level	↓	
↑	Low level	
↓	High level	
High level	↓	Down-count
Low level	↑	
↑	High level	
↓	Low level	

[Legend]
↑: Rising edge
↓: Falling edge

(d) Phase counting mode 4

Figure 14.29 shows an example of phase counting mode 4 operation, and table 14.37 summarizes the TCNT up/down-count conditions.

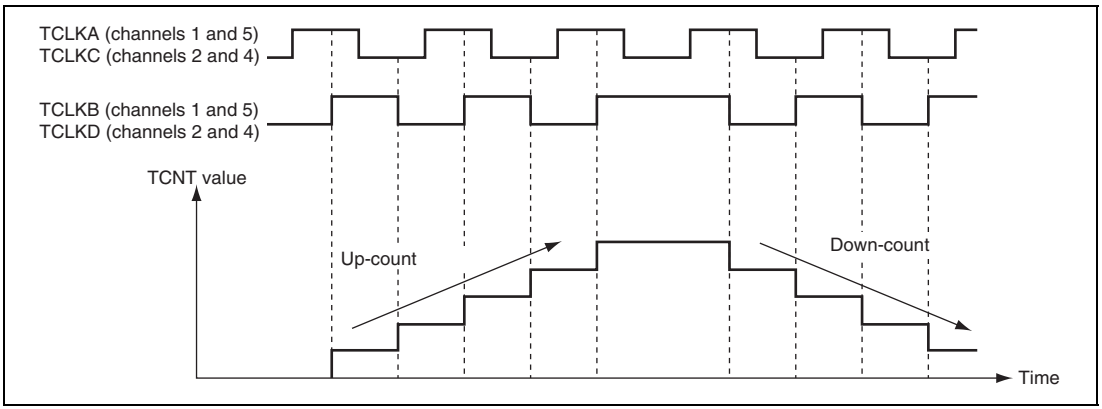


Figure 14.29 Example of Phase Counting Mode 4 Operation

Table 14.37 Up/Down-Count Conditions in Phase Counting Mode 4

TCLKA (Channels 1 and 5) TCLKC (Channels 2 and 4)	TCLKB (Channels 1 and 5) TCLKD (Channels 2 and 4)	Operation
High level	⌜↑	Up-count
Low level	↓⌟	
⌜↑	Low level	Don't care
↓⌟	High level	
High level	↓⌟	Down-count
Low level	⌜↑	
⌜↑	High level	Don't care
↓⌟	Low level	

[Legend]
⌜↑: Rising edge
↓⌟: Falling edge

Table 19.1 lists the functions of each channel.

Table 19.1 Function List of SCI Channels

		SCI_0, 1, 4	SCI_2	SCI_5, SCI_6
Clocked synchronous mode		O	O	—
Asynchronous mode		O	O	O
TMR clock input		—	—	O
When average transfer rate generator is used	Pϕ = 8 MHz	—	—	460.784 kbps
	Pϕ = 10.667 MHz	—	460.784 kbps	460.606 kbps
			115.192 kbps	115.152 kbps
	Pϕ = 12 MHz	—	—	460.526 kbps
				230.263 kbps
	Pϕ = 16 MHz	—	720 kbps	921.569 kbps
			460 784kbps	720 kbps
			115.192 kbps	460.784 kbps
				115.196 kbps
	Pϕ = 24 MHz	—	—	921.053 kbps
				720 kbps
				460.526 kbps
				115.132 kbps
	Pϕ = 32 MHz	—	720 kbps	720 kbps

Bit	Bit Name	Initial Value	R/W	Description
3	ACS3	0	R/W	0000: Average transfer rate generator is not used.
2	ACS2	0	R/W	0001: 115.152 kbps of average transfer rate specific to Pϕ = 10.667 MHz is selected (operated using the base clock with a frequency 16 times the transfer rate)
1	ACS1	0	R/W	
0	ACS0	0	R/W	

0010: 460.606 kbps of average transfer rate specific to Pϕ = 10.667 MHz is selected (operated using the base clock with a frequency 8 times the transfer rate)

0011: 921.569 kbps of average transfer rate specific to Pϕ = 16 MHz is selected or 460.784 kbps of average transfer rate specific to Pϕ = 8MHz is selected (operated using the base clock with a frequency 8 times the transfer rate)

0100: TMR clock input
This setting allows the TMR compare match output to be used as the base clock. The table below shows the correspondence between the SCI channels and the compare match output.

SCI Channel	TMR Unit	Compare Match Output
SCI_5	Unit 2	TMO4, TMO5
SCI_6	Unit 3	TMO6, TMO7

0101: 115.196 kbps of average transfer rate specific to Pϕ = 16 MHz is selected (operated using the base clock with a frequency 16 times the transfer rate)

0110: 460.784 kbps of average transfer rate specific to Pϕ = 16 MHz is selected (operated using the base clock with a frequency 16 times the transfer rate)

0111: 720 kbps of average transfer rate specific to Pϕ = 16 MHz is selected (operated using the base clock with a frequency 8 times the transfer rate)

20.3.6 Interrupt Select Register 2 (ISR2)

ISR2 selects the vector numbers of the interrupt requests indicated in interrupt flag register 2 (IFR2). If the USB issues an interrupt request to the INTC when a bit in ISR2 is cleared to 0, the interrupt corresponding to the bit will be USBINTN2. If the USB issues an interrupt request to the INTC when a bit in ISR2 is set to 1, the corresponding interrupt will be USBINTN3.

Bit	7	6	5	4	3	2	1	0
Bit Name	—	—	—	SURSE	CFDN	—	SETCE	SETIE
Initial Value	0	0	0	1	1	1	1	1
R/W	R	R	R	R/W	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R	Reserved
6	—	0	R	These bits are always read as 0. The write value should always be 0.
5	—	0	R	
4	SURSE	1	R/W	Suspend/Resume Detection
3	CFDN	1	R/W	End Point Information Load End
2	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
1	SETCE	1	R/W	Set_Configuration Command Detection
0	SETIE	1	R/W	Set_Interface Command Detection

Section 21 I²C Bus Interface 2 (IIC2)

This LSI has a two-channel I²C bus interface.

The I²C bus interface conforms to and provides a subset of the Philips I²C bus (inter-IC bus) interface functions. The register configuration that controls the I²C bus differs partly from the Philips configuration, however.

Figure 21.1 shows the block diagram of the I²C bus interface 2.

Figure 21.2 shows an example of I/O pin connections to external circuits.

21.1 Features

- Continuous transmission/reception

  Since the shift register, transmit data register, and receive data register are independent from each other, the continuous transmission/reception can be performed.
- Start and stop conditions generated automatically in master mode
- Selection of acknowledge output levels when receiving
- Automatic loading of acknowledge bit when transmitting
- Bit synchronization/wait function

  In master mode, the state of SCL is monitored per bit, and the timing is synchronized automatically. If transmission or reception is not yet possible, drive the SCL signal low until preparations are completed
- Six interrupt sources

  Transmit-data-empty (including slave-address match), transmit-end, receive-data-full (including slave-address match), arbitration lost, NACK detection, and stop condition detection
- Direct bus drive

  Two pins, the SCL and SDA pins function as NMOS open-drain outputs.
- Module stop state can be set.

Bit	Bit Name	Initial Value	R/W	Description
5	RDRF	0	R/W	Receive Data Register Full [Setting condition] • When receive data is transferred from ICDRS to ICDRR [Clearing conditions] • When 0 is written to this bit after reading RDRF = 1 (When the CPU is used to clear this flag by writing 0 while the corresponding interrupt is enabled, be sure to read the flag after writing 0 to it.) • When data is read from ICDRR
4	NACKF	0	R/W	No Acknowledge Detection Flag [Setting condition] • When no acknowledge is detected from the receive device in transmission while the ACKE bit in ICIER is set to 1 [Clearing condition] • When 0 is written to this bit after reading NACKF = 1 (When the CPU is used to clear this flag by writing 0 while the corresponding interrupt is enabled, be sure to read the flag after writing 0 to it.)
3	STOP	0	R/W	Stop Condition Detection Flag [Setting condition] • When a stop condition is detected after frame transfer [Clearing condition] • When 0 is written to this bit after reading STOP = 1 (When the CPU is used to clear this flag by writing 0 while the corresponding interrupt is enabled, be sure to read the flag after writing 0 to it.)

25.8.1 Boot Mode

SCI Boot mode executes programming/erasure of the user MAT or user boot MAT by means of the control command and program data transmitted from the externally connected host via the on-chip SCI_4.

In SCI boot mode, the tool for transmitting the control command and program data, and the program data must be prepared in the host. The serial communications mode is set to asynchronous mode. The system configuration in boot mode is shown in figure 25.6. Interrupts are ignored in SCI boot mode. Configure the user system so that interrupts do not occur.

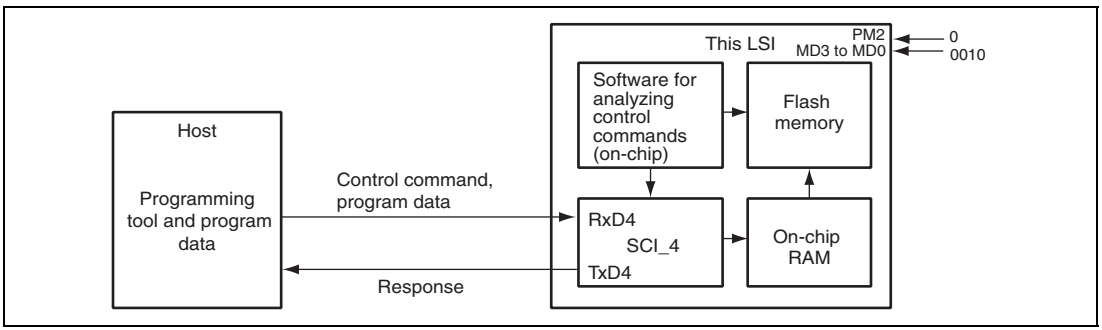


Figure 25.6 System Configuration in Boot Mode

Register Name	Abbreviation	Number of Bits	Address	Module	Data Width	Access Cycles (Read/Write)
IRQ sense control register L	ISCRL	16	H'FFD6A	INTC	16	2Iϕ/3Iϕ
DTC vector base register	DTCVBR	32	H'FFD80	BSC	16	2Iϕ/3Iϕ
Bus width control register	ABWCR	16	H'FFD84	BSC	16	2Iϕ/3Iϕ
Access state control register	ASTCR	16	H'FFD86	BSC	16	2Iϕ/3Iϕ
Wait control register A	WTCRA	16	H'FFD88	BSC	16	2Iϕ/3Iϕ
Wait control register B	WTCRB	16	H'FFD8A	BSC	16	2Iϕ/3Iϕ
Read strobe timing control register	RDNCR	16	H'FFD8C	BSC	16	2Iϕ/3Iϕ
$\overline{CS}$ assertion period control register	CSACR	16	H'FFD8E	BSC	16	2Iϕ/3Iϕ
Idle control register	IDLCR	16	H'FFD90	BSC	16	2Iϕ/3Iϕ
Bus control register 1	BCR1	16	H'FFD92	BSC	16	2Iϕ/3Iϕ
Bus control register 2	BCR2	8	H'FFD94	BSC	16	2Iϕ/3Iϕ
Endian control register	ENDIANCR	8	H'FFD95	BSC	16	2Iϕ/3Iϕ
SRAM mode control register	SRAMCR	16	H'FFD98	BSC	16	2Iϕ/3Iϕ
Burst ROM interface control register	BROMCR	16	H'FFD9A	BSC	16	2Iϕ/3Iϕ
Address/data multiplexed I/O control register	MPXCR	16	H'FFD9C	BSC	16	2Iϕ/3Iϕ
DRAM control register	DRAMCR	16	H'FFDA0	BSC	16	2Iϕ/3Iϕ
DRAM access control register	DRACCR	16	H'FFDA2	BSC	16	2Iϕ/3Iϕ
Synchronous DRAM control register	SDCR	16	H'FFDA4	BSC	16	2Iϕ/3Iϕ
Refresh control register	REFCR	16	H'FFDA6	BSC	16	2Iϕ/3Iϕ
Refresh timer counter	RTCNT	8	H'FFDA8	BSC	16	2Iϕ/3Iϕ
Refresh time constant register	RTCOR	8	H'FFDA9	BSC	16	2Iϕ/3Iϕ
RAM emulation register	RAMER	8	H'FFD9E	BSC	16	2Iϕ/3Iϕ
Mode control register	MDCR	16	H'FFDC0	SYSTEM	16	2Iϕ/3Iϕ
System control register	SYSCR	16	H'FFDC2	SYSTEM	16	2Iϕ/3Iϕ
System clock control register	SCKCR	16	H'FFDC4	SYSTEM	16	2Iϕ/3Iϕ
Standby control register	SBYCR	16	H'FFDC6	SYSTEM	16	2Iϕ/3Iϕ
Module stop control register A	MSTPCRA	16	H'FFDC8	SYSTEM	16	2Iϕ/3Iϕ
Module stop control register B	MSTPCRB	16	H'FFDCA	SYSTEM	16	2Iϕ/3Iϕ
Module stop control register C	MSTPCRC	16	H'FFDCC	SYSTEM	16	2Iϕ/3Iϕ
Subclock control register	SUBCKCR	8	H'FFDCF	SYSTEM	16	2Iϕ/3Iϕ
Flash code control/status register	FCCS	8	H'FFDE8	FLASH	16	2Iϕ/2Iϕ

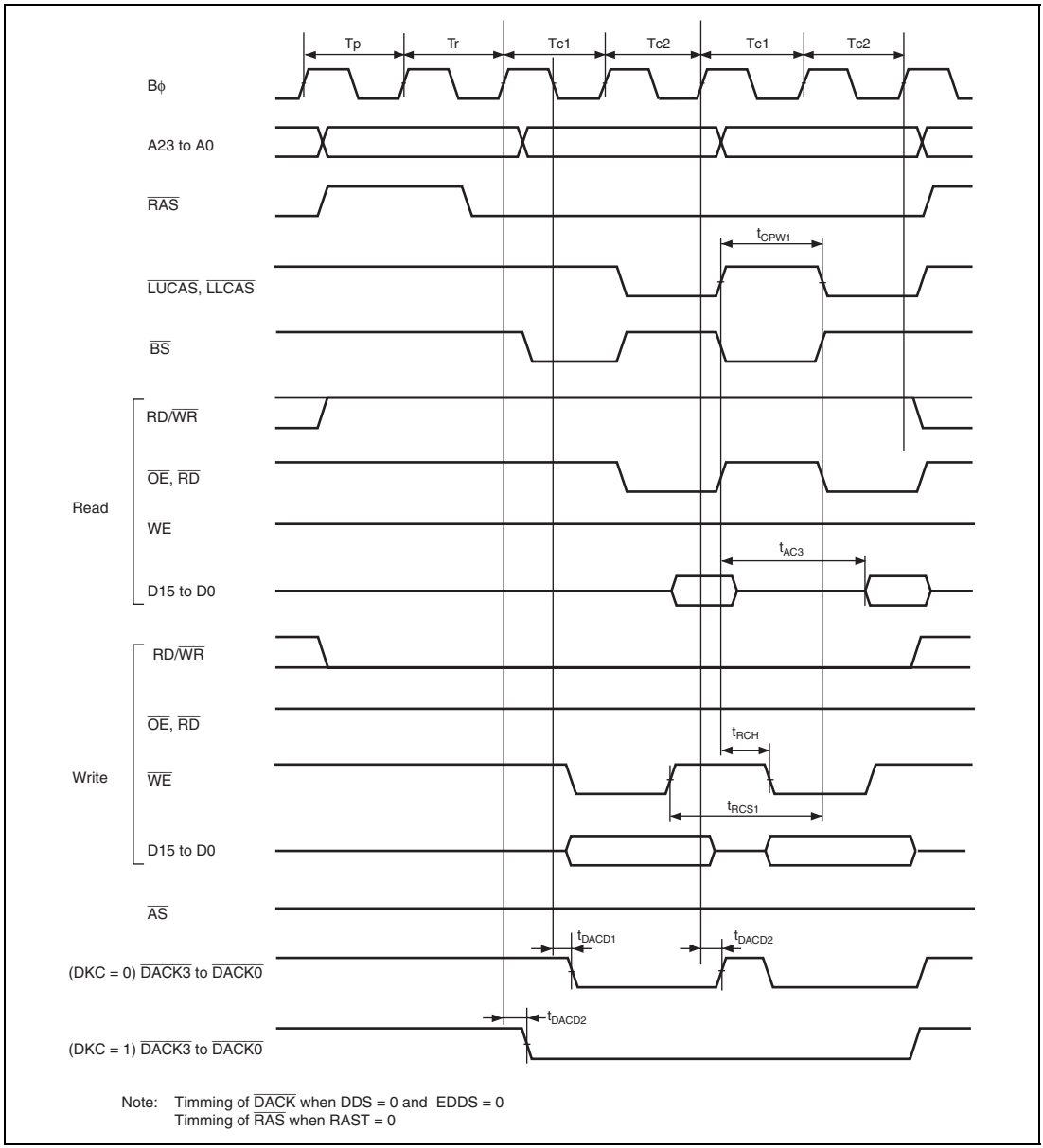


Figure 30.21 DRAM Access Timing: Two-State Burst Access