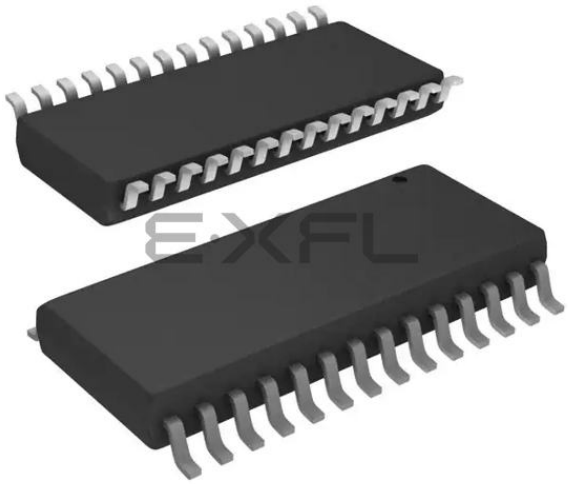

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	24
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f882-i-so

PIC16F882/883/884/886/887 Family Types

Device	Program Memory	Data Memory		I/O	10-bit A/D (ch)	ECCP/ CCP	EUSART	MSSP	Comparators	Timers 8/16-bit
	Flash (words)	SRAM (bytes)	EEPROM (bytes)							
PIC16F882	2048	128	128	24	11	1/1	1	1	2	2/1
PIC16F883	4096	256	256	24	11	1/1	1	1	2	2/1
PIC16F884	4096	256	256	35	14	1/1	1	1	2	2/1
PIC16F886	8192	368	256	24	11	1/1	1	1	2	2/1
PIC16F887	8192	368	256	35	14	1/1	1	1	2	2/1

Pin Diagrams – PIC16F882/883/886, 28-Pin PDIP, SOIC, SSOP

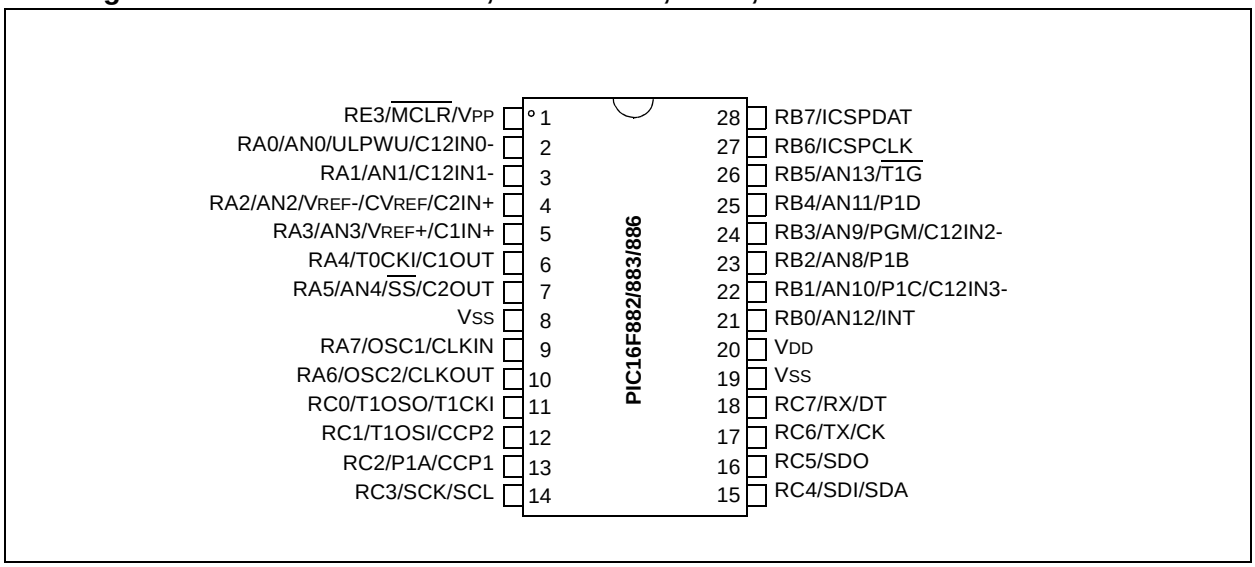


TABLE 2: 28-PIN QFN ALLOCATION TABLE (PIC16F882/883/886)

I/O	28-Pin QFN	Analog	Comparators	Timers	ECCP	EUSART	MSSP	Interrupt	Pull-up	Basic
RA0	27	AN0/ULPWU	C12IN0-	—	—	—	—	—	—	—
RA1	28	AN1	C12IN1-	—	—	—	—	—	—	—
RA2	1	AN2	C2IN+	—	—	—	—	—	—	VREF-/CVREF
RA3	2	AN3	C1IN+	—	—	—	—	—	—	VREF+
RA4	3	—	C1OUT	T0CKI	—	—	—	—	—	—
RA5	4	AN4	C2OUT	—	—	—	$\overline{SS}$	—	—	—
RA6	7	—	—	—	—	—	—	—	—	OSC2/CLKOUT
RA7	6	—	—	—	—	—	—	—	—	OSC1/CLKIN
RB0	18	AN12	—	—	—	—	—	IOC/INT	Y	—
RB1	19	AN10	C12IN3-	—	P1C	—	—	IOC	Y	—
RB2	20	AN8	—	—	P1B	—	—	IOC	Y	—
RB3	21	AN9	C12IN2-	—	—	—	—	IOC	Y	PGM
RB4	22	AN11	—	—	P1D	—	—	IOC	Y	—
RB5	23	AN13	—	$\overline{T1G}$	—	—	—	IOC	Y	—
RB6	24	—	—	—	—	—	—	IOC	Y	ICSPCLK
RB7	25	—	—	—	—	—	—	IOC	Y	ICSPDAT
RC0	8	—	—	T1OSO/T1CKI	—	—	—	—	—	—
RC1	9	—	—	T1OSI	CCP2	—	—	—	—	—
RC2	10	—	—	—	CCP1/P1A	—	—	—	—	—
RC3	11	—	—	—	—	—	SCK/SCL	—	—	—
RC4	12	—	—	—	—	—	SDI/SDA	—	—	—
RC5	13	—	—	—	—	—	SDO	—	—	—
RC6	14	—	—	—	—	TX/CK	—	—	—	—
RC7	15	—	—	—	—	RX/DT	—	—	—	—
RE3	26	—	—	—	—	—	—	—	Y(1)	$\overline{MCLR}$/VPP
—	17	—	—	—	—	—	—	—	—	VDD
—	5	—	—	—	—	—	—	—	—	VSS
—	16	—	—	—	—	—	—	—	—	VSS

Note 1: Pull-up activated only with external $\overline{MCLR}$ configuration.

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC16F882/883/884/886/887 devices have a 13-bit program counter capable of addressing a 2K x 14 (0000h-07FFh) for the PIC16F882, 4K x 14 (0000h-0FFFh) for the PIC16F883/PIC16F884, and 8K x 14 (0000h-1FFFh) for the PIC16F886/PIC16F887 program memory space. Accessing a location above these boundaries will cause a wrap-around within the first 8K x 14 space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figures 2-2 and 2-3).

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F882

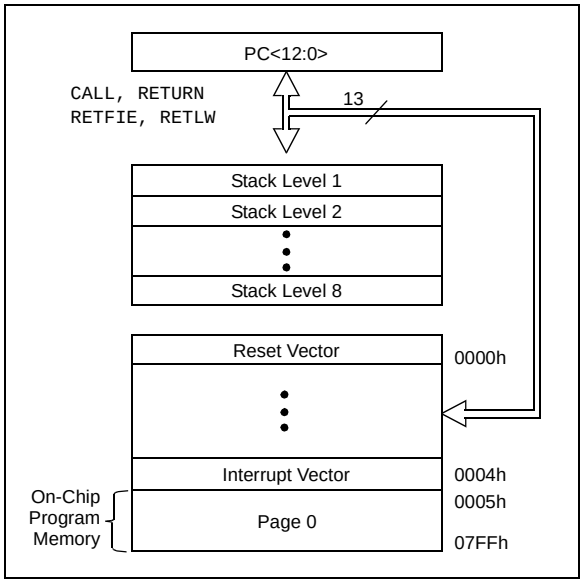


FIGURE 2-2: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F883/PIC16F884

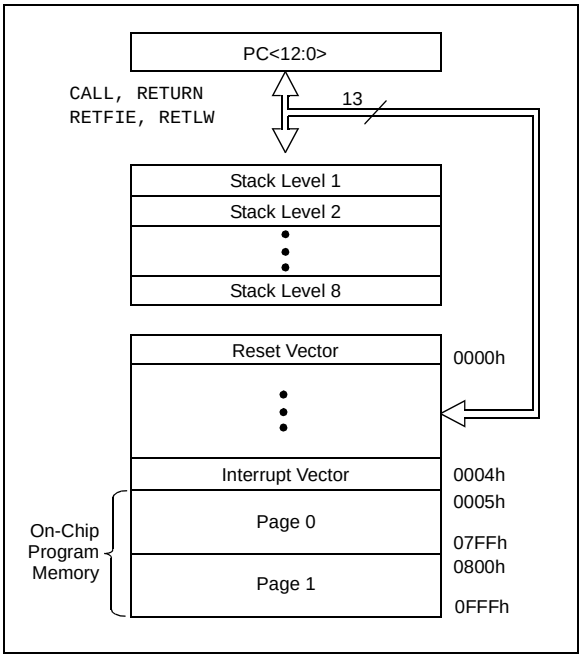


FIGURE 2-3: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F886/PIC16F887

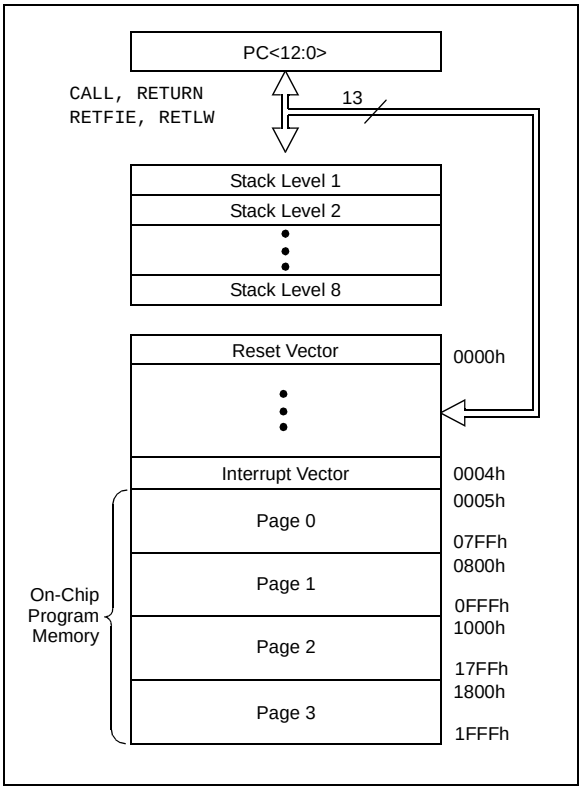
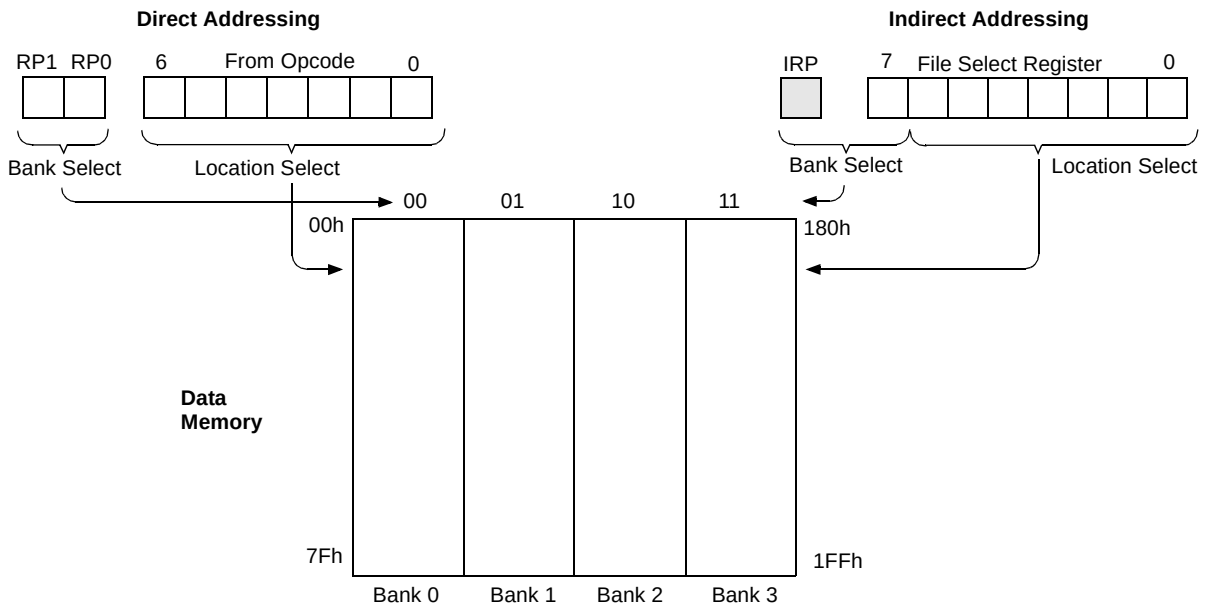


FIGURE 2-8: DIRECT/INDIRECT ADDRESSING PIC16F882/883/884/886/887



Note: For memory map detail, see Figures 2-2 and 2-3.

4.5.2.1 OSCTUNE Register

The HFINTOSC is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 4-2).

The default value of the OSCTUNE register is '0'. The value is a 5-bit two's complement number.

When the OSCTUNE register is modified, the HFINTOSC frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

REGISTER 4-2: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TUN<4:0>:** Frequency Tuning bits

01111 = Maximum frequency
01110 =
•
•
•
00001 =
00000 = Oscillator module is running at the factory-calibrated frequency.
11111 =
•
•
•
10000 = Minimum frequency

FIGURE 10-2: BLOCK WRITES TO 2K AND 4K FLASH PROGRAM MEMORY

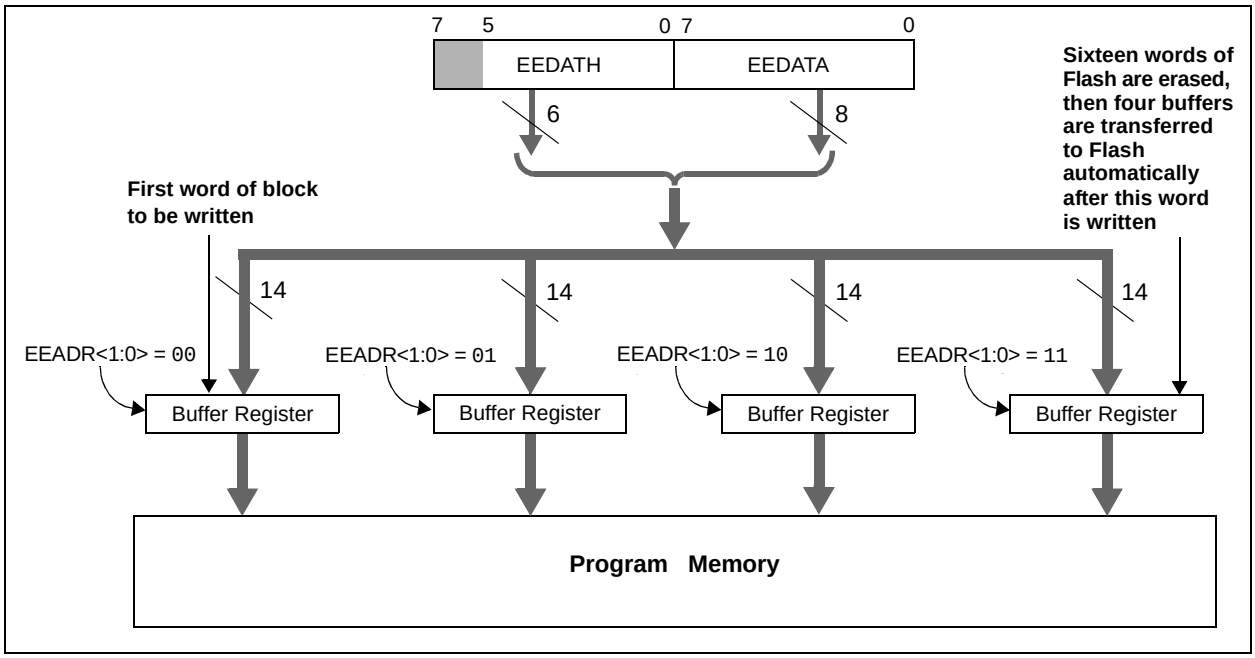


FIGURE 10-3: BLOCK WRITES TO 8K FLASH PROGRAM MEMORY

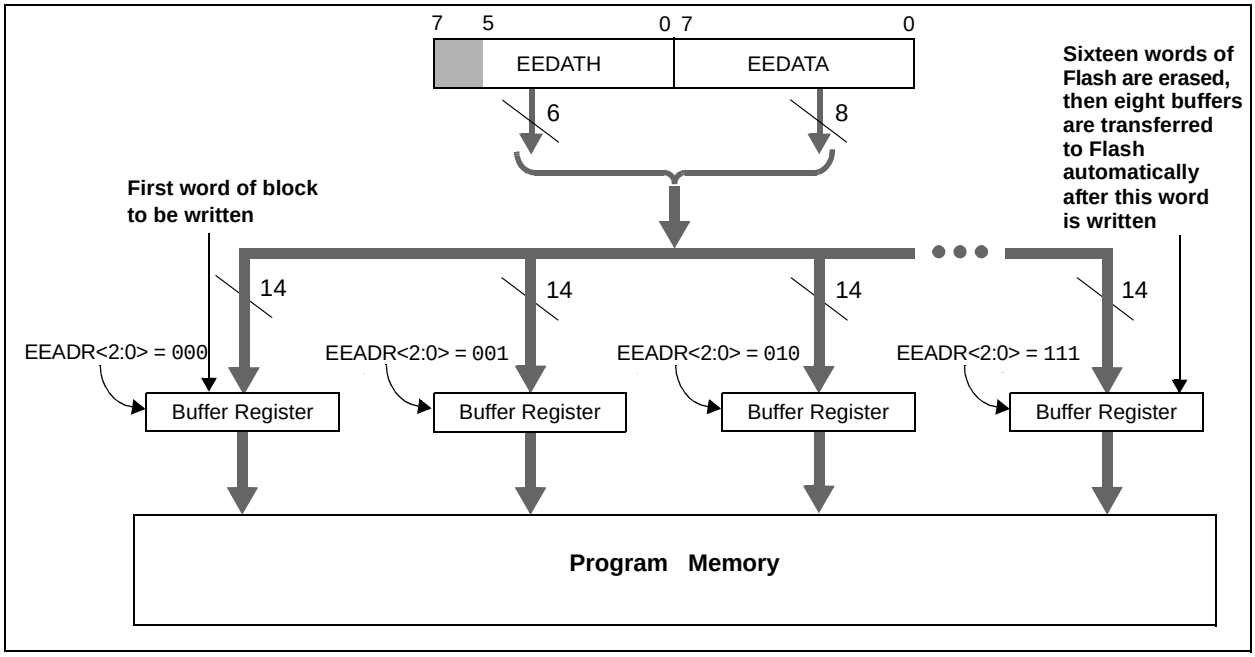


TABLE 10-1: SUMMARY OF REGISTERS ASSOCIATED WITH DATA EEPROM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
EECON1	EEPGD	—	—	—	WRERR	WREN	WR	RD	112
EECON2	EEPROM Control Register 2 (not a physical register)								—
EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	111
EEADRH	—	—	—	EEADRH4(1)	EEADRH3	EEADRH2	EEADRH1	EEADRH0	111
EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	111
EEDATH	—	—	EEDATH5	EEDATH4	EEDATH3	EEDATH2	EEDATH1	EEDATH0	111
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	32
PIE2	OSFIE	C2IE	C1IE	EEIE	BCLIE	ULPWUIE	—	CCP2IE	34
PIR2	OSFIF	C2IF	C1IF	EEIF	BCLIF	ULPWUIF	—	CCP2IF	36

Legend: x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by data EEPROM module.

Note 1: PIC16F886/PIC16F887 only.

11.6.2.1 Direction Change in Full-Bridge Mode

In the Full-Bridge mode, the P1M1 bit in the CCP1CON register allows users to control the forward/reverse direction. When the application firmware changes this direction control bit, the module will change to the new direction on the next PWM cycle.

A direction change is initiated in software by changing the P1M1 bit of the CCP1CON register. The following sequence occurs prior to the end of the current PWM period:

- The modulated outputs (P1B and P1D) are placed in their inactive state.
- The associated unmodulated outputs (P1A and P1C) are switched to drive in the opposite direction.
- PWM modulation resumes at the beginning of the next period.

See Figure 11-12 for an illustration of this sequence.

The Full-Bridge mode does not provide dead-band delay. As one output is modulated at a time, dead-band delay is generally not required. There is a situation where dead-band delay is required. This situation occurs when both of the following conditions are true:

1. The direction of the PWM output changes when the duty cycle of the output is at or near 100%.
2. The turn off time of the power switch, including the power device and driver circuit, is greater than the turn on time.

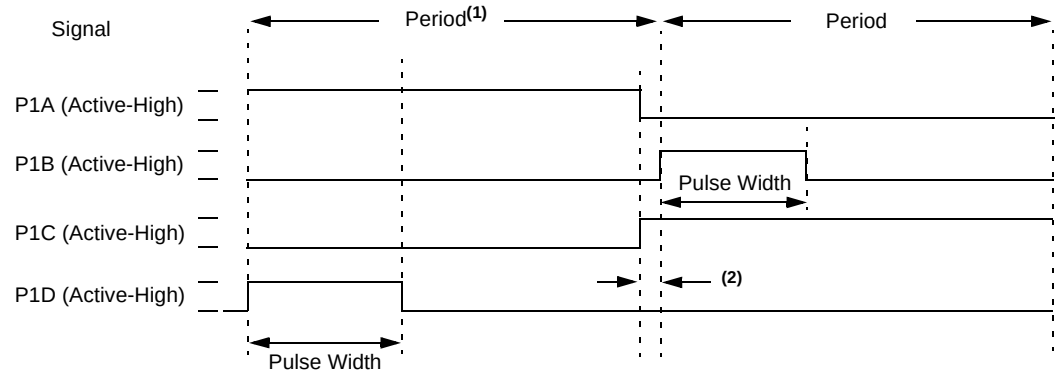
Figure 11-13 shows an example of the PWM direction changing from forward to reverse, at a near 100% duty cycle. In this example, at time t1, the output P1A and P1D become inactive, while output P1C becomes active. Since the turn off time of the power devices is longer than the turn on time, a shoot-through current will flow through power devices QC and QD (see Figure 11-10) for the duration of 't'. The same phenomenon will occur to power devices QA and QB for PWM direction change from reverse to forward.

If changing PWM direction at high duty cycle is required for an application, two possible solutions for eliminating the shoot-through current are:

1. Reduce PWM duty cycle for one PWM period before changing directions.
2. Use switch drivers that can drive the switches off faster than they can drive them on.

Other options to prevent shoot-through current may exist.

FIGURE 11-12: EXAMPLE OF PWM DIRECTION CHANGE



Note 1: The direction bit P1M1 of the CCP1CON register is written any time during the PWM cycle.

2: When changing directions, the P1A and P1C signals switch before the end of the current PWM cycle. The modulated P1B and P1D signals are inactive at this time. The length of this time is (1/Fosc) • TMR2 prescale value.

12.1.1.4 TSR Status

The TRMT bit of the TXSTA register indicates the status of the TSR register. This is a read-only bit. The TRMT bit is set when the TSR register is empty and is cleared when a character is transferred to the TSR register from the TXREG. The TRMT bit remains clear until all bits have been shifted out of the TSR register. No interrupt logic is tied to this bit, so the user has to poll this bit to determine the TSR status.

Note:	The TSR register is not mapped in data memory, so it is not available to the user.

12.1.1.5 Transmitting 9-Bit Characters

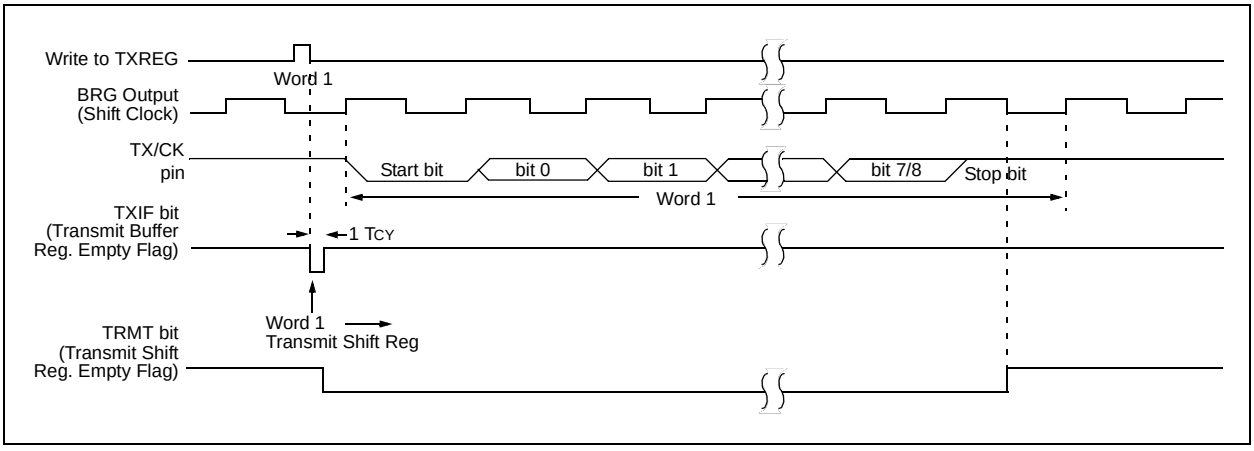
The EUSART supports 9-bit character transmissions. When the TX9 bit of the TXSTA register is set the EUSART will shift nine bits out for each character transmitted. The TX9D bit of the TXSTA register is the ninth, and Most Significant, data bit. When transmitting 9-bit data, the TX9D data bit must be written before writing the eight Least Significant bits into the TXREG. All nine bits of data will be transferred to the TSR shift register immediately after the TXREG is written.

A special 9-bit Address mode is available for use with multiple receivers. See **Section 12.1.2.7 "Address Detection"** for more information on the Address mode.

12.1.1.6 Asynchronous Transmission Setup:

1. Initialize the SPBRGH, SPBRG register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 12.3 "EUSART Baud Rate Generator (BRG)"**).
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. If 9-bit transmission is desired, set the TX9 control bit. A set ninth data bit will indicate that the eight Least Significant data bits are an address when the receiver is set for address detection.
4. Enable the transmission by setting the TXEN control bit. This will cause the TXIF interrupt bit to be set.
5. If interrupts are desired, set the TXIE interrupt enable bit of the PIE1 register. An interrupt will occur immediately provided that the GIE and PEIE bits of the INTCON register are also set.
6. If 9-bit transmission is selected, the ninth bit should be loaded into the TX9D data bit.
7. Load 8-bit data into the TXREG register. This will start the transmission.

FIGURE 12-3: ASYNCHRONOUS TRANSMISSION



12.4.2.3 EUSART Synchronous Slave Reception

The operation of the Synchronous Master and Slave modes is identical (**Section 12.4.1.5 "Synchronous Master Reception"**), with the following exceptions:

- Sleep
- CREN bit is always set, therefore the receiver is never Idle
- SREN bit, which is a "don't care" in Slave mode

A character may be received while in Sleep mode by setting the CREN bit prior to entering Sleep. Once the word is received, the RSR register will transfer the data to the RCREG register. If the RCIE enable bit is set, the interrupt generated will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will branch to the interrupt vector.

12.4.2.4 Synchronous Slave Reception Setup:

1. Set the SYNC and SPEN bits and clear the CSRC bit.
2. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
3. If 9-bit reception is desired, set the RX9 bit.
4. Set the CREN bit to enable reception.
5. The RCIF bit will be set when reception is complete. An interrupt will be generated if the RCIE bit was set.
6. If 9-bit mode is enabled, retrieve the Most Significant bit from the RX9D bit of the RCSTA register.
7. Retrieve the eight Least Significant bits from the receive FIFO by reading the RCREG register.
8. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

TABLE 12-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BAUDCTL	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	159
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	32
PIE1	—	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	33
PIR1	—	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	35
RCREG	EUSART Receive Data Register								155
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	158
SPBRG	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	160
SPBRGH	BRG15	BRG14	BRG13	BRG12	BRG11	BRG10	BRG9	BRG8	160
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	54
TXREG	EUSART Transmit Data Register								150
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	157

Legend: x = unknown, – = unimplemented read as '0'. Shaded cells are not used for Synchronous Slave Reception.

FIGURE 13-4: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 0)

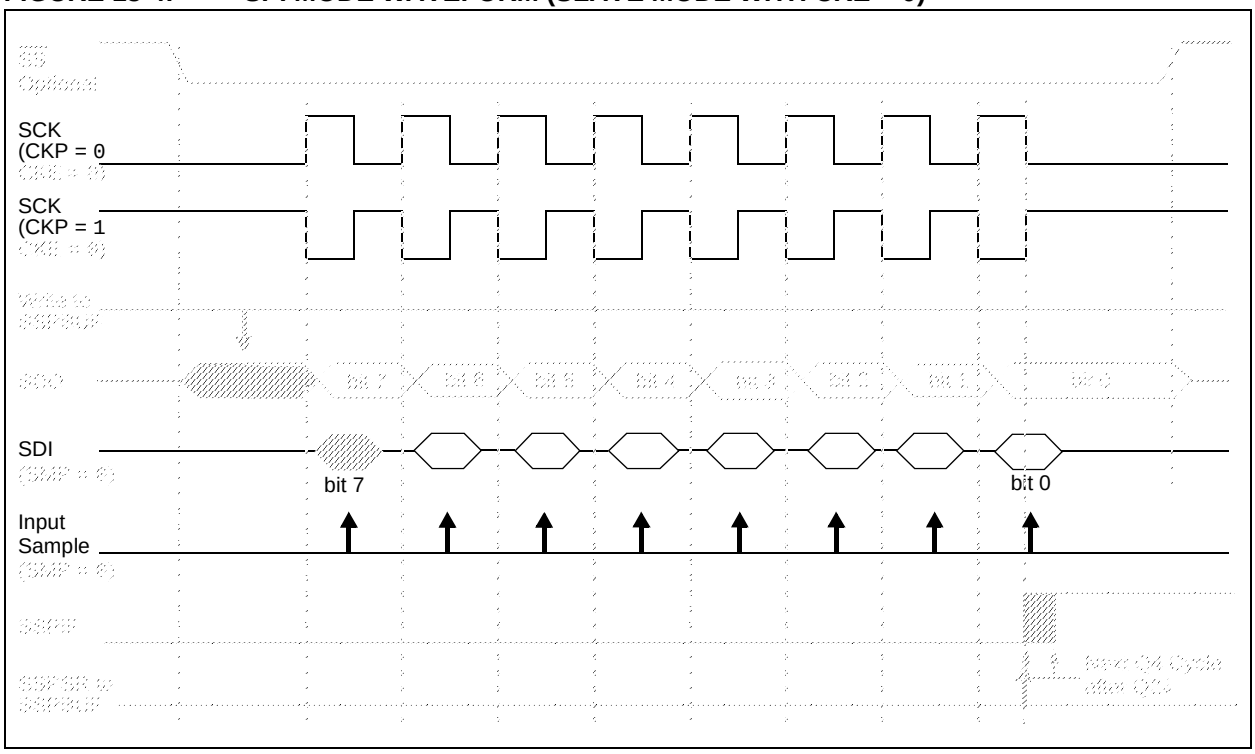
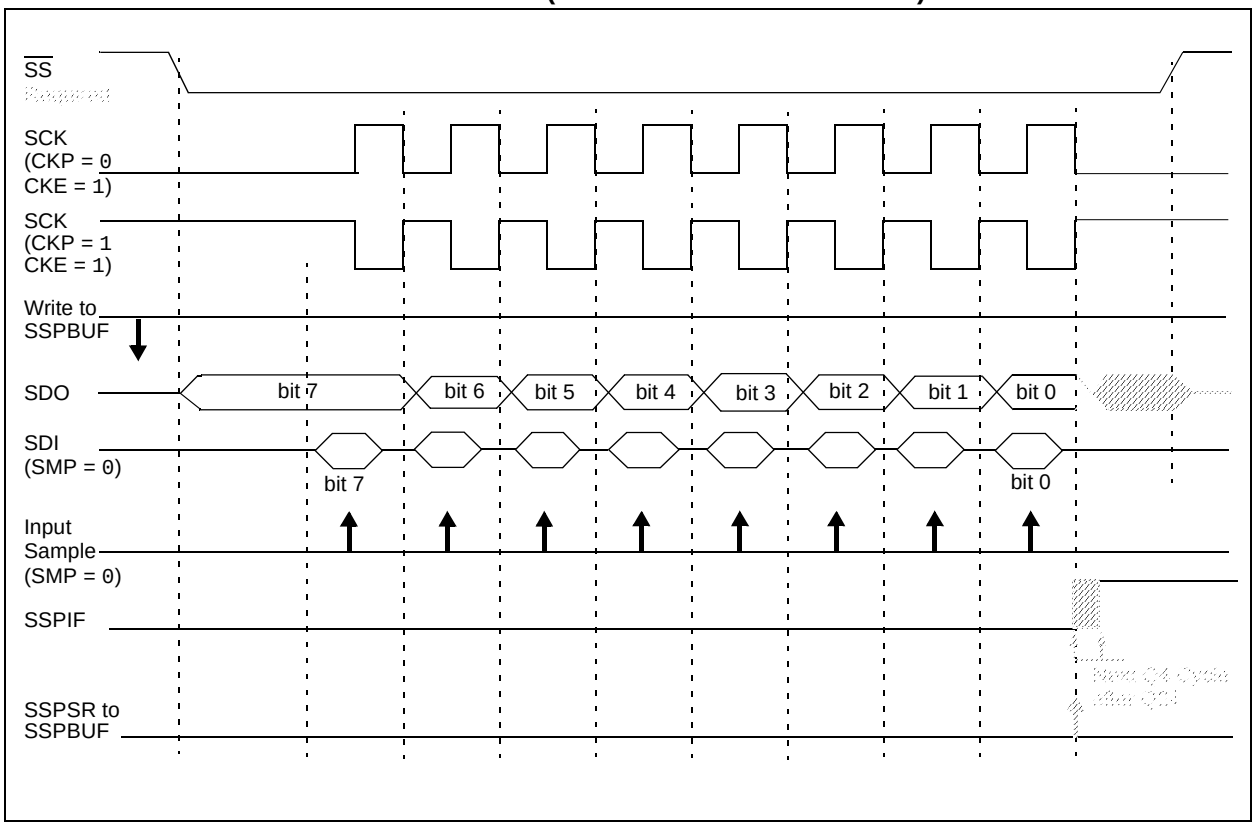


FIGURE 13-5: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)



13.4.16.3 Bus Collision During a Stop Condition

Bus collision occurs during a Stop condition if:

a) After the SDA pin has been de-asserted and allowed to float high, SDA is sampled low after the BRG has timed out.

b) After the SCL pin is de-asserted, SCL is sampled low before SDA goes high.

The Stop condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allowed to float. When the pin is sampled high (clock arbitration), the Baud Rate Generator is loaded with SSPADD<6:0> and counts down to 0. After the BRG times out, SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 13-26). If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 13-27).

FIGURE 13-26: BUS COLLISION DURING A STOP CONDITION (CASE 1)

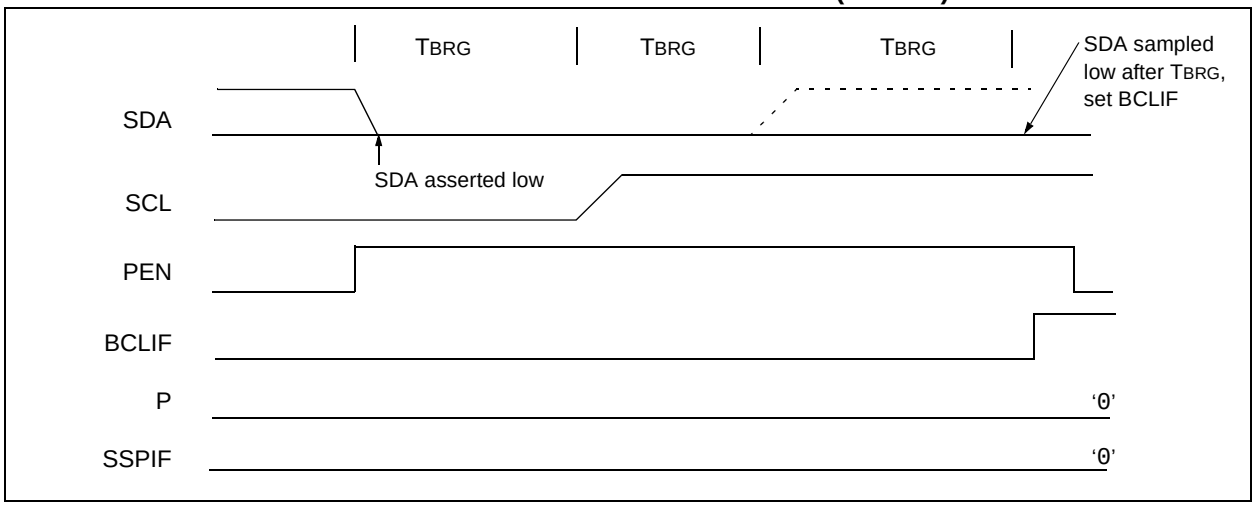
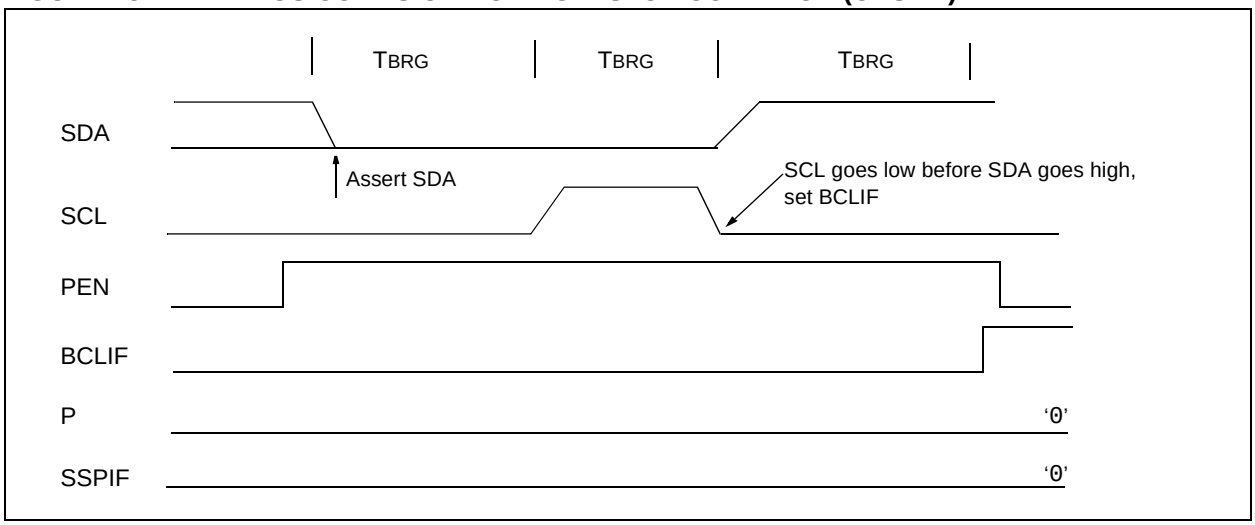


FIGURE 13-27: BUS COLLISION DURING A STOP CONDITION (CASE 2)



REGISTER 14-3: WDTCON: WATCHDOG TIMER CONTROL REGISTER

U-0	U-0	U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-1 **WDTPS<3:0>:** Watchdog Timer Period Select bits

Bit Value = Prescale Rate

0000 = 1:32
0001 = 1:64
0010 = 1:128
0011 = 1:256
0100 = 1:512 (Reset value)
0101 = 1:1024
0110 = 1:2048
0111 = 1:4096
1000 = 1:8192
1001 = 1:16384
1010 = 1:32768
1011 = 1:65536
1100 = reserved
1101 = reserved
1110 = reserved
1111 = reserved

bit 0 **SWDTEN:** Software Enable or Disable the Watchdog Timer(1)

1 = WDT is turned on
0 = WDT is turned off (Reset value)

Note 1: If WDTE Configuration bit = 1, then WDT is always enabled, irrespective of this control bit. If WDTE Configuration bit = 0, then it is possible to turn WDT on/off with this control bit.

TABLE 14-8: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OPTION_REG	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	31
WDTCON	—	—	—	WDTPS3	WDTPS2	WSTPS1	WDTPS0	SWDTEN	221

Legend: Shaded cells are not used by the Watchdog Timer.

TABLE 14-9: SUMMARY OF CONFIGURATION WORD ASSOCIATED WITH WATCHDOG TIMER

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1(1)	13:8	—	—	$\overline{\text{DEBUG}}$	LVP	FCMEN	IESO	BOREN 1	BOREN0	206
	7:0	$\overline{\text{CPD}}$	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC 2	FOSC 1	FOSC 0	

Legend: – = unimplemented locations read as '0'. Shaded cells are not used by the Watchdog Timer.

Note 1: See Configuration Word Register 1 (Register 14-1) for operation of all register bits.

17.1 DC Characteristics: PIC16F882/883/884/886/887-I (Industrial) PIC16F882/883/884/886/887-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
	VDD	**Supply Voltage**	2.0	—	5.5	V	FOSC < = 8 MHz: HFINTOSC, EC
D001			2.0	—	5.5	V	FOSC < = 4 MHz
D001C			3.0	—	5.5	V	FOSC < = 10 MHz
D001D			4.5	—	5.5	V	FOSC < = 20 MHz
D002*	VDR	**RAM Data Retention Voltage(1)**	1.5	—	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	VSS	—	V	See **Section 14.2.1 "Power-on Reset (POR)"** for details.
D004*	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See **Section 14.2.1 "Power-on Reset (POR)"** for details.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

17.7 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

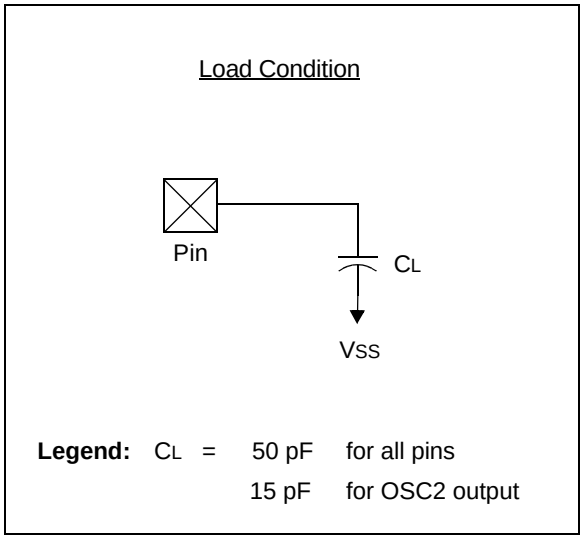
Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O PORT	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

FIGURE 17-3: LOAD CONDITIONS



Legend: C_L = 50 pF for all pins
15 pF for OSC2 output

FIGURE 17-14: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)

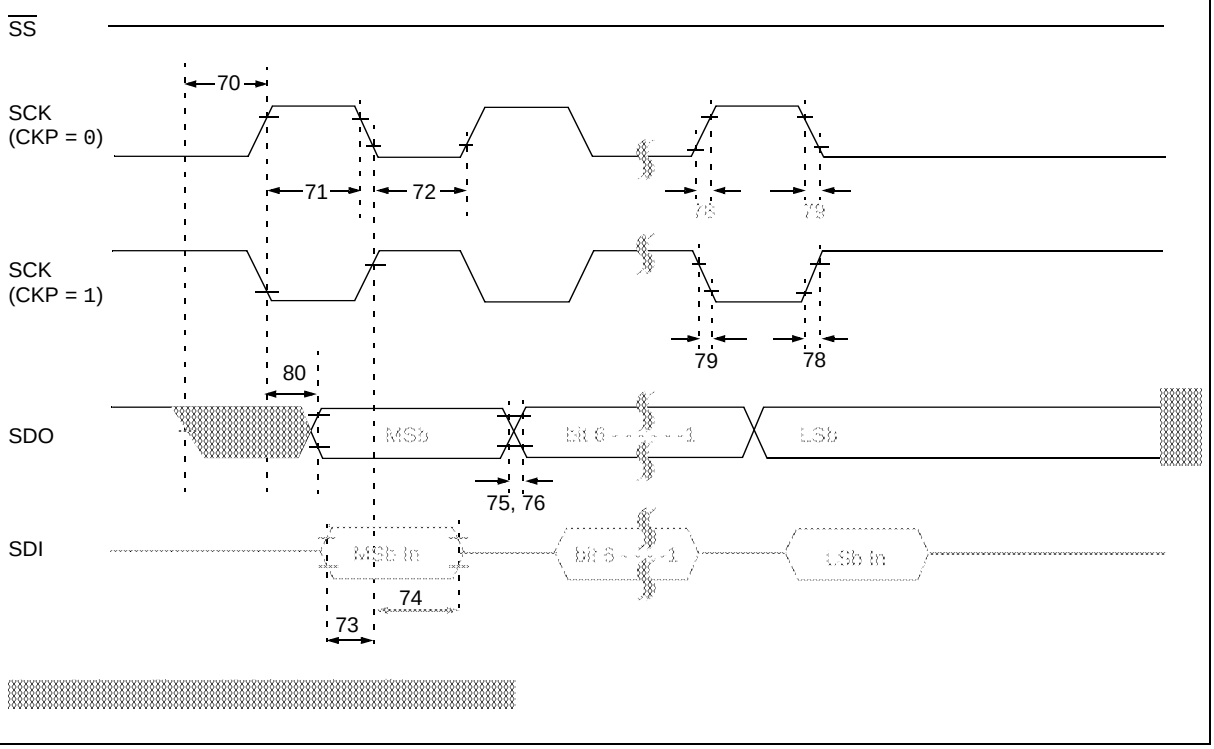
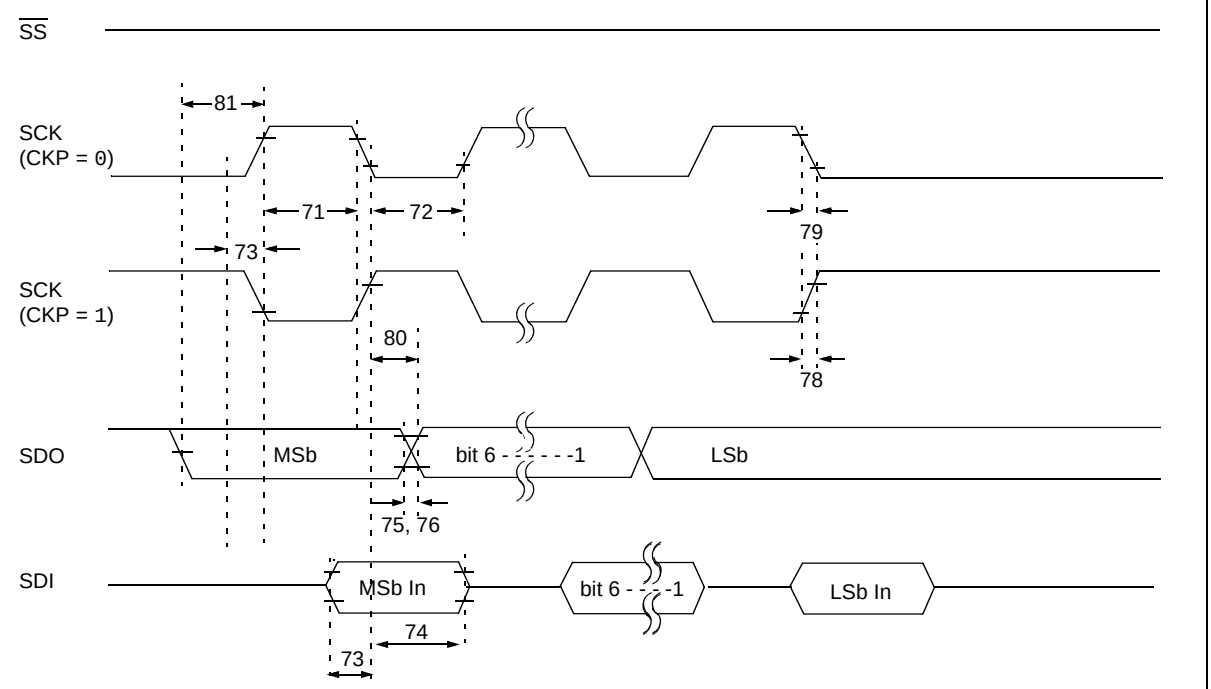


FIGURE 17-15: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)



Note: Refer to Figure 17-3 for load conditions.

FIGURE 18-3: TYPICAL IDD vs. FOSC OVER VDD (HS MODE)

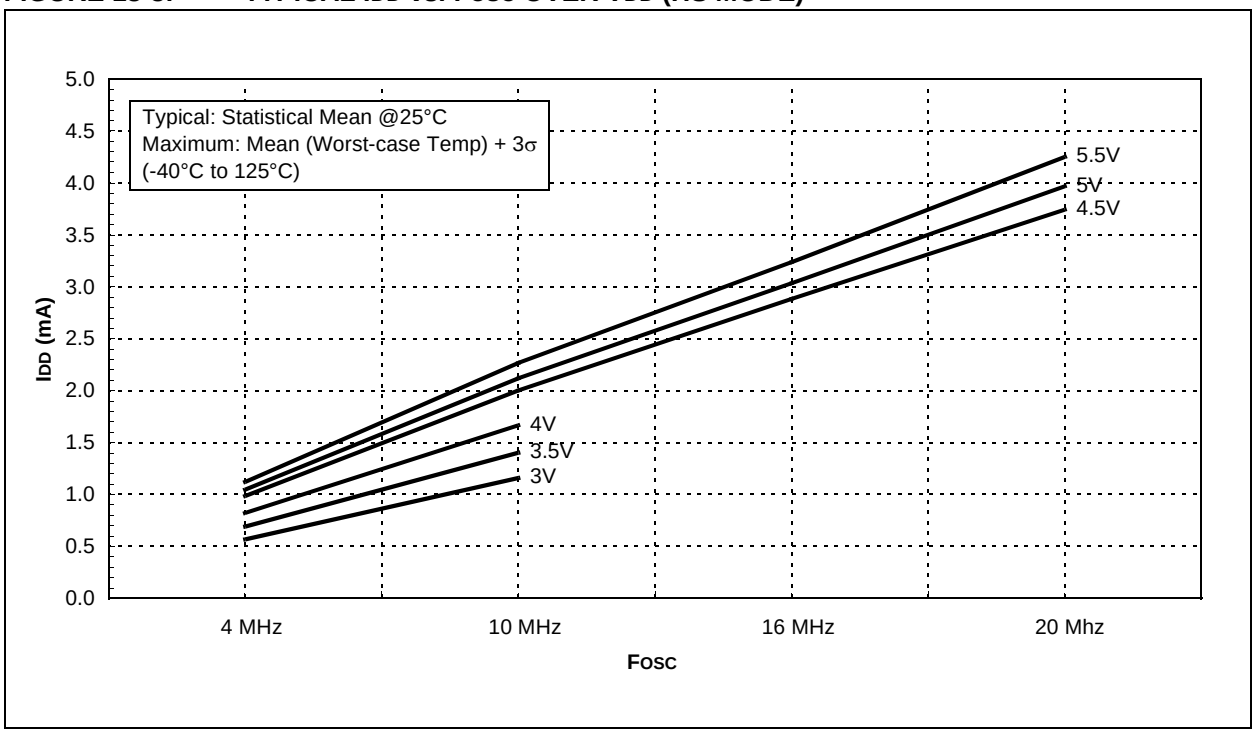
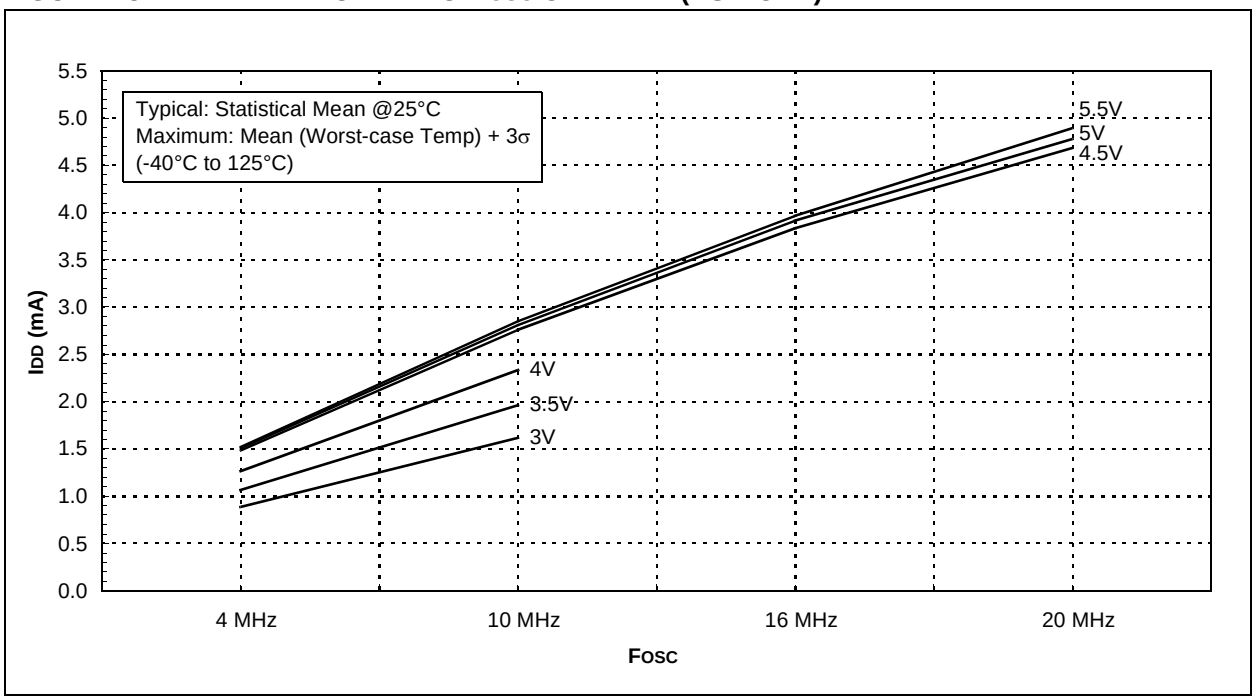
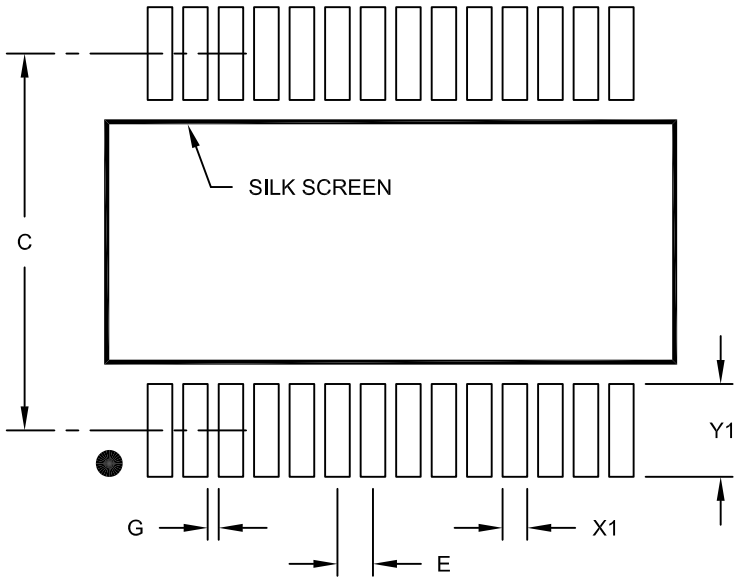


FIGURE 18-4: MAXIMUM IDD vs. FOSC OVER VDD (HS MODE)



28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

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