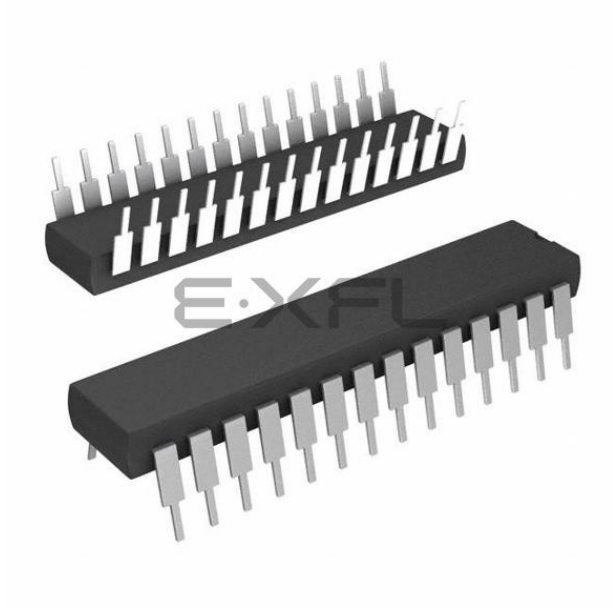

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 24 |
| Program Memory Size | 7KB (4K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | 256 x 8 |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V |
| Data Converters | A/D 11x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 28-DIP (0.300", 7.62mm) |
| Supplier Device Package | 28-SPDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16f883-e-sp |

**FIGURE 2-5: PIC16F883/PIC16F884 SPECIAL FUNCTION REGISTERS**

| | File Address | | File Address | | File Address | | File Address |
|---|---|---|---|---|---|---|---|
| Indirect addr. (1) | 00h | Indirect addr. (1) | 80h | Indirect addr. (1) | 100h | Indirect addr. (1) | 180h |
| TMR0 | 01h | OPTION_REG | 81h | TMR0 | 101h | OPTION_REG | 181h |
| PCL | 02h | PCL | 82h | PCL | 102h | PCL | 182h |
| STATUS | 03h | STATUS | 83h | STATUS | 103h | STATUS | 183h |
| FSR | 04h | FSR | 84h | FSR | 104h | FSR | 184h |
| PORTA | 05h | TRISA | 85h | WDTCON | 105h | SRCON | 185h |
| PORTB | 06h | TRISB | 86h | PORTB | 106h | TRISB | 186h |
| PORTC | 07h | TRISC | 87h | CM1CON0 | 107h | BAUDCTL | 187h |
| PORTD(2) | 08h | TRISD(2) | 88h | CM2CON0 | 108h | ANSEL | 188h |
| PORTE | 09h | TRISE | 89h | CM2CON1 | 109h | ANSELH | 189h |
| PCLATH | 0Ah | PCLATH | 8Ah | PCLATH | 10Ah | PCLATH | 18Ah |
| INTCON | 0Bh | INTCON | 8Bh | INTCON | 10Bh | INTCON | 18Bh |
| PIR1 | 0Ch | PIE1 | 8Ch | EEDAT | 10Ch | EECON1 | 18Ch |
| PIR2 | 0Dh | PIE2 | 8Dh | EEADR | 10Dh | EECON2(1) | 18Dh |
| TMR1L | 0Eh | PCON | 8Eh | EEDATH | 10Eh | Reserved | 18Eh |
| TMR1H | 0Fh | OSCCON | 8Fh | EEADRH | 10Fh | Reserved | 18Fh |
| T1CON | 10h | OSCTUNE | 90h | | 110h | | 190h |
| TMR2 | 11h | SSPCON2 | 91h | | 111h | | 191h |
| T2CON | 12h | PR2 | 92h | | 112h | | 192h |
| SSPBUF | 13h | SSPADD | 93h | | 113h | | 193h |
| SSPCON | 14h | SSPSTAT | 94h | | 114h | | 194h |
| CCPR1L | 15h | WPUB | 95h | | 115h | | 195h |
| CCPR1H | 16h | IOCB | 96h | | 116h | | 196h |
| CCP1CON | 17h | VRCON | 97h | | 117h | | 197h |
| RCSTA | 18h | TXSTA | 98h | | 118h | | 198h |
| TXREG | 19h | SPBRG | 99h | | 119h | | 199h |
| RCREG | 1Ah | SPBRGH | 9Ah | | 11Ah | | 19Ah |
| CCPR2L | 1Bh | PWM1CON | 9Bh | | 11Bh | | 19Bh |
| CCPR2H | 1Ch | ECCPAS | 9Ch | | 11Ch | | 19Ch |
| CCP2CON | 1Dh | PSTRCON | 9Dh | | 11Dh | | 19Dh |
| ADRESH | 1Eh | ADRESL | 9Eh | | 11Eh | | 19Eh |
| ADCON0 | 1Fh | ADCON1 | 9Fh | | 11Fh | | 19Fh |
| General Purpose Registers 96 Bytes | 20h – 7Fh | General Purpose Registers 80 Bytes | A0h – EFh | General Purpose Registers 80 Bytes | 120h – 16Fh | | 1A0h – 1EFh |
| | | accesses 70h-7Fh | F0h – FFh | accesses 70h-7Fh | 170h – 17Fh | accesses 70h-7Fh | 1F0h – 1FFh |
| Bank 0 | | Bank 1 | | Bank 2 | | Bank 3 | |

Unimplemented data memory locations, read as '0'.

**Note 1:** Not a physical register.

**2:** PIC16F884 only.

#### 2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- the Reset status
- the bank select bits for data memory (GPR and SFR)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS`, will clear the upper three bits and set the Z bit. This leaves the STATUS register as `'000u u1uu'` (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see **Section 15.0 "Instruction Set Summary"**

**Note 1:** The C and DC bits operate as a $\overline{Borrow}$ and $\overline{Digit\ Borrow}$ out bit, respectively, in subtraction.

## REGISTER DEFINITIONS: STATUS

**REGISTER 2-1: STATUS: STATUS REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R-1 | R-1 | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| IRP | RP1 | RP0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC(1) | C(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)
`1` = Bank 2, 3 (100h-1FFh)
`0` = Bank 0, 1 (00h-FFh)

bit 6-5 **RP<1:0>:** Register Bank Select bits (used for direct addressing)
`00` = Bank 0 (00h-7Fh)
`01` = Bank 1 (80h-FFh)
`10` = Bank 2 (100h-17Fh)
`11` = Bank 3 (180h-1FFh)

bit 4 **$\overline{TO}$:** Time-out bit
`1` = After power-up, `CLRWDT` instruction or `SLEEP` instruction
`0` = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
`1` = After power-up or by the `CLRWDT` instruction
`0` = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
`1` = A carry-out from the 4th low-order bit of the result occurred
`0` = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
`1` = A carry-out from the Most Significant bit of the result occurred
`0` = No carry-out from the Most Significant bit of the result occurred

**Note 1:** For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

### 3.2.3 PIN DESCRIPTIONS AND DIAGRAMS

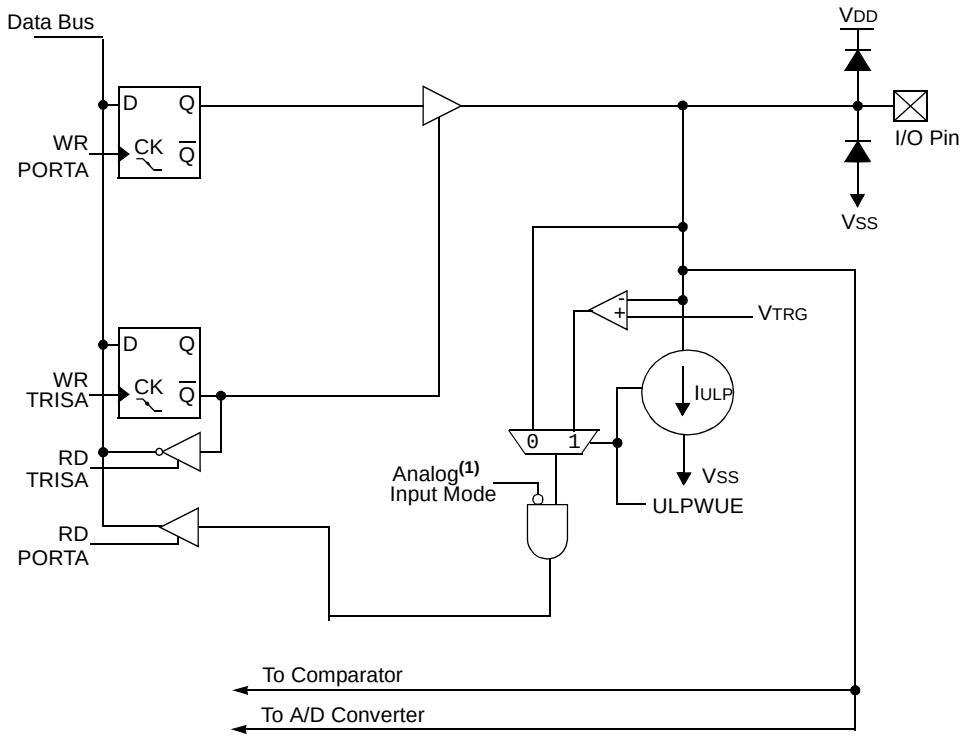
Each PORTA pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the comparator or the A/D Converter (ADC), refer to the appropriate section in this data sheet.

#### 3.2.3.1 RA0/AN0/ULPWU/C12IN0-

Figure 3-1 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a negative analog input to Comparator C1 or C2
- an analog input for the Ultra Low-Power Wake-up

**FIGURE 3-1: BLOCK DIAGRAM OF RA0**



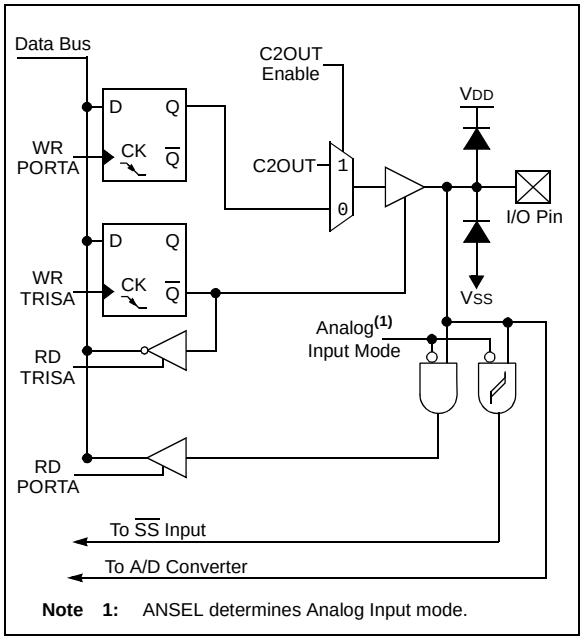

**Note 1:** ANSEL determines Analog Input mode.

### 3.2.3.6 RA5/AN4/$\overline{SS}$/C2OUT

Figure 3-6 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a slave select input
- a digital output from Comparator C2

**FIGURE 3-6: BLOCK DIAGRAM OF RA5**



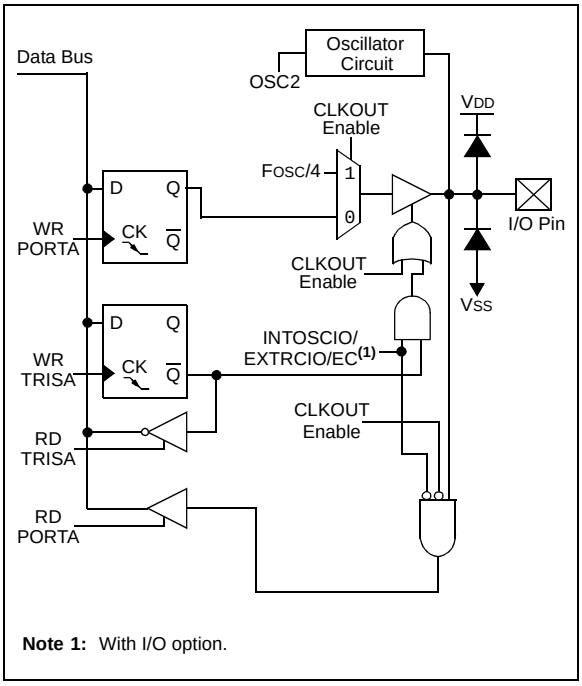

**Note 1:** ANSEL determines Analog Input mode.

### 3.2.3.7 RA6/OSC2/CLKOUT

Figure 3-7 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- a crystal/resonator connection
- a clock output

**FIGURE 3-7: BLOCK DIAGRAM OF RA6**




**Note 1:** With I/O option.

## 8.5 Operation During Sleep

The comparator, if enabled before entering Sleep mode, remains active during Sleep. The additional current consumed by the comparator is shown separately in the **Section 17.0 "Electrical Specifications"**. If the comparator is not used to wake the device, power consumption can be minimized while in Sleep mode by turning off the comparator. Each comparator is turned off by clearing the CxON bit of the CMxCON0 register.

A change to the comparator output can wake-up the device from Sleep. To enable the comparator to wake the device from Sleep, the CxIE bit of the PIE2 register and the PEIE bit of the INTCON register must be set. The instruction following the Sleep instruction always executes following a wake from Sleep. If the GIE bit of the INTCON register is also set, the device will then execute the Interrupt Service Routine.

## 8.6 Effects of a Reset

A device Reset forces the CMxCON0 and CM2CON1 registers to their Reset states. This forces both comparators and the voltage references to their Off states.

## REGISTER DEFINITIONS: COMPARATOR C1

**REGISTER 8-1: CM1CON0: COMPARATOR C1 CONTROL REGISTER 0**

| R/W-0 | R-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| C1ON | C1OUT | C1OE | C1POL | — | C1R | C1CH1 | C1CH0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **C1ON:** Comparator C1 Enable bit
1 = Comparator C1 is enabled
0 = Comparator C1 is disabled

bit 6 **C1OUT:** Comparator C1 Output bit
If C1POL = 1 (inverted polarity):
C1OUT = 0 when C1VIN+ > C1VIN-
C1OUT = 1 when C1VIN+ < C1VIN-
If C1POL = 0 (non-inverted polarity):
C1OUT = 1 when C1VIN+ > C1VIN-
C1OUT = 0 when C1VIN+ < C1VIN-

bit 5 **C1OE:** Comparator C1 Output Enable bit
1 = C1OUT is present on the C1OUT pin(1)
0 = C1OUT is internal only

bit 4 **C1POL:** Comparator C1 Output Polarity Select bit
1 = C1OUT logic is inverted
0 = C1OUT logic is not inverted

bit 3 **Unimplemented:** Read as '0'

bit 2 **C1R:** Comparator C1 Reference Select bit (non-inverting input)
1 = C1VIN+ connects to C1VREF output
0 = C1VIN+ connects to C1IN+ pin

bit 1-0 **C1CH<1:0>:** Comparator C1 Channel Select bit
00 = C12IN0- pin of C1 connects to C1VIN-
01 = C12IN1- pin of C1 connects to C1VIN-
10 = C12IN2- pin of C1 connects to C1VIN-
11 = C12IN3- pin of C1 connects to C1VIN-

**Note 1:** Comparator output requires the following three conditions: C1OE = 1, C1ON = 1 and corresponding port TRIS bit = 0.

**REGISTER 9-2: ADCON1: A/D CONTROL REGISTER 1**

| R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| ADFM | — | VCFG1 | VCFG0 | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **ADFM:** A/D Conversion Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **VCFG1:** Voltage Reference bit
1 = $V_{REF-}$ pin
0 = $V_{SS}$

bit 4 **VCFG0:** Voltage Reference bit
1 = $V_{REF+}$ pin
0 = $V_{DD}$

bit 3-0 **Unimplemented:** Read as ‘0’

An example of the complete 8-word write sequence is shown in Example 10-4. The initial address is loaded into the EEADRH and EEADR register pair; the eight words of data are loaded using indirect addressing.

**EXAMPLE 10-4: WRITING TO FLASH PROGRAM MEMORY**

```
        ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
        ; This write routine assumes the following:
        ;     A valid starting address (the least significant bits = '000')
        ;     is loaded in ADDRH:ADDRL
        ;     ADDRH, ADDRL and DATADDR are all located in data memory
        ;
        BANKSEL  EEADRH
        MOVF     ADDRH,W      ; Load initial address
        MOVWF    EEADRH       ;
        MOVF     ADDRL,W      ;
        MOVWF    EEADR        ;
        MOVF     DATAADDR,W   ; Load initial data address
        MOVWF    FSR          ;
LOOP    MOVF     INDF,W       ; Load first data byte into lower
        MOVWF    EEDATA       ;
        INCF     FSR,F        ; Next byte
        MOVF     INDF,W       ; Load second data byte into upper
        MOVWF    EEDATH       ;
        INCF     FSR,F        ;
        BANKSEL  EECON1
        BSF      EECON1,EEPGD ; Point to program memory
        BSF      EECON1,WREN  ; Enable writes
        BCF      INTCON,GIE   ; Disable interrupts (if using)
        BTFSC    INTCON,GIE   ; See AN576
        GOTO     $-2
        ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
        ;                         Required Sequence
        MOVLW    55h          ; Start of required write sequence:
        MOVWF    EECON2       ; Write 55h
        MOVLW    0AAh         ;
        MOVWF    EECON2       ; Write 0AAh
        BSF      EECON1,WR    ; Set WR bit to begin write
        NOP                   ; Required to transfer data to the buffer
        NOP                   ; registers
        ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
        BCF      EECON1,WREN  ; Disable writes
        BSF      INTCON,GIE   ; Enable interrupts (comment out if not using interrupts)
        BANKSEL  EEADR
        MOVF     EEADR, W
        INCF     EEADR,F      ; Increment address
        ANDLW    0x0F         ; Indicates when sixteen words have been programmed
        SUBLW    0x0F         ;   0x0F = 16 words
                              ;   0x0B = 12 words (PIC16F884/883/882 only)
                              ;   0x07 = 8 words
                              ;   0x03 = 4 words(PIC16F884/883/882 only)
        BTFSS    STATUS,Z     ; Exit on a match,
        GOTO     LOOP         ; Continue if more data needs to be written
```

### 11.6.7 PULSE STEERING MODE

In Single Output mode, pulse steering allows any of the PWM pins to be the modulated signal. Additionally, the same PWM signal can be simultaneously available on multiple pins.

Once the Single Output mode is selected (CCP1M<3:2> = 11 and P1M<1:0> = 00 of the CCP1CON register), the user firmware can bring out the same PWM signal to one, two, three or four output pins by setting the appropriate STR<D:A> bits of the PSTRCON register, as shown in Table 11-5.

| **Note:** | The associated TRIS bits must be set to output ('0') to enable the pin output driver in order to see the PWM signal on the pin. |
|---|---|

While the PWM Steering mode is active, CCP1M<1:0> bits of the CCP1CON register select the PWM output polarity for the P1<D:A> pins.

The PWM auto-shutdown operation also applies to PWM Steering mode as described in **Section 11.6.4 "Enhanced PWM Auto-Shutdown Mode"**. An auto-shutdown event will only affect pins that have PWM outputs enabled.

## REGISTER DEFINITIONS: PULSE STEERING CONTROL

**REGISTER 11-5: PSTRCON: PULSE STEERING CONTROL REGISTER(1)**

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | STRSYNC | STRD | STRC | STRB | STRA |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **STRSYNC:** Steering Sync bit
1 = Output steering update occurs on next PWM period
0 = Output steering update occurs at the beginning of the instruction cycle boundary

bit 3 **STRD:** Steering Enable bit D
1 = P1D pin has the PWM waveform with polarity control from CCPxM<1:0>
0 = P1D pin is assigned to port pin

bit 2 **STRC:** Steering Enable bit C
1 = P1C pin has the PWM waveform with polarity control from CCPxM<1:0>
0 = P1C pin is assigned to port pin

bit 1 **STRB:** Steering Enable bit B
1 = P1B pin has the PWM waveform with polarity control from CCPxM<1:0>
0 = P1B pin is assigned to port pin

bit 0 **STRA:** Steering Enable bit A
1 = P1A pin has the PWM waveform with polarity control from CCPxM<1:0>
0 = P1A pin is assigned to port pin

**Note 1:** The PWM Steering mode is available only when the CCP1CON register bits CCP1M<3:2> = 11 and P1M<1:0> = 00.

## 12.0 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer independent of device program execution. The EUSART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system or half-duplex synchronous system. Full-Duplex mode is useful for communications with peripheral systems, such as CRT terminals and personal computers. Half-Duplex Synchronous mode is intended for communications with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs or other microcontrollers. These devices typically do not have internal clocks for baud rate generation and require the external clock signal provided by a master synchronous device.

The EUSART module includes the following capabilities:

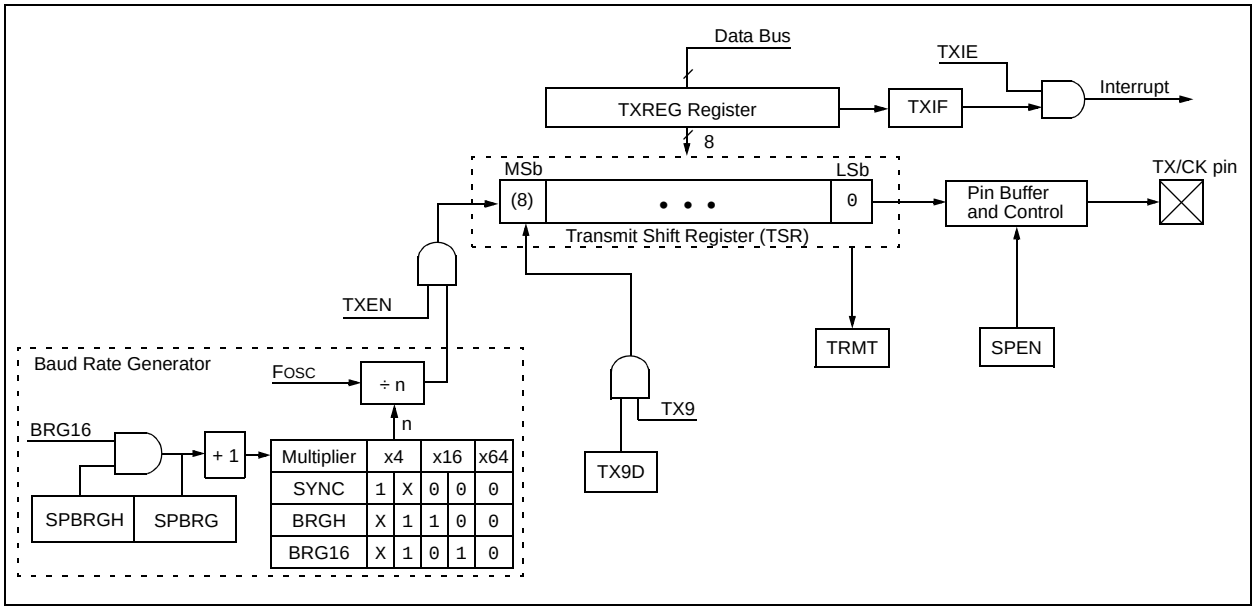
- Full-duplex asynchronous transmit and receive
- Two-character input buffer
- One-character output buffer
- Programmable 8-bit or 9-bit character length
- Address detection in 9-bit mode
- Input buffer overrun error detection
- Received character framing error detection
- Half-duplex synchronous master
- Half-duplex synchronous slave
- Programmable clock polarity in synchronous modes
- Sleep operation

The EUSART module implements the following additional features, making it ideally suited for use in Local Interconnect Network (LIN) bus systems:

- Automatic detection and calibration of the baud rate
- Wake-up on Break reception
- 13-bit Break character transmit

Block diagrams of the EUSART transmitter and receiver are shown in Figure 12-1 and Figure 12-2.

**FIGURE 12-1: EUSART TRANSMIT BLOCK DIAGRAM**



## 12.1 EUSART Asynchronous Mode

The EUSART transmits and receives data using the standard non-return-to-zero (NRZ) format. NRZ is implemented with two levels: a VOH mark state which represents a '1' data bit, and a VOL space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the mark state. Each character transmission consists of one Start bit followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is eight bits. Each transmitted bit persists for a period of 1/(Baud Rate). An on-chip dedicated 8-bit/16-bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. See Table 12-5 for examples of baud rate configurations.

The EUSART transmits and receives the LSb first. The EUSART's transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is not supported by the hardware, but can be implemented in software and stored as the ninth data bit.

### 12.1.1 EUSART ASYNCHRONOUS TRANSMITTER

The EUSART transmitter block diagram is shown in Figure 12-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the TXREG register.

#### 12.1.1.1 Enabling the Transmitter

The EUSART transmitter is enabled for asynchronous operations by configuring the following three control bits:

- TXEN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the TXEN bit of the TXSTA register enables the transmitter circuitry of the EUSART. Clearing the SYNC bit of the TXSTA register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the EUSART and automatically configures the TX/CK I/O pin as an output. If the TX/CK pin is shared with an analog peripheral the analog I/O function must be disabled by clearing the corresponding ANSEL bit.

**Note 1:** When the SPEN bit is set the RX/DT I/O pin is automatically configured as an input, regardless of the state of the corresponding TRIS bit and whether or not the EUSART receiver is enabled. The RX/DT pin data can be read via a normal PORT read but PORT latch data output is precluded.

**2:** The TXIF transmitter interrupt flag is set when the TXEN enable bit is set.

#### 12.1.1.2 Transmitting Data

A transmission is initiated by writing a character to the TXREG register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TXREG until the Stop bit of the previous character has been transmitted. The pending character in the TXREG is then transferred to the TSR in one TCY immediately following the Stop bit transmission. The transmission of the Start bit, data bits and Stop bit sequence commences immediately following the transfer of the data to the TSR from the TXREG.

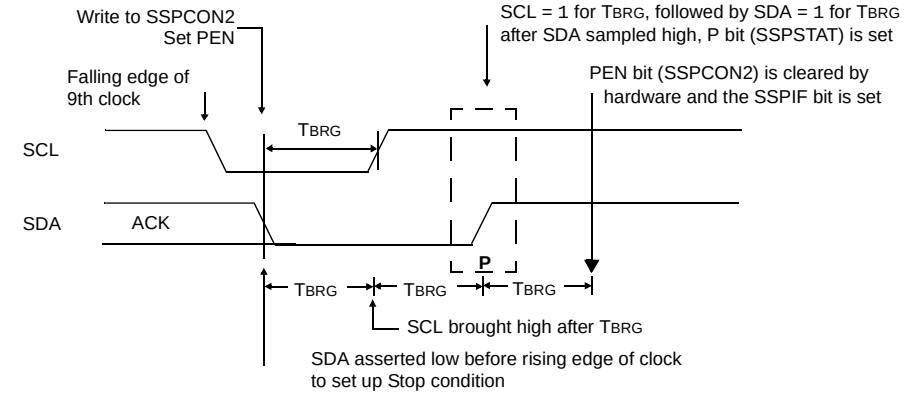
#### 12.1.1.3 Transmit Interrupt Flag

The TXIF interrupt flag bit of the PIR1 register is set whenever the EUSART transmitter is enabled and no character is being held for transmission in the TXREG. In other words, the TXIF bit is only clear when the TSR is busy with a character and a new character has been queued for transmission in the TXREG. The TXIF flag bit is not cleared immediately upon writing TXREG. TXIF becomes valid in the second instruction cycle following the write execution. Polling TXIF immediately following the TXREG write will return invalid results. The TXIF bit is read-only, it cannot be set or cleared by software.

The TXIF interrupt can be enabled by setting the TXIE interrupt enable bit of the PIE1 register. However, the TXIF flag bit will be set whenever the TXREG is empty, regardless of the state of TXIE enable bit.

To use interrupts when transmitting data, set the TXIE bit only when there is more data to send. Clear the TXIE interrupt enable bit upon writing the last character of the transmission to the TXREG.

**FIGURE 13-18: STOP CONDITION RECEIVE OR TRANSMIT MODE**




**Note:** TBRG = one Baud Rate Generator period.

### 13.4.12 CLOCK ARBITRATION

Clock arbitration occurs when the master, during any receive, transmit or Repeated Start/Stop condition, de-asserts the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the Baud Rate Generator (BRG) is suspended from counting until the SCL pin is actually sampled high. When the SCL pin is sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<6:0> and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count, in the event that the clock is held low by an external device (Figure 13-19).

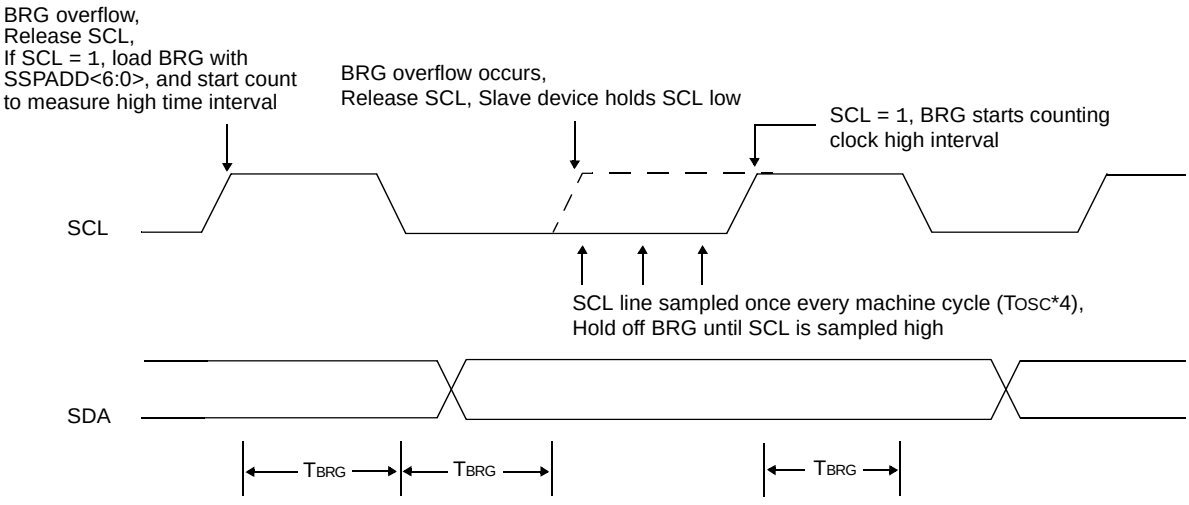
### 13.4.13 SLEEP OPERATION

While in Sleep mode, the $I^2C$ module can receive addresses or data, and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSP interrupt is enabled).

### 13.4.14 EFFECT OF A RESET

A Reset disables the MSSP module and terminates the current transfer.

**FIGURE 13-19: CLOCK ARBITRATION TIMING IN MASTER TRANSMIT MODE**



### 13.4.17 SSP MASK REGISTER

An SSP Mask (SSPMSK) register is available in $I^2C$ Slave mode as a mask for the value held in the SSPSR register during an address comparison operation. A zero (‘0’) bit in the SSPMSK register has the effect of making the corresponding bit in the SSPSR register a “don’t care”.

This register is reset to all ‘1’s upon any Reset condition and, therefore, has no effect on standard SSP operation until written with a mask value.

This register must be initiated prior to setting SSPM<3:0> bits to select the $I^2C$ Slave mode (7-bit or 10-bit address).

This register can only be accessed when the appropriate mode is selected by bits (SSPM<3:0> of SSPCON).

The SSP Mask register is active during:

- 7-bit Address mode: address compare of A<7:1>.
- 10-bit Address mode: address compare of A<7:0> only. The SSP mask has no effect during the reception of the first (high) byte of the address.

**REGISTER 13-4: SSPMSK: SSP MASK REGISTER(1)**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| MSK7 | MSK6 | MSK5 | MSK4 | MSK3 | MSK2 | MSK1 | MSK0(2) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-1 **MSK<7:1>:** Mask bits
1 = The received address bit n is compared to SSPADD<n> to detect $I^2C$ address match
0 = The received address bit n is not used to detect $I^2C$ address match

bit 0 **MSK<0>:** Mask bit for $I^2C$ Slave mode, 10-bit Address(2)
$I^2C$ Slave mode, 10-bit Address (SSPM<3:0> = 0111):
1 = The received address bit 0 is compared to SSPADD<0> to detect $I^2C$ address match
0 = The received address bit 0 is not used to detect $I^2C$ address match

**Note 1:** When SSPCON bits SSPM<3:0> = 1001, any reads or writes to the SSPADD SFR address are accessed through the SSPMSK register.

**2:** In all other SSP modes, this bit has no effect.

### 14.2.5 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows: first, PWRT time-out is invoked after POR has expired, then OST is activated after the PWRT time-out has expired. The total time-out will vary based on oscillator configuration and $\overline{\text{PWRTE}}$ bit status. For example, in EC mode with $\overline{\text{PWRTE}}$ bit erased (PWRT disabled), there will be no time-out at all. Figures 14-4, 14-5 and 14-6 depict time-out sequences. The device can execute code from the INTOSC while OST is active by enabling Two-Speed Start-up or Fail-Safe Monitor (see **Section 4.7.2 "Two-Speed Start-up Sequence"** and **Section 4.8 "Fail-Safe Clock Monitor"**).

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then, bringing $\overline{\text{MCLR}}$ high will begin execution immediately (see Figure 14-5). This is useful for testing purposes or to synchronize more than one PIC16F882/883/884/886/887 device operating in parallel.

Table 14-5 shows the Reset conditions for some special registers, while Table 14-4 shows the Reset conditions for all the registers.

### 14.2.6 POWER CONTROL (PCON) REGISTER

The Power Control register PCON (address 8Eh) has two Status bits to indicate what type of Reset that last occurred.

Bit 0 is $\overline{\text{BOR}}$ (Brown-out Reset). $\overline{\text{BOR}}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if $\overline{\text{BOR}}$ = 0, indicating that a brown-out has occurred. The $\overline{\text{BOR}}$ Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (BOREN<1:0> = 00 in the Configuration Word Register 1).

Bit 1 is $\overline{\text{POR}}$ (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent Reset, if $\overline{\text{POR}}$ is '0', it will indicate that a Power-on Reset has occurred (i.e., $V_{DD}$ may have gone too low).

For more information, see **Section 3.2.2 "Ultra Low-Power Wake-up"** and **Section 14.2.4 "Brown-out Reset (BOR)"**.

**TABLE 14-1: TIME-OUT IN VARIOUS SITUATIONS**

| Oscillator Configuration | Power-up | | Brown-out Reset | | Wake-up from Sleep |
|---|---|---|---|---|---|
| | $\overline{\text{PWRTE}}$ = 0 | $\overline{\text{PWRTE}}$ = 1 | $\overline{\text{PWRTE}}$ = 0 | $\overline{\text{PWRTE}}$ = 1 | |
| XT, HS, LP | $T_{PWRT}$ + 1024 • $T_{OSC}$ | 1024 • $T_{OSC}$ | $T_{PWRT}$ + 1024 • $T_{OSC}$ | 1024 • $T_{OSC}$ | 1024 • $T_{OSC}$ |
| LP, T1OSCIN = 1 | $T_{PWRT}$ | — | $T_{PWRT}$ | — | — |
| RC, EC, INTOSC | $T_{PWRT}$ | — | $T_{PWRT}$ | — | — |

**TABLE 14-2: STATUS/PCON BITS AND THEIR SIGNIFICANCE**

| POR | BOR | $\overline{\text{TO}}$ | $\overline{\text{PD}}$ | Condition |
|---|---|---|---|---|
| 0 | x | 1 | 1 | Power-on Reset |
| u | 0 | 1 | 1 | Brown-out Reset |
| u | u | 0 | u | WDT Reset |
| u | u | 0 | 0 | WDT Wake-up |
| u | u | u | u | $\overline{\text{MCLR}}$ Reset during normal operation |
| u | u | 1 | 0 | $\overline{\text{MCLR}}$ Reset during Sleep |

**Legend:** u = unchanged, x = unknown

**TABLE 14-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|
| PCON | — | — | ULPWUE | SBOREN | — | — | $\overline{\text{POR}}$ | $\overline{\text{BOR}}$ | 37 |
| STATUS | IRP | RP1 | RPO | $\overline{\text{TO}}$ | $\overline{\text{PD}}$ | Z | DC | C | 30 |

**Legend:** u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition. Shaded cells are not used by BOR.

**Note 1:** Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.

## 15.0 INSTRUCTION SET SUMMARY

The PIC16F882/883/884/886/887 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 14-bit word divided into an **opcode,** which specifies the instruction type and one or more **operands,** which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 15-1, while the various opcode fields are summarized in Table 15-1.

Table 15-2 lists the instructions recognized by the MPASM™ assembler.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1 μs. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

### 15.1 Read-Modify-Write Operations

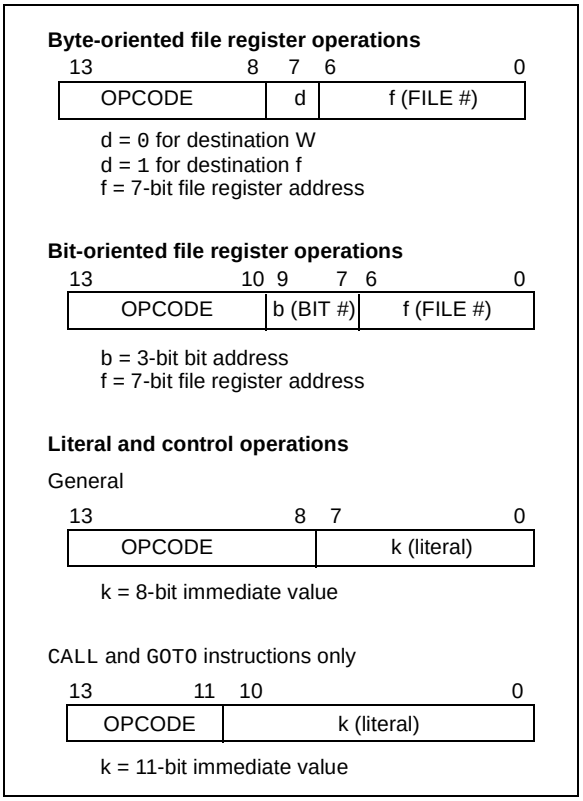
Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (RMW) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

For example, a CLRF PORTA instruction will read PORTA, clear all the data bits, then write the result back to PORTA. This example would have the unintended consequence of clearing the condition that set the RAIF flag.

**TABLE 15-1: OPCODE FIELD DESCRIPTIONS**

| Field | Description |
|---|---|
| f | Register file address (0x00 to 0x7F) |
| W | Working register (accumulator) |
| b | Bit address within an 8-bit file register |
| k | Literal field, constant data or label |
| x | Don't care location (= 0 or 1).<br>The assembler will generate code with x = 0.<br>It is the recommended form of use for compatibility with all Microchip software tools. |
| d | Destination select; d = 0: store result in W,<br>d = 1: store result in file register f.<br>Default is d = 1. |
| PC | Program Counter |
| $\overline{TO}$ | Time-out bit |
| C | Carry bit |
| DC | Digit carry bit |
| Z | Zero bit |
| $\overline{PD}$ | Power-down bit |

**FIGURE 15-1: GENERAL FORMAT FOR INSTRUCTIONS**



## 17.1 DC Characteristics: PIC16F882/883/884/886/887-I (Industrial) PIC16F882/883/884/886/887-E (Extended)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial<br>-40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| | VDD | **Supply Voltage** | 2.0 | — | 5.5 | V | FOSC < = 8 MHz: HFINTOSC, EC |
| D001 | | | 2.0 | — | 5.5 | V | FOSC < = 4 MHz |
| D001C | | | 3.0 | — | 5.5 | V | FOSC < = 10 MHz |
| D001D | | | 4.5 | — | 5.5 | V | FOSC < = 20 MHz |
| D002* | VDR | **RAM Data Retention Voltage(1)** | 1.5 | — | — | V | Device in Sleep mode |
| D003 | VPOR | **VDD Start Voltage** to ensure internal Power-on Reset signal | — | VSS | — | V | See **Section 14.2.1 "Power-on Reset (POR)"** for details. |
| D004* | SVDD | **VDD Rise Rate** to ensure internal Power-on Reset signal | 0.05 | — | — | V/ms | See **Section 14.2.1 "Power-on Reset (POR)"** for details. |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

## 17.5 DC Characteristics: PIC16F882/883/884/886/887-I (Industrial) PIC16F882/883/884/886/887-E (Extended) (Continued)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial<br>-40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| D100 | IULP | Ultra Low-Power Wake-Up Current | — | 200 | — | nA | See Application Note AN879, "*Using the Microchip Ultra Low-Power Wake-up Module*" (DS00879) |
| | | **Capacitive Loading Specs on Output Pins** | | | | | |
| D101* | COSC2 | OSC2 pin | — | — | 15 | pF | In XT, HS and LP modes when external clock is used to drive OSC1 |
| D101A* | CIO | All I/O pins | — | — | 50 | pF | |
| | | **Data EEPROM Memory** | | | | | |
| D120 | ED | Byte Endurance | 100K | 1M | — | E/W | -40°C ≤ TA ≤ +85°C |
| D120A | ED | Byte Endurance | 10K | 100K | — | E/W | +85°C ≤ TA ≤ +125°C |
| D121 | VDRW | VDD for Read/Write | VMIN | — | 5.5 | V | Using EECON1 to read/write VMIN = Minimum operating voltage |
| D122 | TDEW | Erase/Write Cycle Time | — | 5 | 6 | ms | |
| D123 | TRETD | Characteristic Retention | 40 | — | — | Year | Provided no other specifications are violated |
| D124 | TREF | Number of Total Erase/Write Cycles before Refresh(4) | 1M | 10M | — | E/W | -40°C ≤ TA ≤ +85°C |
| | | **Program Flash Memory** | | | | | |
| D130 | EP | Cell Endurance | 10K | 100K | — | E/W | -40°C ≤ TA ≤ +85°C |
| D130A | ED | Cell Endurance | 1K | 10K | — | E/W | +85°C ≤ TA ≤ +125°C |
| D131 | VPR | VDD for Read | VMIN | — | 5.5 | V | VMIN = Minimum operating voltage |
| D132 | VPEW | VDD for Row Erase/Write | VMIN | — | 5.5 | V | |
| | | VDD for Bulk Erase Operations | 4.5 | — | 5.5 | V | |
| D133 | TPEW | Erase/Write cycle time | — | 2 | 2.5 | ms | |
| D134 | TRETD | Characteristic Retention | 40 | — | — | Year | Provided no other specifications are violated |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

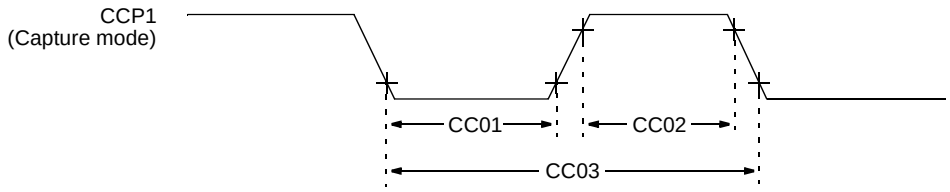
**2:** Negative current is defined as current sourced by the pin.

**3:** The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**4:** See **Section 10.3.1 "Using the Data EEPROM"** for additional information.

**5:** Including OSC2 in CLKOUT mode.

**FIGURE 17-9: CAPTURE/COMPARE/PWM TIMINGS (ECCP)**




**Note:** Refer to Figure 17-3 for load conditions.

**TABLE 17-6: CAPTURE/COMPARE/PWM REQUIREMENTS (ECCP)**

| **Standard Operating Conditions (unless otherwise stated)**<br>Operating Temperature -40°C ≤ TA ≤ +125°C | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| CC01* | TccL | CCP1 Input Low Time | No Prescaler | 0.5TCY + 20 | — | — | ns | |
| | | | With Prescaler | 20 | — | — | ns | |
| CC02* | TccH | CCP1 Input High Time | No Prescaler | 0.5TCY + 20 | — | — | ns | |
| | | | With Prescaler | 20 | — | — | ns | |
| CC03* | TccP | CCP1 Input Period | | $\frac{3T_{CY} + 40}{N}$ | — | — | ns | N = prescale value (1, 4 or 16) |

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**TABLE 17-19: DC CHARACTERISTICS FOR IDD SPECIFICATIONS FOR PIC16F886/7-H (High Temp.)**

| Param No. | Device Characteristics | Min. | Typ. | Max. | Units | Condition | |
|---|---|---|---|---|---|---|---|
| | | | | | | VDD | Note |
| D001 | VDD | 2.1 | — | 5.5 | V | — | FOSC ≤ 8 MHz: HFINTOSC, EC |
| | | 2.1 | — | 5.5 | V | — | FOSC ≤ 4 MHz |

**TABLE 17-20: DC CHARACTERISTICS FOR IPD SPECIFICATIONS FOR PIC16F886/7-H (High Temp.)**

| Param No. | Device Characteristics | Units | Min. | Typ. | Max. | Condition | |
|---|---|---|---|---|---|---|---|
| | | | | | | VDD | Note |
| D020E | Power Down Base Current (IPD) | — | — | 27 | μA | 2.1 | IPD Base: WDT, BOR, Comparators, VREF and T1OSC disabled |
| | | — | — | 29 | | 3.0 | |
| | | — | — | 32 | | 5.0 | |
| D021E | | — | — | 55 | μA | 2.1 | WDT Current |
| | | — | — | 59 | | 3.0 | |
| | | — | — | 69 | | 5.0 | |
| D022E | | — | — | 75 | μA | 3.0 | BOR Current |
| | | — | — | 147 | | 5.0 | |
| D023E | | — | — | 73 | μA | 2.1 | Comparator current, both comparators enabled |
| | | — | — | 117 | | 3.0 | |
| | | — | — | 235 | | 5.0 | |
| D024E | | — | — | 102 | μA | 2.1 | CVREF current, high range |
| | | — | — | 128 | | 3.0 | |
| | | — | — | 170 | | 5.0 | |
| D024AE | | — | — | 133 | μA | 2.1 | CVREF current, low range |
| | | — | — | 167 | | 3.0 | |
| | | — | — | 222 | | 5.0 | |
| D025E | | — | — | 36 | μA | 2.1 | T1OSC current, 32 kHz |
| | | — | — | 41 | | 3.0 | |
| | | — | — | 47 | | 5.0 | |
| D026E | | — | — | 22 | μA | 3.0 | Analog-to-Digital current, no conversion in progress |
| | | — | — | 24 | | 5.0 | |
| D027E | | — | — | 189 | μA | 3.0 | VP6 current (Fixed Voltage Reference) |
| | | — | — | 250 | | 5.0 | |

**TABLE 17-21: LEAKAGE CURRENT SPECIFICATIONS FOR PIC16F886/7-H (High Temp.)**

| Param No. | Sym. | Characteristic | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| D061 | IIL | Input Leakage Current(1) (RA3/MCLR) | — | ±0.5 | ±5.0 | μA | VSS ≤ VPIN ≤ VDD |
| D062 | IIL | Input Leakage Current(2) (RA3/MCLR) | 50 | 250 | 400 | μA | VDD = 5.0V |

**Note 1:** This specification applies when RA3/$\overline{\text{MCLR}}$ is configured as an input with the pull-up disabled. The leakage current for the RA3/$\overline{\text{MCLR}}$ pin is higher than for the standard I/O port pins.

**2:** This specification applies when RA3/$\overline{\text{MCLR}}$ is configured as the $\overline{\text{MCLR}}$ reset pin function with the weak pull-up enabled.

## 18.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

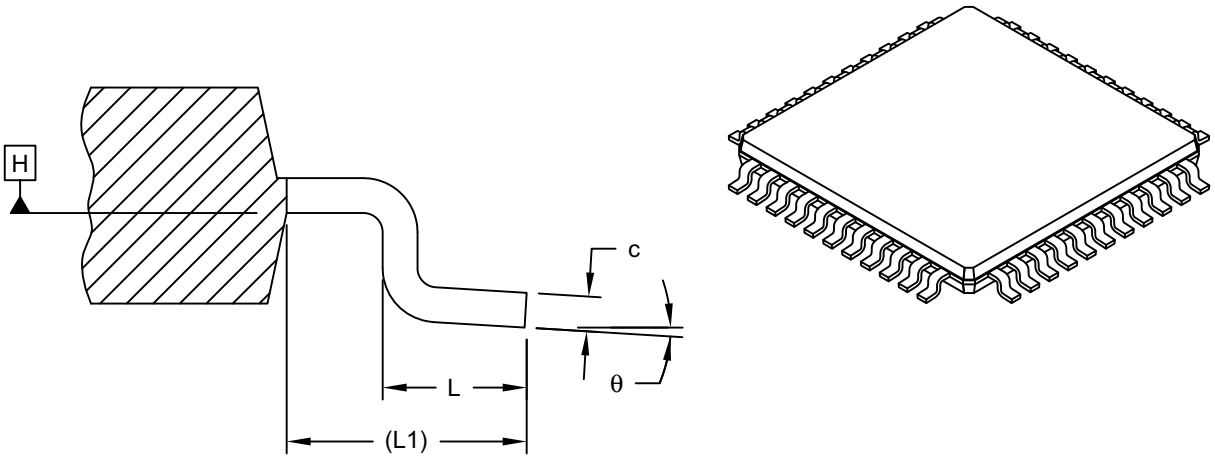
In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified $V_{DD}$ range). This is for **information only** and devices are ensured to operate properly only within the specified range.

| | |
|---|---|
| **Note:** | The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range. |

**"Typical" represents the mean of the distribution at 25°C. "MAXIMUM", "Max.", "MINIMUM" or "Min." represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.**

### 44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




SECTION A-A

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 44 | |
| Lead Pitch | e | | 0.80 BSC | |
| Overall Height | A | - | - | 1.20 |
| Standoff | A1 | 0.05 | - | 0.15 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Overall Width | E | | 12.00 BSC | |
| Molded Package Width | E1 | | 10.00 BSC | |
| Overall Length | D | | 12.00 BSC | |
| Molded Package Length | D1 | | 10.00 BSC | |
| Lead Width | b | 0.30 | 0.37 | 0.45 |
| Lead Thickness | c | 0.09 | - | 0.20 |
| Lead Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | θ | 0° | 3.5° | 7° |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Exact shape of each corner is optional.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076C Sheet 2 of 2