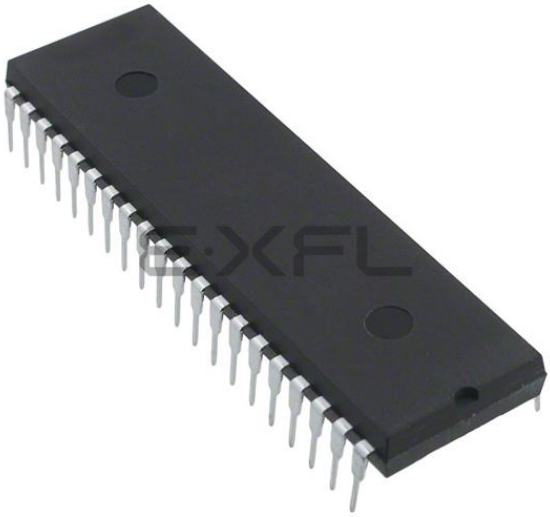

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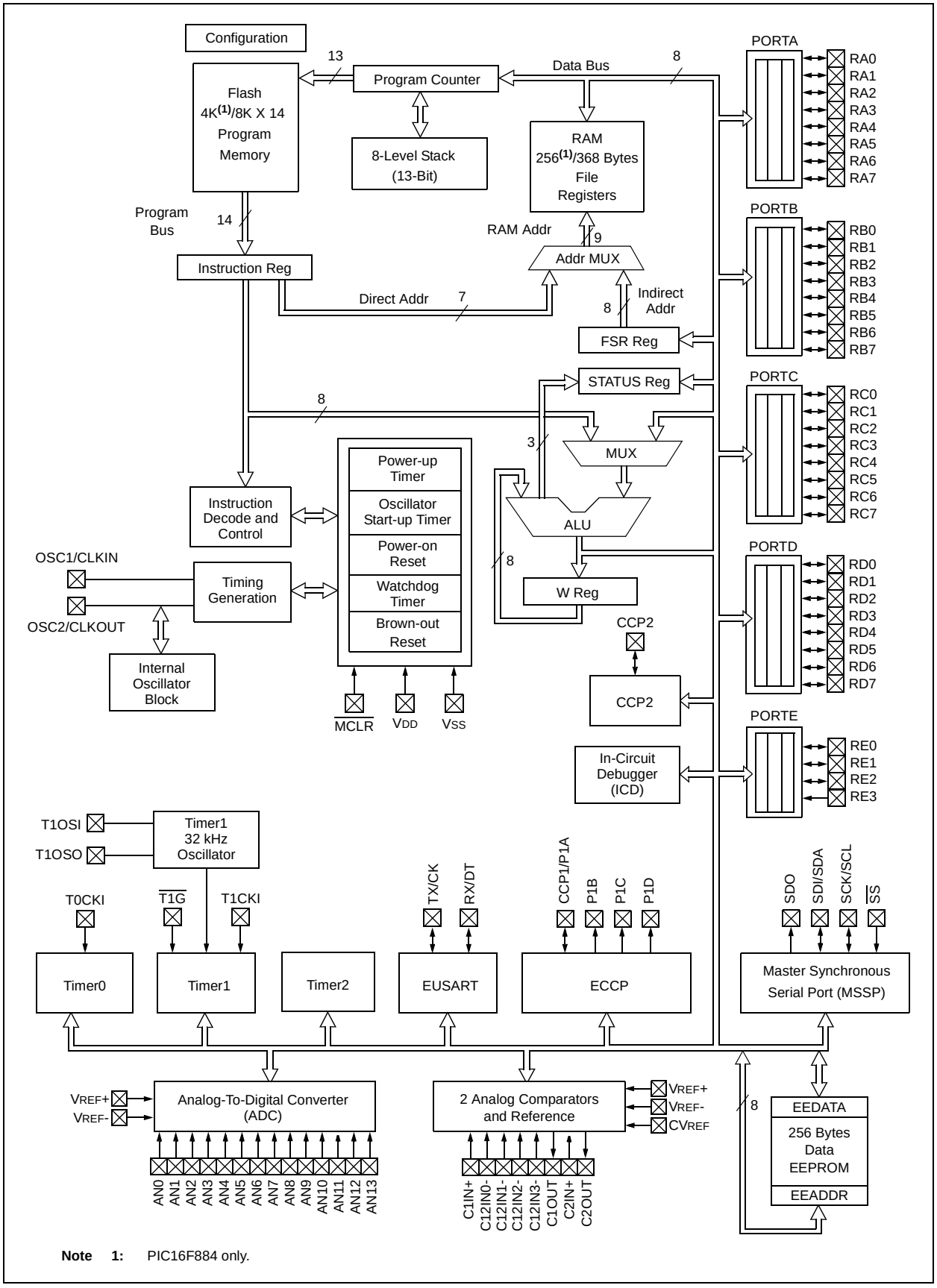
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f884-i-p

FIGURE 1-2: PIC16F884/PIC16F887 BLOCK DIAGRAM



Note 1: PIC16F884 only.

2.2 Data Memory Organization

The data memory (see Figures 2-2 and 2-3) is partitioned into four banks which contain the General Purpose Registers (GPR) and the Special Function Registers (SFR). The Special Function Registers are located in the first 32 locations of each bank. The General Purpose Registers, implemented as static RAM, are located in the last 96 locations of each Bank. Register locations F0h-FFh in Bank 1, 170h-17Fh in Bank 2 and 1F0h-1FFh in Bank 3, point to addresses 70h-7Fh in Bank 0. The actual number of General Purpose Resisters (GPR) implemented in each Bank depends on the device. Details are shown in Figures 2-5 and 2-6. All other RAM is unimplemented and returns '0' when read. RP<1:0> of the STATUS register are the bank select bits:

RP1	RP0	
0	0	→Bank 0 is selected
0	1	→Bank 1 is selected
1	0	→Bank 2 is selected
1	1	→Bank 3 is selected

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 128 x 8 in the PIC16F882, 256 x 8 in the PIC16F883/PIC16F884, and 368 x 8 in the PIC16F886/PIC16F887. Each register is accessed, either directly or indirectly, through the File Select Register (FSR) (see **Section 2.4 "Indirect Addressing, INDF and FSR Registers"**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 2-1). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

FIGURE 2-4: PIC16F882 SPECIAL FUNCTION REGISTERS

Bank 0	File Address	Bank 1	File Address	Bank 2	File Address	Bank 3	File Address
Indirect addr. (1)	00h	Indirect addr. (1)	80h	Indirect addr. (1)	100h	Indirect addr. (1)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h	WDTCON	105h	SRCON	185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h	CM1CON0	107h	BAUDCTL	187h
	08h		88h	CM2CON0	108h	ANSEL	188h
PORTE	09h	TRISE	89h	CM2CON1	109h	ANSELH	189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDAT	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2(1)	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved	18Eh
TMR1H	0Fh	OSCCON	8Fh	EEADRH	10Fh	Reserved	18Fh
T1CON	10h	OSCTUNE	90h		110h		190h
TMR2	11h	SSPCON2	91h		111h		191h
T2CON	12h	PR2	92h		112h		192h
SSPBUF	13h	SSPADD	93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1L	15h	WPUB	95h		115h		195h
CCPR1H	16h	IOCB	96h		116h		196h
CCP1CON	17h	VRCON	97h		117h		197h
RCSTA	18h	TXSTA	98h		118h		198h
TXREG	19h	SPBRG	99h		119h		199h
RCREG	1Ah	SPBRGH	9Ah		11Ah		19Ah
CCPR2L	1Bh	PWM1CON	9Bh		11Bh		19Bh
CCPR2H	1Ch	ECCPAS	9Ch		11Ch		19Ch
CCP2CON	1Dh	PSTRCON	9Dh		11Dh		19Dh
ADRESH	1Eh	ADRESL	9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
	20h	General Purpose Registers	A0h		120h		1A0h
General Purpose Registers		32 Bytes	BFh				
			C0h				
96 Bytes			EFh		16Fh		1EFh
		accesses 70h-7Fh	F0h	accesses 70h-7Fh	170h	accesses 70h-7Fh	1F0h
	7Fh		FFh		17Fh		1FFh

Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

3.2.3 PIN DESCRIPTIONS AND DIAGRAMS

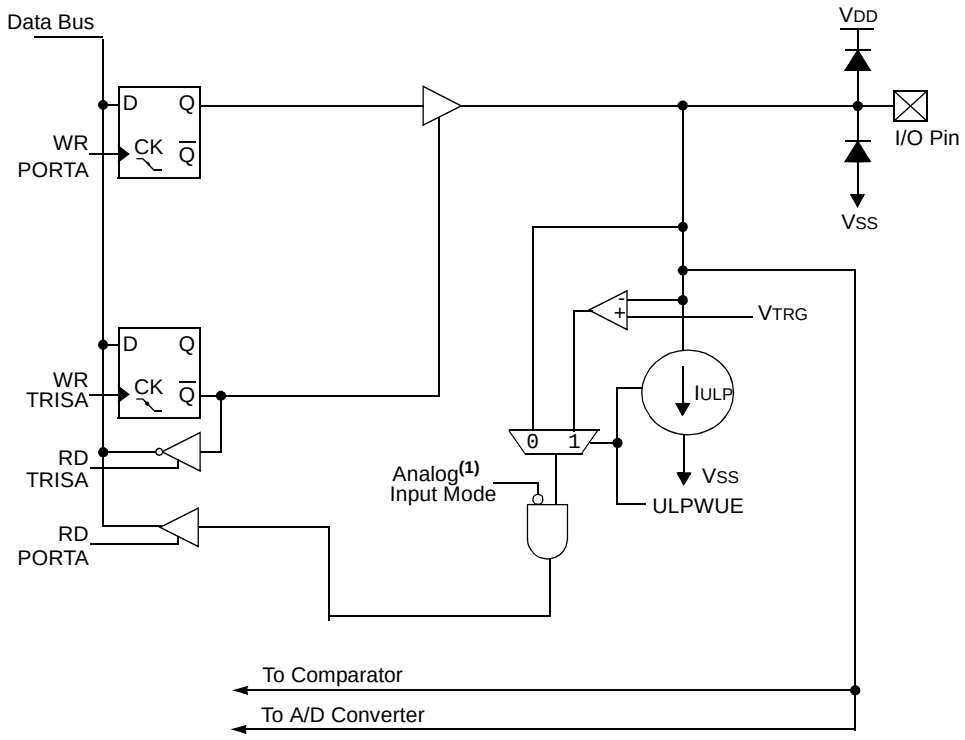
Each PORTA pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the comparator or the A/D Converter (ADC), refer to the appropriate section in this data sheet.

3.2.3.1 RA0/AN0/ULPWU/C12IN0-

Figure 3-1 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a negative analog input to Comparator C1 or C2
- an analog input for the Ultra Low-Power Wake-up

FIGURE 3-1: BLOCK DIAGRAM OF RA0



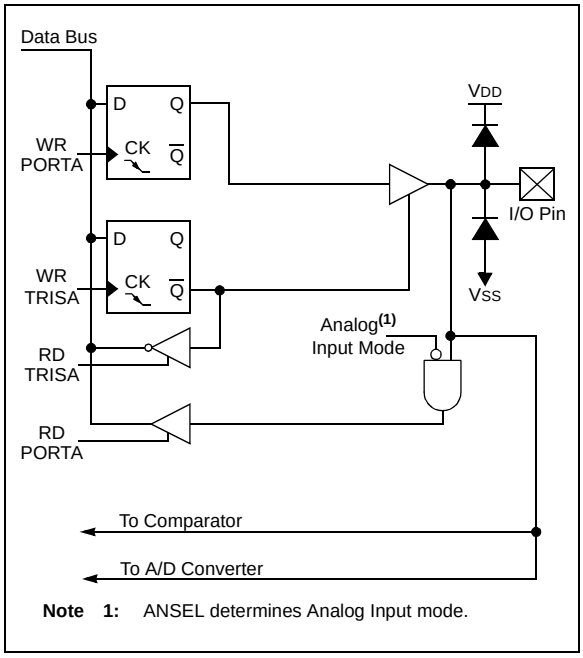
Note 1: ANSEL determines Analog Input mode.

3.2.3.2 RA1/AN1/C12IN1-

Figure 3-2 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a negative analog input to Comparator C1 or C2

FIGURE 3-2: BLOCK DIAGRAM OF RA1



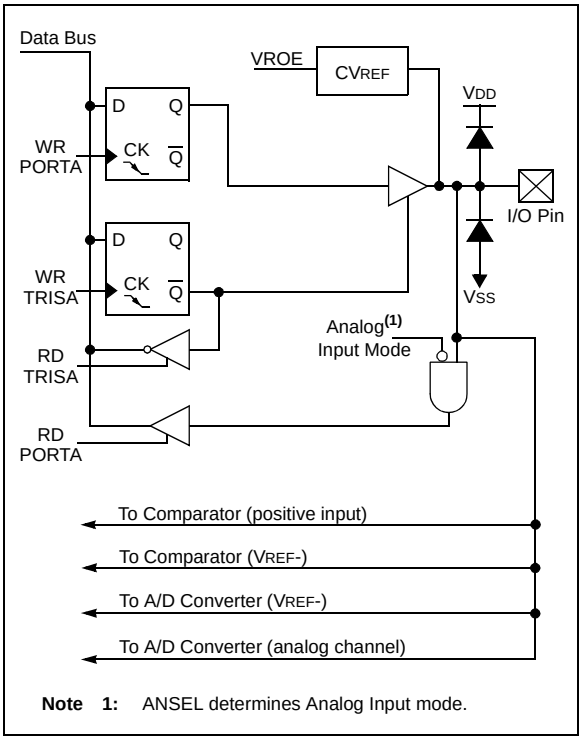
Note 1: ANSEL determines Analog Input mode.

3.2.3.3 RA2/AN2/VREF-/CVREF/C2IN+

Figure 3-3 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a negative voltage reference input for the ADC and CVREF
- a comparator voltage reference output
- a positive analog input to Comparator C2

FIGURE 3-3: BLOCK DIAGRAM OF RA2



Note 1: ANSEL determines Analog Input mode.

3.2.3.8 RA7/OSC1/CLKIN

Figure 3-8 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- a crystal/resonator connection
- a clock input

FIGURE 3-8: BLOCK DIAGRAM OF RA7

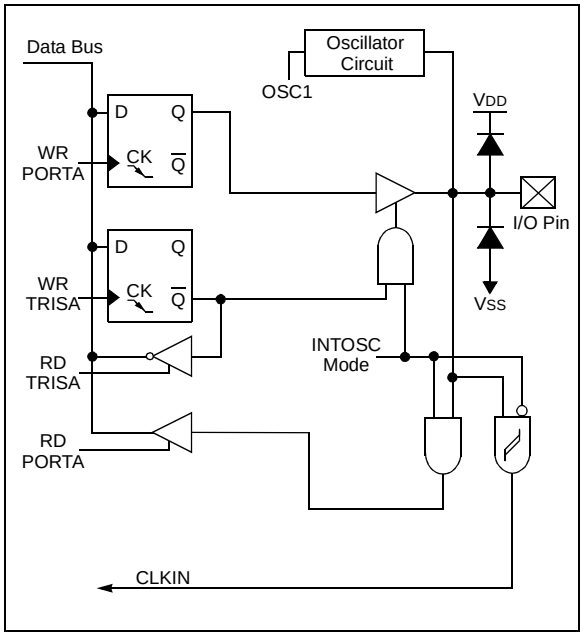


TABLE 3-1: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	ADCS1	ADCS0	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	104
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	41
CM1CON0	C1ON	C1OUT	C1OE	C1POL	—	C1R	C1CH1	C1CH0	89
CM2CON0	C2ON	C2OUT	C2OE	C2POL	—	C2R	C2CH1	C2CH0	90
CM2CON1	MC1OUT	MC2OUT	C1RSEL	C2RSEL	—	—	T1GSS	C2SYNC	92
PCON	—	—	ULPWUE	SBOREN	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	37
OPTION_REG	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	31
PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	40
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	177
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	40

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

3.3 PORTB and TRISB Registers

PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB (Register 3-6). Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 3-3 shows how to initialize PORTB.

Reading the PORTB register (Register 3-5) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch.

The TRISB register (Register 3-6) controls the PORTB pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISB register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'. Example 3-3 shows how to initialize PORTB.

EXAMPLE 3-3: INITIALIZING PORTB

```
BANKSEL PORTB       ;
CLRF    PORTB       ;Init PORTB
BANKSEL TRISB       ;
MOVLW   B'11110000' ;Set RB<7:4> as inputs
                    ;and RB<3:0> as outputs
MOVWF   TRISB       ;
```

Note:	The ANSELH register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

3.4 Additional PORTB Pin Functions

PORTB pins RB<7:0> on the device family device have an interrupt-on-change option and a weak pull-up option. The following three sections describe these PORTB pin functions.

Every PORTB pin on this device family has an interrupt-on-change option and a weak pull-up option.

3.4.1 ANSELH REGISTER

The ANSELH register (Register 3-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELH bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELH bits has no affect on digital output functions. A pin with TRIS clear and ANSELH set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

3.4.2 WEAK PULL-UPS

Each of the PORTB pins has an individually configurable internal weak pull-up. Control bits WPUB<7:0> enable or disable each pull-up (see Register 3-7). Each weak pull-up is automatically turned off when the port pin is configured as an output. All pull-ups are disabled on a Power-on Reset by the $\overline{\text{RBPU}}$ bit of the OPTION register.

3.4.3 INTERRUPT-ON-CHANGE

All of the PORTB pins are individually configurable as an interrupt-on-change pin. Control bits IOCB<7:0> enable or disable the interrupt function for each pin. Refer to Register 3-8. The interrupt-on-change feature is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the present value is compared with the old value latched on the last read of PORTB to determine which bits have changed or mismatched the old value. The 'mismatch' outputs of the last read are OR'd together to set the PORTB Change Interrupt flag bit (RBIF) in the INTCON register.

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, clears the interrupt by:

a) Any read or write of PORTB. This will end the mismatch condition.
b) Clear the flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading or writing PORTB will end the mismatch condition and allow flag bit RBIF to be cleared. The latch holding the last read value is not affected by a $\overline{\text{MCLR}}$ nor Brown-out Reset. After these Resets, the RBIF flag will continue to be set if a mismatch is present.

Note:	If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not get set. Furthermore, since a read or write on a port affects all bits of that port, care must be taken when using multiple pins in Interrupt-on-Change mode. Changes on one pin may not be seen while servicing changes on another pin.

10.1.4 READING THE FLASH PROGRAM MEMORY

To read a program memory location, the user must write the Least and Most Significant address bits to the EEADR and EEADRH registers, set the EEPGD control bit of the EECON1 register, and then set control bit RD. Once the read control bit is set, the program memory Flash controller will use the second instruction cycle to read the data. This causes the second instruction immediately following the "BSF EECON1,RD" instruction to be ignored. The data is available in the very next cycle, in the EEDAT and EEDATH registers; therefore, it can be read as two bytes in the following instructions.

EEDAT and EEDATH registers will hold this value until another read or until it is written to by the user.

Note 1: The two instructions following a program memory read are required to be NOPs. This prevents the user from executing a 2-cycle instruction on the next instruction after the RD bit is set.

2: If the WR bit is set when EEPGD = 1, it will be immediately reset to '0' and no operation will take place.

EXAMPLE 10-3: FLASH PROGRAM READ

```
    BANKSEL EEADR               ;
    MOVLW   MS_PROG_EE_ADDR     ;
    MOVWF   EEADRH              ;MS Byte of Program Address to read
    MOVLW   LS_PROG_EE_ADDR     ;
    MOVWF   EEADR               ;LS Byte of Program Address to read
    BANKSEL EECON1              ;
    BSF     EECON1, EEPGD       ;Point to PROGRAM memory
    BSF     EECON1, RD          ;EE Read
                                ;
                                ;First instruction after BSF EECON1,RD executes normally
    NOP
    NOP                         ;Any instructions here are ignored as program
                                ;memory is read in second cycle after BSF EECON1,RD
;
    BANKSEL EEDAT               ;
    MOVF    EEDAT, W            ;W = LS Byte of Program Memory
    MOVWF   LOWPMBYTE           ;
    MOVF    EEDATH, W           ;W = MS Byte of Program EEDAT
    MOVWF   HIGHPMBYTE          ;
    BCF     STATUS, RP1         ;Bank 0
```

Required Sequence

11.5.4 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCPx pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

11.5.5 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See **Section 4.0 "Oscillator Module (With Fail-Safe Clock Monitor)"** for additional details.

11.5.6 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

11.5.7 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Disable the PWM pin (CCPx) output drivers as an input by setting the associated TRIS bit.
2. Set the PWM period by loading the PR2 register.
3. Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.
4. Set the PWM duty cycle by loading the CCPRxL register and DCxB<1:0> bits of the CCPxCON register.
5. Configure and start Timer2:
   - Clear the TMR2IF interrupt flag bit of the PIR1 register.
   - Set the Timer2 prescale value by loading the T2CKPS bits of the T2CON register.
   - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output after a new PWM cycle has started:
   - Wait until Timer2 overflows (TMR2IF bit of the PIR1 register is set).
   - Enable the CCPx pin output driver by clearing the associated TRIS bit.

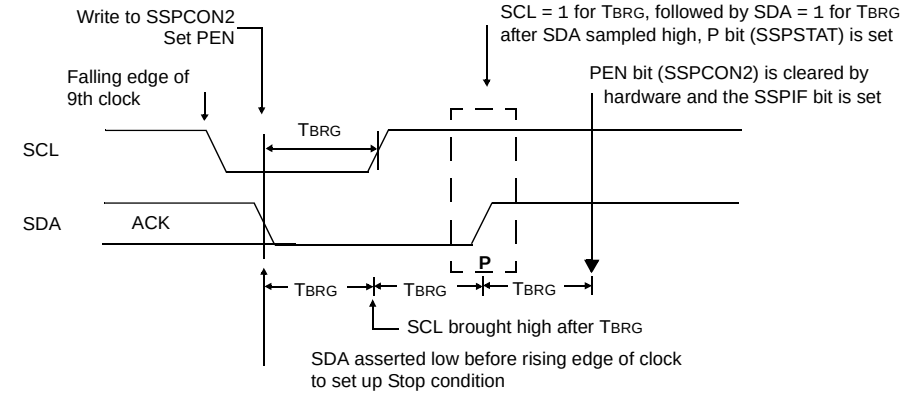
TABLE 12-5: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 0											
	FOSC = 4.000 MHz			FOSC = 3.6864 MHz			FOSC = 2.000 MHz			FOSC = 1.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	—	—	—	—	—	—	—	—	—	300	0.16	207
1200	1202	0.16	207	1200	0.00	191	1202	0.16	103	1202	0.16	51
2400	2404	0.16	103	2400	0.00	95	2404	0.16	51	2404	0.16	25
9600	9615	0.16	25	9600	0.00	23	9615	0.16	12	—	—	—
10417	10417	0.00	23	10473	0.53	21	10417	0.00	11	10417	0.00	5
19.2k	19.23k	0.16	12	19.2k	0.00	11	—	—	—	—	—	—
57.6k	—	—	—	57.60k	0.00	3	—	—	—	—	—	—
115.2k	—	—	—	115.2k	0.00	1	—	—	—	—	—	—

BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 1											
	FOSC = 20.000 MHz			FOSC = 18.432 MHz			FOSC = 11.0592 MHz			FOSC = 8.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	-0.01	4166	300.0	0.00	3839	300.0	0.00	2303	299.9	-0.02	1666
1200	1200	-0.03	1041	1200	0.00	959	1200	0.00	575	1199	-0.08	416
2400	2399	-0.03	520	2400	0.00	479	2400	0.00	287	2404	0.16	207
9600	9615	0.16	129	9600	0.00	119	9600	0.00	71	9615	0.16	51
10417	10417	0.00	119	10378	-0.37	110	10473	0.53	65	10417	0.00	47
19.2k	19.23k	0.16	64	19.20k	0.00	59	19.20k	0.00	35	19.23k	0.16	25
57.6k	56.818	-1.36	21	57.60k	0.00	19	57.60k	0.00	11	55556	-3.55	8
115.2k	113.636	-1.36	10	115.2k	0.00	9	115.2k	0.00	5	—	—	—

BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 1											
	FOSC = 4.000 MHz			FOSC = 3.6864 MHz			FOSC = 2.000 MHz			FOSC = 1.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.1	0.04	832	300.0	0.00	767	299.8	-0.108	416	300.5	0.16	207
1200	1202	0.16	207	1200	0.00	191	1202	0.16	103	1202	0.16	51
2400	2404	0.16	103	2400	0.00	95	2404	0.16	51	2404	0.16	25
9600	9615	0.16	25	9600	0.00	23	9615	0.16	12	—	—	—
10417	10417	0.00	23	10473	0.53	21	10417	0.00	11	10417	0.00	5
19.2k	19.23k	0.16	12	19.20k	0.00	11	—	—	—	—	—	—
57.6k	—	—	—	57.60k	0.00	3	—	—	—	—	—	—
115.2k	—	—	—	115.2k	0.00	1	—	—	—	—	—	—

FIGURE 13-18: STOP CONDITION RECEIVE OR TRANSMIT MODE



Note: TBRG = one Baud Rate Generator period.

13.4.12 CLOCK ARBITRATION

Clock arbitration occurs when the master, during any receive, transmit or Repeated Start/Stop condition, de-asserts the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the Baud Rate Generator (BRG) is suspended from counting until the SCL pin is actually sampled high. When the SCL pin is sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<6:0> and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count, in the event that the clock is held low by an external device (Figure 13-19).

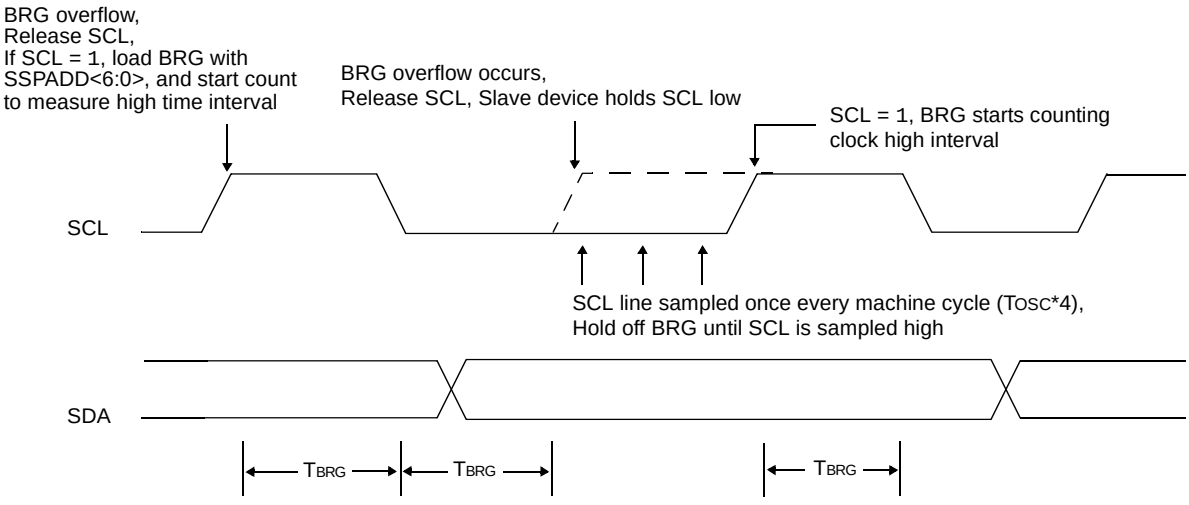
13.4.13 SLEEP OPERATION

While in Sleep mode, the I^2C module can receive addresses or data, and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSP interrupt is enabled).

13.4.14 EFFECT OF A RESET

A Reset disables the MSSP module and terminates the current transfer.

FIGURE 13-19: CLOCK ARBITRATION TIMING IN MASTER TRANSMIT MODE



14.1 Configuration Bits

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations as shown in Register 14-1. These bits are mapped in program memory location 2007h and 2008h, respectively.

Note: Address 2007h and 2008h are beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "*PIC16F88X Memory Programming Specification*" (DS41287) for more information.

REGISTER DEFINITIONS: CONFIGURATION WORDS

REGISTER 14-1: CONFIG1: CONFIGURATION WORD REGISTER 1

$\overline{\text{DEBUG}}$	LVP	FCMEN	IESO	BOREN<1:0>
bit 13				bit 8

$\overline{\text{CPD}}$	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC<2:0>
bit 7					bit 0

bit 13 **$\overline{\text{DEBUG}}$:** In-Circuit Debugger Mode bit
1 = In-Circuit Debugger disabled, RB6/ICSPCLK and RB7/ICSPDAT are general purpose I/O pins
0 = In-Circuit Debugger enabled, RB6/ICSPCLK and RB7/ICSPDAT are dedicated to the debugger

bit 12 **LVP:** Low Voltage Programming Enable bit
1 = RB3/PGM pin has PGM function, low voltage programming enabled
0 = RB3 pin is digital I/O, HV on $\overline{\text{MCLR}}$ must be used for programming

bit 11 **FCMEN:** Fail-Safe Clock Monitor Enabled bit
1 = Fail-Safe Clock Monitor is enabled
0 = Fail-Safe Clock Monitor is disabled

bit 10 **IESO:** Internal External Switchover bit
1 = Internal/External Switchover mode is enabled
0 = Internal/External Switchover mode is disabled

bit 9-8 **BOREN<1:0>:** Brown-out Reset Selection bits(1)
11 = BOR enabled
10 = BOR enabled during operation and disabled in Sleep
01 = BOR controlled by SBOREN bit of the PCON register
00 = BOR disabled

bit 7 **$\overline{\text{CPD}}$:** Data Code Protection bit(2)
1 = Data memory code protection is disabled
0 = Data memory code protection is enabled

bit 6 **$\overline{\text{CP}}$:** Code Protection bit(3)
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 5 **MCLRE:** RE3/$\overline{\text{MCLR}}$ pin function select bit(4)
1 = RE3/$\overline{\text{MCLR}}$ pin function is $\overline{\text{MCLR}}$
0 = RE3/$\overline{\text{MCLR}}$ pin function is digital input, $\overline{\text{MCLR}}$ internally tied to V_{DD}

bit 4 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled and can be enabled by SWDTEN bit of the WDTCON register

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
111 = RC oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, RC on RA7/OSC1/CLKIN
110 = RCIO oscillator: I/O function on RA6/OSC2/CLKOUT pin, RC on RA7/OSC1/CLKIN
101 = INTOSC oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN
100 = INTOSCIO oscillator: I/O function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN
011 = EC: I/O function on RA6/OSC2/CLKOUT pin, CLKIN on RA7/OSC1/CLKIN
010 = HS oscillator: High-speed crystal/resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN
001 = XT oscillator: Crystal/resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN
000 = LP oscillator: Low-power crystal on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: The entire data EEPROM will be erased when the code protection is turned off.
3: The entire program memory will be erased when the code protection is turned off.
4: When $\overline{\text{MCLR}}$ is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.

TABLE 14-4: INITIALIZATION CONDITION FOR REGISTER (CONTINUED)

Register	Address	Power-on Reset	$\overline{\text{MCLR}}$ Reset WDT Reset (Continued) Brown-out Reset(1)	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out (Continued)
CM2CON1	109h	0000 0--0	0000 0--0	uuuu u--u
EEDAT	10Ch	0000 0000	0000 0000	uuuu uuuu
EEADR	10Dh	0000 0000	0000 0000	uuuu uuuu
EEDATH	10Eh	--00 0000	--00 0000	--uu uuuu
EEADRH	10Fh	---0 0000	---0 0000	---u uuuu
SRCON	185h	0000 00-0	0000 00-0	uuuu uu-u
BAUDCTL	187h	01-0 0-00	01-0 0-00	uu-u u-uu
ANSEL	188h	1111 1111	1111 1111	uuuu uuuu
ANSELH	189h	1111 1111	1111 1111	uuuu uuuu
EECON1	18Ch	---- x000	---- q000	---- uuuu
EECON2	18Dh	---- ----	---- ----	---- ----

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 14-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

6: Accessible only when SSPCON register bits SSPM<3:0> = 1001.

TABLE 14-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	Status Register	PCON Register
Power-on Reset	000h	0001 1xxx	--01 --0x
$\overline{\text{MCLR}}$ Reset during normal operation	000h	000u uuuu	--0u --uu
$\overline{\text{MCLR}}$ Reset during Sleep	000h	0001 0uuu	--0u --uu
WDT Reset	000h	0000 uuuu	--0u --uu
WDT Wake-up	PC + 1	uuu0 0uuu	--uu --uu
Brown-out Reset	000h	0001 1uuu	--01 --u0
Interrupt Wake-up from Sleep	PC + 1(1)	uuu1 0uuu	--uu --uu

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and Global Interrupt Enable bit, GIE, is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

14.3 Interrupts

The PIC16F882/883/884/886/887 devices have multiple interrupt sources:

- External Interrupt RB0/INT
- Timer0 Overflow Interrupt
- PORTB Change Interrupts
- 2 Comparator Interrupts
- A/D Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- EEPROM Data Write Interrupt
- Fail-Safe Clock Monitor Interrupt
- Enhanced CCP Interrupt
- EUSART Receive and Transmit Interrupts
- Ultra Low-Power Wake-up Interrupt
- MSSP Interrupt

The Interrupt Control register (INTCON) and Peripheral Interrupt Request Register 1 (PIR1) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

A Global Interrupt Enable bit, GIE (INTCON<7>), enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in the INTCON, PIE1 and PIE2 registers, respectively. GIE is cleared on Reset.

The Return from Interrupt instruction, RETFIE, exits the interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT Pin Interrupt
- PORTB Change Interrupts
- Timer0 Overflow Interrupt

The peripheral interrupt flags are contained in the PIR1 and PIR2 registers. The corresponding interrupt enable bits are contained in PIE1 and PIE2 registers.

The following interrupt flags are contained in the PIR1 register:

- A/D Interrupt
- EUSART Receive and Transmit Interrupts
- Timer1 Overflow Interrupt
- Synchronous Serial Port (SSP) Interrupt
- Enhanced CCP1 Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt

The following interrupt flags are contained in the PIR2 register:

- Fail-Safe Clock Monitor Interrupt
- 2 Comparator Interrupts
- EEPROM Data Write Interrupt
- Ultra Low-Power Wake-up Interrupt
- CCP2 Interrupt

When an interrupt is serviced:

- The GIE is cleared to disable any further interrupt.
- The return address is pushed onto the stack.
- The PC is loaded with 0004h.

For external interrupt events, such as the INT pin, PORTB change interrupts, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 14-8). The latency is the same for one or two-cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

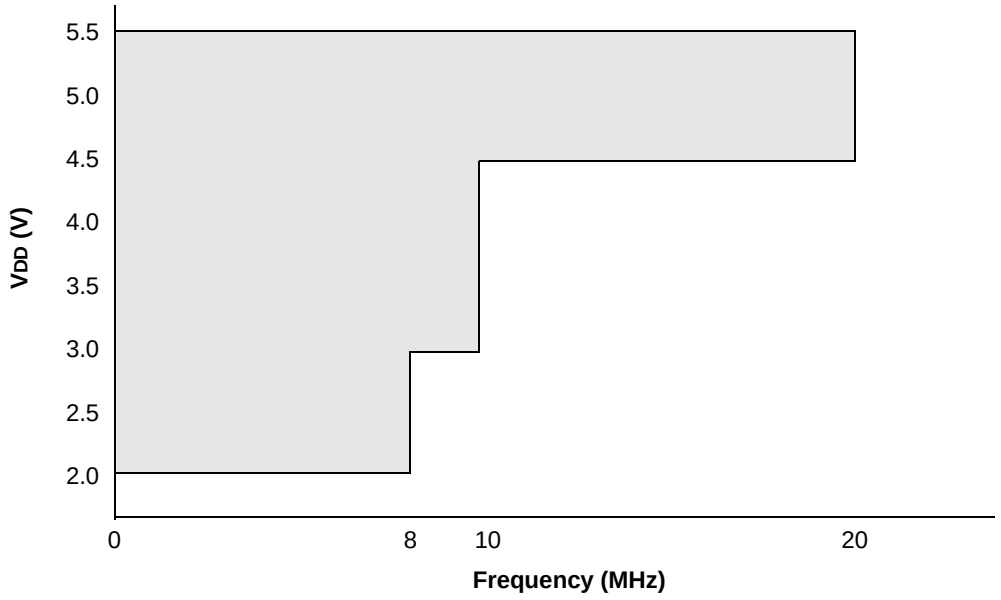
Note 1:	Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.
2:	When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts, which were ignored, are still pending to be serviced when the GIE bit is set again.

For additional information on Timer1, Timer2, comparators, A/D, data EEPROM, EUSART, MSSP or Enhanced CCP modules, refer to the respective peripheral section.

14.3.1 RB0/INT INTERRUPT

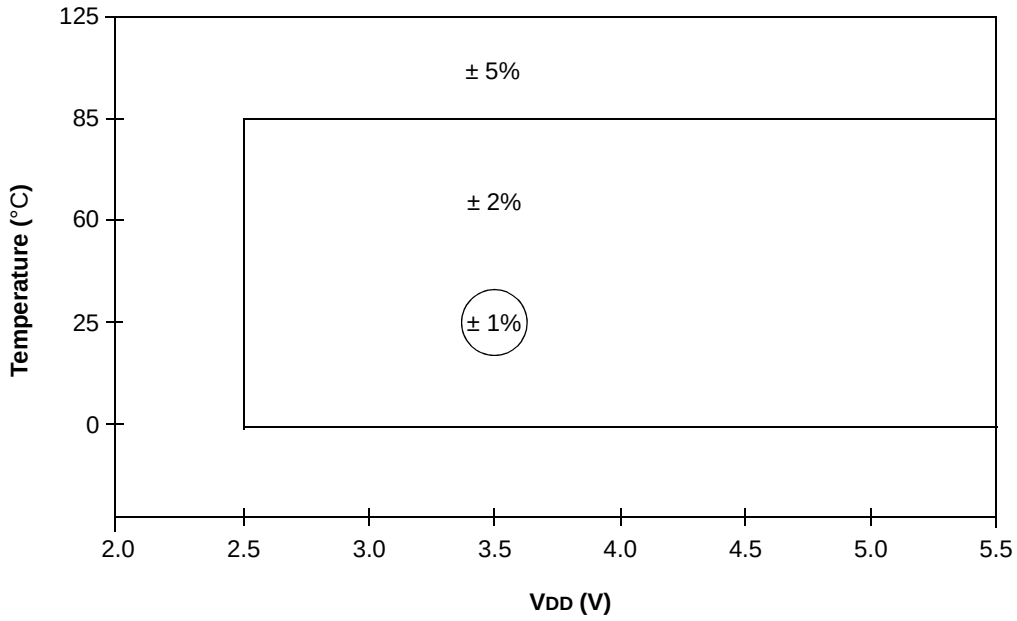
External interrupt on RB0/INT pin is edge-triggered; either rising if the INTEDG bit (OPTION_REG<6>) is set, or falling, if the INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing the INTE control bit (INTCON<4>). The INTF bit must be cleared in software in the Interrupt Service Routine before re-enabling this interrupt. The RB0/INT interrupt can wake-up the processor from Sleep, if the INTE bit was set prior to going into Sleep. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up (0004h). See **Section 14.6 “Power-Down Mode (Sleep)”** for details on Sleep and Figure 14-10 for timing of wake-up from Sleep through RB0/INT interrupt.

FIGURE 17-1: PIC16F882/883/884/886/887 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 17-2: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE



17.2 DC Characteristics: PIC16F882/883/884/886/887-I (Industrial) PIC16F882/883/884/886/887-E (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
						VDD	Note
D010	Supply Current (IDD)(1, 2)	—	13	19	µA	2.0	FOSC = 32 kHz LP Oscillator mode
		—	22	30	µA	3.0	
		—	33	60	µA	5.0	
D011*		—	180	250	µA	2.0	FOSC = 1 MHz XT Oscillator mode
		—	290	400	µA	3.0	
		—	490	650	µA	5.0	
D012		—	280	380	µA	2.0	FOSC = 4 MHz XT Oscillator mode
		—	480	670	µA	3.0	
		—	0.9	1.4	mA	5.0	
D013*		—	170	295	µA	2.0	FOSC = 1 MHz EC Oscillator mode
		—	280	480	µA	3.0	
		—	470	690	µA	5.0	
D014		—	290	450	µA	2.0	FOSC = 4 MHz EC Oscillator mode
		—	490	720	µA	3.0	
		—	0.85	1.3	mA	5.0	
D015		—	8	20	µA	2.0	FOSC = 31 kHz LFINTOSC mode
		—	16	40	µA	3.0	
		—	31	65	µA	5.0	
D016*		—	416	520	µA	2.0	FOSC = 4 MHz HFINTOSC mode
		—	640	840	µA	3.0	
		—	1.13	1.6	mA	5.0	
D017		—	0.65	0.9	mA	2.0	FOSC = 8 MHz HFINTOSC mode
		—	1.01	1.3	mA	3.0	
		—	1.86	2.3	mA	5.0	
D018		—	340	580	µA	2.0	FOSC = 4 MHz EXTRC mode(3)
		—	550	900	µA	3.0	
		—	0.92	1.4	mA	5.0	
D019		—	3.8	4.7	mA	4.5	FOSC = 20 MHz HS Oscillator mode
		—	4.0	4.8	mA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.

17.8 AC Characteristics: PIC16F882/883/884/886/887 (Industrial, Extended)

FIGURE 17-4: CLOCK TIMING

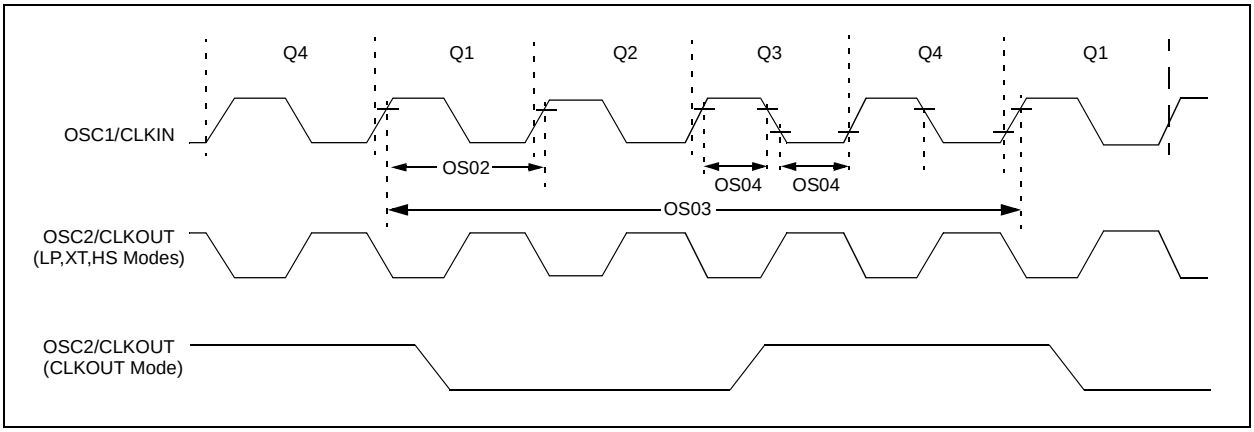


TABLE 17-1: CLOCK OSCILLATOR TIMING REQUIREMENTS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
OS01	FOSC	External CLKIN Frequency(1)	DC	—	37	kHz	LP Oscillator mode
			DC	—	4	MHz	XT Oscillator mode
			DC	—	20	MHz	HS Oscillator mode
			DC	—	20	MHz	EC Oscillator mode
		Oscillator Frequency(1)	—	32.768	—	kHz	LP Oscillator mode
			0.1	—	4	MHz	XT Oscillator mode
			1	—	20	MHz	HS Oscillator mode
			DC	—	4	MHz	RC Oscillator mode
OS02	TOSC	External CLKIN Period(1)	27	—	•	µs	LP Oscillator mode
			250	—	•	ns	XT Oscillator mode
			50	—	•	ns	HS Oscillator mode
			50	—	•	ns	EC Oscillator mode
		Oscillator Period(1)	—	30.5	—	µs	LP Oscillator mode
			250	—	10,000	ns	XT Oscillator mode
			50	—	1,000	ns	HS Oscillator mode
			250	—	—	ns	RC Oscillator mode
OS03	TCY	Instruction Cycle Time(1)	200	TCY	DC	ns	TCY = 4/FOSC
OS04*	TosH, TosL	External CLKIN High, External CLKIN Low	2	—	—	µs	LP oscillator
			100	—	—	ns	XT oscillator
			20	—	—	ns	HS oscillator
OS05*	TosR, TosF	External CLKIN Rise, External CLKIN Fall	0	—	•	ns	LP oscillator
			0	—	•	ns	XT oscillator
			0	—	•	ns	HS oscillator

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

TABLE 17-7: COMPARATOR SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C								
Param No.	**Sym.**	**Characteristics**		**Min.**	**Typ†**	**Max.**	**Units**	**Comments**
CM01	VOS	Input Offset Voltage		—	± 5.0	± 10	mV	(VDD - 1.5)/2
CM02	VCM	Input Common Mode Voltage		0	—	VDD - 1.5	V	
CM03*	CMRR	Common Mode Rejection Ratio		+55	—	—	dB	
CM04*	TRT	Response Time	Falling	—	150	600	ns	**(Note 1)**
			Rising	—	200	1000	ns	
CM05*	TMC2COV	Comparator Mode Change to Output Valid		—	—	10	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Response time is measured with one comparator input at (VDD - 1.5)/2 - 100 mV to (VDD - 1.5)/2 + 20 mV.

TABLE 17-8: COMPARATOR VOLTAGE REFERENCE (CVREF) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym.**	**Characteristics**	**Min.**	**Typ†**	**Max.**	**Units**	**Comments**
CV01*	CLSB	Step Size(2)	— —	VDD/24 VDD/32	— —	V V	Low Range (VRR = 1) High Range (VRR = 0)
CV02*	CACC	Absolute Accuracy	— —	— —	± 1/2 ± 1/2	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
CV03*	CR	Unit Resistor Value (R)	—	2k	—	Ω	
CV04*	CST	Settling Time(1)	—	—	10	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from '0000' to '1111'.

2: See **Section 8.10 "Comparator Voltage Reference"** for more information.

TABLE 17-9: VOLTAGE (VR) REFERENCE SPECIFICATIONS

VR Voltage Reference Specifications			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
VR01	VROUT	VR voltage output	0.5	0.6	0.7	V	
VR02*	TSTABLE	Settling Time	—	10	100*	µs	

* These parameters are characterized but not tested.

17.9 High Temperature Operation

This section outlines the specifications for the following devices operating in the high temperature range between -40°C and 150°C.(4)

- PIC16F886
- PIC16F887

When the value of any parameter is identical for both the 125°C Extended and the 150°C High Temp. temperature ranges, then that value will be found in the standard specification tables shown earlier in this chapter, under the fields listed for the 125°C Extended temperature range. If the value of any parameter is unique to the 150°C High Temp. temperature range, then it will be listed here, in this section of the data sheet.

If a Silicon Errata exists for the product and it lists a modification to the 125°C Extended temperature range value, one that is also shared at the 150°C high temp. temperature range, then that modified value will apply to both temperature ranges.

Note 1: Writes are **not allowed** for Flash program memory above 125°C.

2: The temperature range indicator in the catalog part number and device marking is “H” for -40°C to 150°C.

Example: PIC16F887T-H/PT indicates the device is shipped in a Tape and reel configuration, in the TQFP package, and is rated for operation from -40°C to 150°C.

3: The +150°C version of the PIC16F886 and PIC16F887 will not be offered in PDIP. It will only be offered in SSOP, SOIC, QFN and TQFP.

4: AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time from 125°C to 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

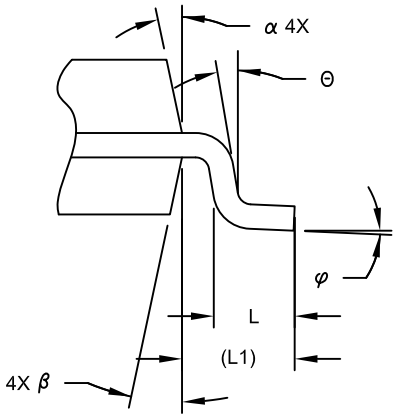
TABLE 17-17: ABSOLUTE MAXIMUM RATINGS

Parameter	Source/Sink	Value	Units
Max. Current: V_{DD}	Source	20	mA
Max. Current: V_{SS}	Sink	50	mA
Max. Current: Pin	Source	5	mA
Max. Current: Pin	Sink	10	mA
Max. Pin Current: at V_{OH}	Source	3	mA
Max. Pin Current: at V_{OL}	Sink	8.5	mA
Max. Port Current: A, B, and C combined	Source	20	mA
Max. Port Current: A, B, and C combined	Sink	50	mA
Max. Junction Temperature		155	°C

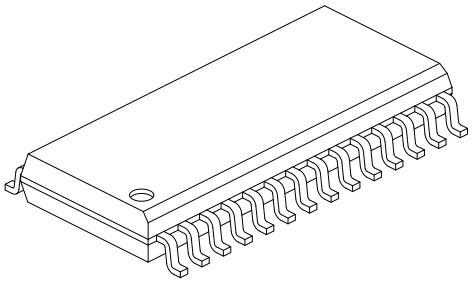
Note: Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2