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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	24
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f886-e-ss

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TABLE 1-1: PIC16F882/883/886 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB3/AN9/PGM/C12IN2-	RB3	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN9	AN		A/D Channel 9.
	PGM	ST		Low-voltage ICSP™ Programming enable pin.
	C12IN2-	AN		Comparator C1 or C2 negative input.
RB4/AN11/P1D	RB4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN11	AN	_	A/D Channel 11.
	P1D	—	CMOS	PWM output.
RB5/AN13/T1G	RB5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN13	AN	—	A/D Channel 13.
	T1G	ST	—	Timer1 Gate input.
RB6/ICSPCLK	RB6	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	ICSPCLK	ST		Serial Programming Clock.
RB7/ICSPDAT	RB7	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RC0/T1OSO/T1CKI	RC0	ST	CMOS	General purpose I/O.
	T10SO	—	CMOS	Timer1 oscillator output.
	T1CKI	ST	—	Timer1 clock input.
RC1/T1OSI/CCP2	RC1	ST	CMOS	General purpose I/O.
	T1OSI	ST	—	Timer1 oscillator input.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
RC2/P1A/CCP1	RC2	ST	CMOS	General purpose I/O.
	P1A	—	CMOS	PWM output.
	CCP1	ST	CMOS	Capture/Compare/PWM1.
RC3/SCK/SCL	RC3	ST	CMOS	General purpose I/O.
	SCK	ST	CMOS	SPI clock.
	SCL	SI	OD	
RC4/SDI/SDA	RC4	ST	CMOS	General purpose I/O.
	SDI	SI	-	SPI data input.
	SDA	SI	OD	
RC5/3D0	RC5	31	CIVIOS	Selleral pulpose I/O.
PC6/TV/CK	BC6	— ет	CMOS	
KC0/TA/CK	ту	51	CMOS	ELISAPT asynchronous transmit
	CK	ST	CMOS	EUSART synchronous clock
	BC7	ST	CMOS	
	RX	ST		EUSART asynchronous input
		ST	CMOS	EUSART synchronous data
RE3/MCLR/Vpp	RE3	тті	_	General purpose input.
	MCLR	ST	_	Master Clear with internal pull-up
	VPP	HV		Programming voltage.
Vss	Vss	Power		Ground reference.
Vdd	VDD	Power		Positive supply.
Legend: AN = Analog input	or output	CMOS	= CMO	S compatible input or output OD = Open-Drain
TTL = TTL compatil HV = High Voltage	ole input	ST XTAL	= Schm = Crysta	itt Trigger input with CMOS levels al

FIGURE 2-6: PIC16F886/PIC16F887 SPECIAL FUNCTION REGISTERS

	File		File		File		File
	Address		Address		Address		Address
Indirect addr. (1)	00h	Indirect addr. (1)	80h	Indirect addr. (1)	100h	Indirect addr. (1)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h	WDTCON	105h	SRCON	185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h	CM1CON0	107h	BAUDCTL	187h
PORTD ⁽²⁾	08h	TRISD ⁽²⁾	88h	CM2CON0	108h	ANSEL	188h
PORTE	09h	TRISE	89h	CM2CON1	109h	ANSELH	189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDAT	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2 ⁽¹⁾	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved	18Eh
TMR1H	0Fh	OSCCON	8Fh	EEADRH	10Fh	Reserved	18Fh
T1CON	10h	OSCTUNE	90h		110h		190h
TMR2	11h	SSPCON2	91h		111h		191h
T2CON	12h	PR2	92h		112h		192h
SSPBUF	13h	SSPADD	93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1L	15h	WPUB	95h		115h		195h
CCPR1H	16h	IOCB	96h	General	116h	General	196h
CCP1CON	17h	VRCON	97h	Purpose	117h	Purpose	197h
RCSTA	18h	TXSTA	98h	registers	118h	registers	198h
TXREG	19h	SPBRG	99h	16 Bytes	119h	16 Bytes	199h
RCREG	1Ah	SPBRGH	9Ah		11Ah		19Ah
CCPR2L	1Bh	PWM1CON	9Bh		11Bh		19Bh
CCPR2H	1Ch	ECCPAS	9Ch		11Ch		19Ch
CCP2CON	1Dh	PSTRCON	9Dh		11Dh		19Dh
ADRESH	1Eh	ADRESL	9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
	20h	General	A0h		120h		1A0h
	2Eb	Purpose		General		General	l
General	3F11 40b	Registers		Purpose Registers		Purpose Registers	l
Purpose	4011			registers		registers	l
Registers		80 Bytes		80 Bytes		80 Bytes	l
96 Bytes	6Fh		EFh		16Fh		1EFh
	70h	accesses	F0h	accesses	170h	accesses	1F0h
	7Fh	70h-7Fh	FFh	70h-7Fh	17Fh	70h-7Fh	1FFh
Bank 0		Bank 1		Bank 2		Bank 3	
Unimplement	ed data me	emory locations, re	ad as '0'.				
Note 1: Not a	physical re	gister.					

2: PIC16F887 only.

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0
bit 7		•					bit 0
Legend:							

REGISTER 3-7: WPUB: WEAK PULL-UP PORTB REGISTER

Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 7-0 WPUB<7:0>: Weak Pull-up Register bit

- 1 = Pull-up enabled
- 0 = Pull-up disabled

Note 1: Global RBPU bit of the OPTION register must be cleared for individual pull-ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is in configured as an output.

REGISTER 3-8: IOCB: INTERRUPT-ON-CHANGE PORTB REGISTER

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IOCB7 | IOCB6 | IOCB5 | IOCB4 | IOCB3 | IOCB2 | IOCB1 | IOCB0 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 IOCB<7:0>: Interrupt-on-Change PORTB Control bit

1 = Interrupt-on-change enabled

0 = Interrupt-on-change disabled

3.4.4.5 RB4/AN11/P1D⁽¹⁾

Figure 3-10 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a PWM output⁽¹⁾

Note 1: P1D is available on PIC16F882/883/886 only.

3.4.4.6 RB5/AN13/T1G

Figure 3-10 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a Timer1 gate input

3.4.4.7 RB6/ICSPCLK

Figure 3-10 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- In-Circuit Serial Programming clock

3.4.4.8 RB7/ICSPDAT

Figure 3-10 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- In-Circuit Serial Programming data

3.5.7 RC6/TX/CK

Figure 3-17 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an asynchronous serial output
- a synchronous clock I/O



3.5.8 RC7/RX/DT

Figure 3-18 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- an asynchronous serial input
- a synchronous serial data I/O



TABLE 3-3: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CCP1CON	P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	122
CCP2CON	—	_	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	123
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	54
PSTRCON	—	—	—	STRSYNC	STRD	STRC	STRB	STRA	144
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	158
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	177
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	81
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	54

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTC.

4.7.2 TWO-SPEED START-UP SEQUENCE

- 1. Wake-up from Power-on Reset or Sleep.
- Instructions begin execution by the internal oscillator at the frequency set in the IRCF<2:0> bits of the OSCCON register.
- 3. OST enabled to count 1024 clock cycles.
- 4. OST timed out, wait for falling edge of the internal oscillator.
- 5. OSTS is set.
- 6. System clock held low until the next falling edge of new clock (LP, XT or HS mode).
- 7. System clock is switched to external clock source.

4.7.3 CHECKING TWO-SPEED CLOCK STATUS

Checking the state of the OSTS bit of the OSCCON register will confirm if the microcontroller is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Word Register 1 (CONFIG1), or the internal oscillator.



FIGURE 4-7: TWO-SPEED START-UP

6.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is a 16-bit timer/counter with the following features:

- 16-bit timer/counter register pair (TMR1H:TMR1L)
- · Programmable internal or external clock source
- 3-bit prescaler
- Optional LP oscillator
- Synchronous or asynchronous operation
- Timer1 gate (count enable) via comparator or T1G pin
- Interrupt on overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- Time base for the Capture/Compare function
- Special Event Trigger (with ECCP)
- Comparator output synchronization to Timer1 clock

Figure 6-1 is a block diagram of the Timer1 module.

TMR1GE T1GINV TMR10N Set flag bit TMR1IF on To C2 Comparator Module Overflow Timer1 Clock TMR1⁽²⁾ Synchronized 0 ΕN clock input TMR1H TMR1L Oscillator (1) T1SYNC T1OSO/T1CKI 1 Synchronize⁽³⁾ Prescaler 1, 2, 4, 8 det 0 T10SI 🖹 2 T1CKPS<1:0> TMR1CS TIG > 1 INTOSC SYNCC2OUT(4) 0 Without CLKOUT T1OSCEN Fosc/4 T1GSS Internal Clock ST Buffer is low power type when using LP osc, or high speed type when using T1CKI. Note 1: 2: Timer1 register increments on rising edge. Synchronize does not operate while in Sleep. 3: 4: SYNCC2OUT is synchronized when the C2SYNC bit of the CM2CON1 register is set.

FIGURE 6-1: TIMER1 BLOCK DIAGRAM

6.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing counter which is accessed through the TMR1H:TMR1L register pair. Writes to TMR1H or TMR1L directly update the counter.

When used with an internal clock source, the module is a timer. When used with an external clock source, the module can be used as either a timer or counter.

6.2 Clock Source Selection

The TMR1CS bit of the T1CON register is used to select the clock source. When TMR1CS = 0, the clock source is FOSC/4. When TMR1CS = 1, the clock source is supplied externally.

Clock Source	TMR1CS
Fosc/4	0
T1CKI pin	1

8.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. The comparators are very useful mixed signal building blocks because they provide analog functionality independent of the program execution. The analog comparator module includes the following features:

- Independent comparator control
- Programmable input selection
- · Comparator output is available internally/externally
- Programmable output polarity
- Interrupt-on-change
- Wake-up from Sleep
- PWM shutdown
- Timer1 gate (count enable)
- Output synchronization to Timer1 clock input
- SR Latch
- Programmable and Fixed Voltage Reference

Note: Only Comparator C2 can be linked to Timer1.

8.1 Comparator Overview

A single comparator is shown in Figure 8-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.



8.10 Comparator Voltage Reference

The comparator voltage reference module provides an internally generated voltage reference for the comparators. The following features are available:

- Independent from Comparator operation
- Two 16-level voltage ranges
- Output clamped to Vss
- Ratiometric with VDD
- Fixed Reference (0.6V)

The VRCON register (Register 8-5) controls the voltage reference module shown in Figure 8-8.

The voltage source is selectable through both ends of the 16 connection resistor ladder network. Bit VRSS of the VRCON register selects either the internal or external voltage source.

The PIC16F882/883/884/886/887 allows the CVREF signal to be output to the RA2 pin of PORTA under certain configurations only. For more details, see Figure 8-9.

8.10.1 INDEPENDENT OPERATION

The comparator voltage reference is independent of the comparator configuration. Setting the VREN bit of the VRCON register will enable the voltage reference.

8.10.2 OUTPUT VOLTAGE SELECTION

The CVREF voltage reference has two ranges with 16 voltage levels in each range. Range selection is controlled by the VRR bit of the VRCON register. The 16 levels are set with the VR<3:0> bits of the VRCON register.

The CVREF output voltage is determined by the following equations:

EQUATION 8-1: CVREF OUTPUT VOLTAGE

VRR = 1 (low range): CVREF = (VR<3:0>/24) × VLADDER VRR = 0 (high range): CVREF = (VLADDER/4) + (VR<3:0> × VLADDER/32) VLADDER = VDD or ([VREF+] - [VREF-]) or VREF+

The full range of VSS to VDD cannot be realized due to the construction of the module. See Figure 8-8.

8.10.3 OUTPUT CLAMPED TO Vss

The CVREF output voltage can be set to Vss with no power consumption by clearing the FVREN bit of the VRCON register.

This allows the comparator to detect a zero-crossing while not consuming additional CVREF module current.

Note: Depending on the application, additional components may be required for a zero cross circuit. Reference TB3013, *"Using the ESD Parasitic Diodes on Mixed Signal Microcontrollers"* (DS93013), for more information.

8.10.4 OUTPUT RATIOMETRIC TO VDD

The comparator voltage reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the Comparator Voltage Reference can be found in **Section 17.0 "Electrical Specifications"**.

8.10.5 FIXED VOLTAGE REFERENCE

The Fixed Voltage Reference is independent of VDD, with a nominal output voltage of 0.6V. This reference can be enabled by setting the FVREN bit of the SRCON register to '1'. This reference is always enabled when the HFINTOSC oscillator is active.

8.10.6 FIXED VOLTAGE REFERENCE STABILIZATION PERIOD

When the Fixed Voltage Reference module is enabled, it will require some time for the reference and its amplifier circuits to stabilize. The user program must include a small delay routine to allow the module to settle. See **Section 17.0 "Electrical Specifications"** for the minimum delay requirement.

8.10.7 VOLTAGE REFERENCE SELECTION

Multiplexers on the output of the voltage reference module enable selection of either the CVREF or Fixed Voltage Reference for use by the comparators.

Setting the C1RSEL bit of the CM2CON1 register enables current to flow in the CVREF voltage divider and selects the CVREF voltage for use by C1. Clearing the C1RSEL bit selects the fixed voltage for use by C1.

Setting the C2RSEL bit of the CM2CON1 register enables current to flow in the CVREF voltage divider and selects the CVREF voltage for use by C2. Clearing the C2RSEL bit selects the fixed voltage for use by C2.

When both the C1RSEL and C2RSEL bits are cleared, current flow in the CVREF voltage divider is disabled minimizing the power drain of the voltage reference peripheral.



FIGURE 8-8: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

FIGURE 8-9: COMPARATOR AND ADC VOLTAGE REFERENCE BLOCK DIAGRAM



10.2 Writing to Flash Program Memory

Flash program memory may only be written to if the destination address is in a segment of memory that is not write-protected, as defined in bits WRT<1:0> of the Configuration Word Register 2. Flash program memory must be written in 8-word blocks (4-word blocks for 4K memory devices). See Figures 10-2 and 10-3 for more details. A block consists of eight words with sequential addresses, with a lower boundary defined by an address, where EEADR<2:0> = 000. All block writes to program memory are done as 16-word erase by 8-word write operations. The write operation is edge-aligned and cannot occur across boundaries.

To write program data, it must first be loaded into the buffer registers (see Figure 10-2). This is accomplished by first writing the destination address to EEADR and EEADRH and then writing the data to EEDATA and EEDATH. After the address and data have been set up, then the following sequence of events must be executed:

- 1. Set the EEPGD control bit of the EECON1 register.
- 2. Write 55h, then AAh, to EECON2 (Flash programming sequence).
- 3. Set the WR control bit of the EECON1 register.

All eight buffer register locations should be written to with correct data. If less than eight words are being written to in the block of eight words, then a read from the program memory location(s) not being written to must be performed. This takes the data from the program location(s) not being written and loads it into the EEDATA and EEDATH registers. Then the sequence of events to transfer data to the buffer registers must be executed.

To transfer data from the buffer registers to the program memory, the EEADR and EEADRH must point to the last location in the 8-word block (EEADR<2:0> = 111). Then the following sequence of events must be executed:

- 1. Set the EEPGD control bit of the EECON1 register.
- 2. Write 55h, then AAh, to EECON2 (Flash programming sequence).
- 3. Set control bit WR of the EECON1 register to begin the write operation.

The user must follow the same specific sequence to initiate the write for each word in the program block, writing each program word in sequence (000, 001, 010, 011, 100, 101, 110, 111). When the write is performed on the last word (EEADR<2:0> = 111), a block of sixteen words is automatically erased and the content of the 8-word buffer registers are written into the program memory.

After the "BSF EECON1, WR" instruction, the processor requires two cycles to set up the erase/write operation. The user must place two NOP instructions after the WR bit is set. Since data is being written to buffer registers, the writing of the first seven words of the block appears to occur immediately. The processor will halt internal operations for the typical 4 ms, only during the cycle in which the erase takes place (i.e., the last word of the sixteen-word block erase). This is not Sleep mode as the clocks and peripherals will continue to run. After the 8-word write cycle, the processor will resume operation with the third instruction after the EECON1 write instruction. The above sequence must be repeated for the higher eight words.

11.5.4 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCPx pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

11.5.5 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See Section 4.0 "Oscillator Module (With Fail-Safe Clock Monitor)" for additional details.

11.5.6 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

11.5.7 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

- 1. Disable the PWM pin (CCPx) output drivers as an input by setting the associated TRIS bit.
- 2. Set the PWM period by loading the PR2 register.
- Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.
- Set the PWM duty cycle by loading the CCPRxL register and DCxB<1:0> bits of the CCPxCON register.
- 5. Configure and start Timer2:
 - Clear the TMR2IF interrupt flag bit of the PIR1 register.
 - Set the Timer2 prescale value by loading the T2CKPS bits of the T2CON register.
 - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
- 6. Enable PWM output after a new PWM cycle has started:
 - Wait until Timer2 overflows (TMR2IF bit of the PIR1 register is set).
 - Enable the CCPx pin output driver by clearing the associated TRIS bit.

FIGURE 11-6: EXAMPLE PWM (ENHANCED MODE) OUTPUT RELATIONSHIPS (ACTIVE-HIGH STATE)

			'			'
00	(Single Output)	PTA Modulated	Dela	_{ly} (1)	Delay ⁽¹⁾	!
		P1A Modulated			→	
10	(Half-Bridge)	P1B Modulated	'			
		P1A Active				<u> </u>
01	(Full-Bridge,	P1B Inactive			1 1 1	
01	Forward)	P1C Inactive				
		P1D Modulated			<u> </u>	1
		P1A Inactive			1 1 1	
11	(Full-Bridge,	P1B Modulated				; ;
	Reverse)	P1C Active				,
		P1D Inactive	_ : _			
Relat	tionships: • Period = 4 * Tos • Pulse Width = To	c * (PR2 + 1) * (TMR2 Pre osc * (CCPR1L<7:0>:CCF	escale Value) P1CON<5:4>) '	* (TMR2 Prescal	e Value)	

13.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP) MODULE

13.1 Master SSP (MSSP) Module Overview

The Master Synchronous Serial Port (MSSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit[™] (I²C[™])
 - Full Master mode
 - Slave mode (with general address call).

The I^2C interface supports the following modes in hardware:

- Master mode
- Multi-Master mode
- Slave mode.

13.2 Control Registers

The MSSP module has three associated registers. These include a STATUS register and two control registers.

Register 13-1 shows the MSSP STATUS register (SSPSTAT), Register 13-2 shows the MSSP Control Register 1 (SSPCON), and Register 13-3 shows the MSSP Control Register 2 (SSPCON2).

REGISTER 13-1: SSPSTAT: SSP STATUS REGISTER

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/Ā	Р	S	R/W	UA	BF
bit 7							bit 0
Legend:							
R = Readable bit		W = Writable bit		U = Unimplem	ented bit, read as	'0'	
-n = Value at POF	२	'1' = Bit is set		'0' = Bit is clea	ired	x = Bit is unknov	vn
bit 7	SMP: Sample b	it <u>le:</u>					
	1 = Input data s 0 = Input data s	ampled at end of ampled at middle	data output tim of data output	ie time			
	SMP must be cl	<u>.</u> leared when SPI i	s used in Slave	e mode			
	$\frac{\ln I^2 C \text{ Master or}}{1} = \text{Slew rate of}$	<u>Slave mode:</u> control disabled for	r standard spe	ed mode (100 kH	lz and 1 MHz)		
h # C	0 = Slew rate c	control enabled for	high speed m	ode (400 kHz)			
DIT 6		Lage Select bit					
	1 = Data transm 0 = Data transm	nitted on falling ed nitted on rising edg	ge of SCK ge of SCK				
	$\frac{\text{CKP} = 1:}{1 = \text{Data transm}}$ $0 = \text{Data transm}$	nitted on rising edg	ge of SCK				
bit 5	D/A: Data/Addr 1 = Indicates the $0 = $ Indicates the	ess bit (I ² C mode at the last byte rec	only) ceived or trans	mitted was data	acc.		
bit 4	P: Stop bit						
	(I ² C mode only. 1 = Indicates the 0 = Stop bit was	This bit is cleared at a Stop bit has b s not detected last	d when the MS been detected I	SP module is dis ast (this bit is '0'	abled, SSPEN is c on Reset)	leared.)	
bit 3	S: Start bit						
	 (I²C mode only. 1 = Indicates the 0 = Start bit was 	This bit is cleared at a Start bit has b s not detected last	d when the MS been detected l	SP module is dis ast (this bit is '0'	abled, SSPEN is c on Reset)	leared.)	
bit 2	R/W: Read/Writ	e bit information (I ² C mode only)			
	This bit holds th the next Start bi In I^2C Slave mo 1 = Read	e R/W bit informa t, Stop bit, or not / <u>de:</u>	<u>tion f</u> ollowing tl ACK bit.	ne last address m	natch. This bit is or	ily valid from the a	ddress match to
	0 = Write						
	$ln l^2C$ Master m 1 = Transmit is	i <u>ode:</u> s in progress					
	0 = Transmit is OR-ing thi	s not in progress	SEN, PEN, RC	EN, or ACKEN w	vill indicate if the M	ISSP is in Idle mod	de.
bit 1	UA: Update Ade	dress bit (10-bit I ²	C mode only)				
	1 = Indicates the 0 = Address doe	at the user needs es not need to be	to update the a updated	address in the SS	SPADD register		
bit 0	BF: Buffer Full	Status bit					
	<u>Receive (SPI ar</u> 1 = Receive cor	<u>nd I[∠]C modes):</u> nplete, SSPBUF i	s full				
	0 = Receive not	complete, SSPB	UF is empty				
	<u>Transmit (l^2C m</u> 1 = Data transm 0 = Data transm	iode only): hit in progress (does hit complete (does	es not include	the ACK and Sto	p bits), SSPBUF is bits), SSPBUF is e	s full	

14.5 Watchdog Timer (WDT)

The WDT has the following features:

- Operates from the LFINTOSC (31 kHz)
- · Contains a 16-bit prescaler
- Shares an 8-bit prescaler with Timer0
- Time-out period is from 1 ms to 268 seconds
- · Configuration bit and software controlled

WDT is cleared under certain conditions described in Table 14-7.

14.5.1 WDT OSCILLATOR

The WDT derives its time base from the 31 kHz LFINTOSC. The LTS bit of the OSCCON register does not reflect that the LFINTOSC is enabled.

The value of WDTCON is '---0 1000' on all Resets. This gives a nominal time base of 17 ms.

Note: When the Oscillator Start-up Timer (OST) is invoked, the WDT is held in Reset, because the WDT Ripple Counter is used by the OST to perform the oscillator delay count. When the OST count has expired, the WDT will begin counting (if enabled).

FIGURE 14-9: WATCHDOG TIMER BLOCK DIAGRAM



WDT CONTROL

The WDTE bit is located in the Configuration Word

When the WDTE bit in the Configuration Word

Register 1 is set, the SWDTEN bit of the WDTCON

register has no effect. If WDTE is clear, then the

SWDTEN bit can be used to enable and disable the

WDT. Setting the bit will enable it and clearing the bit

The PSA and PS<2:0> bits of the OPTION register have the same function as in previous versions of the

PIC16F882/883/884/886/887 family of microcontrollers. See Section 5.0 "Timer0 Module" for more

Register 1. When set, the WDT runs continuously.

14.5.2

will disable it.

information.

TABLE 14-7: WDT STATUS

Conditions	WDT
WDTE = 0	Cleared
CLRWDT Command	
Oscillator Fail Detected	
Exit Sleep + System Clock = T1OSC, EXTRC, INTOSC, EXTCLK	
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST

16.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

16.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

16.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a highspeed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

16.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a fullspeed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming[™] (ICSP[™]).

16.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.



FIGURE 18-47: TYPICAL VP6 REFERENCE VOLTAGE DISTRIBUTION (3V, 85°C)







FIGURE 18-50: TYPICAL VP6 REFERENCE VOLTAGE DISTRIBUTION (5V, 25°C)

