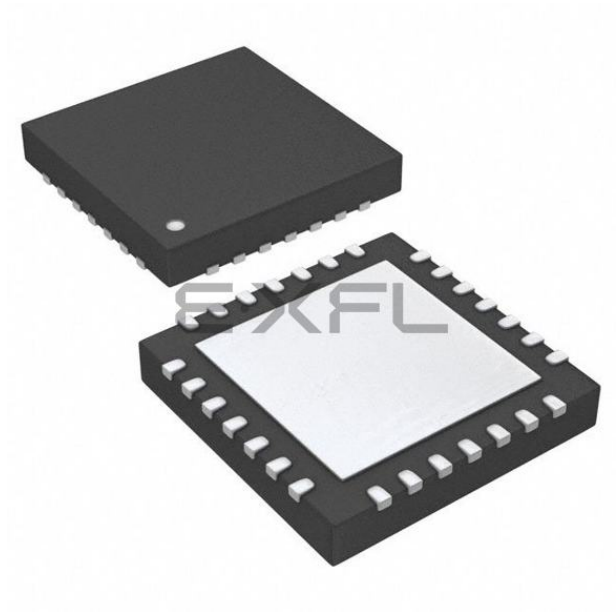

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## What is "Embedded - Microcontrollers"?

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 24 |
| Program Memory Size | 14KB (8K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | 256 x 8 |
| RAM Size | 368 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V |
| Data Converters | A/D 11x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-VQFN Exposed Pad |
| Supplier Device Package | 28-QFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16f886t-i-ml |

**TABLE 1: 28-PIN PDIP, SOIC, SSOP ALLOCATION TABLE (PIC16F882/883/886)**

| I/O | 28-Pin PDIP/SOIC/SSOP | Analog | Comparators | Timers | ECCP | EUSART | MSSP | Interrupt | Pull-up | Basic |
|---|---|---|---|---|---|---|---|---|---|---|
| RA0 | 2 | AN0/ULPWU | C12IN0- | — | — | — | — | — | — | — |
| RA1 | 3 | AN1 | C12IN1- | — | — | — | — | — | — | — |
| RA2 | 4 | AN2 | C2IN+ | — | — | — | — | — | — | VREF-/CVREF |
| RA3 | 5 | AN3 | C1IN+ | — | — | — | — | — | — | VREF+ |
| RA4 | 6 | — | C1OUT | T0CKI | — | — | — | — | — | — |
| RA5 | 7 | AN4 | C2OUT | — | — | — | $\overline{SS}$ | — | — | — |
| RA6 | 10 | — | — | — | — | — | — | — | — | OSC2/CLKOUT |
| RA7 | 9 | — | — | — | — | — | — | — | — | OSC1/CLKIN |
| RB0 | 21 | AN12 | — | — | — | — | — | IOC/INT | Y | — |
| RB1 | 22 | AN10 | C12IN3- | — | P1C | — | — | IOC | Y | — |
| RB2 | 23 | AN8 | — | — | P1B | — | — | IOC | Y | — |
| RB3 | 24 | AN9 | C12IN2- | — | — | — | — | IOC | Y | PGM |
| RB4 | 25 | AN11 | — | — | P1D | — | — | IOC | Y | — |
| RB5 | 26 | AN13 | — | $\overline{T1G}$ | — | — | — | IOC | Y | — |
| RB6 | 27 | — | — | — | — | — | — | IOC | Y | ICSPCLK |
| RB7 | 28 | — | — | — | — | — | — | IOC | Y | ICSPDAT |
| RC0 | 11 | — | — | T1OSO/T1CKI | — | — | — | — | — | — |
| RC1 | 12 | — | — | T1OSI | CCP2 | — | — | — | — | — |
| RC2 | 13 | — | — | — | CCP1/P1A | — | — | — | — | — |
| RC3 | 14 | — | — | — | — | — | SCK/SCL | — | — | — |
| RC4 | 15 | — | — | — | — | — | SDI/SDA | — | — | — |
| RC5 | 16 | — | — | — | — | — | SDO | — | — | — |
| RC6 | 17 | — | — | — | — | TX/CK | — | — | — | — |
| RC7 | 18 | — | — | — | — | RX/DT | — | — | — | — |
| RE3 | 1 | — | — | — | — | — | — | — | Y(1) | $\overline{MCLR}$/VPP |
| — | 20 | — | — | — | — | — | — | — | — | VDD |
| — | 8 | — | — | — | — | — | — | — | — | VSS |
| — | 19 | — | — | — | — | — | — | — | — | VSS |

**Note 1:** Pull-up activated only with external $\overline{MCLR}$ configuration.

**Pin Diagrams – PIC16F882/883/886, 28-Pin QFN**

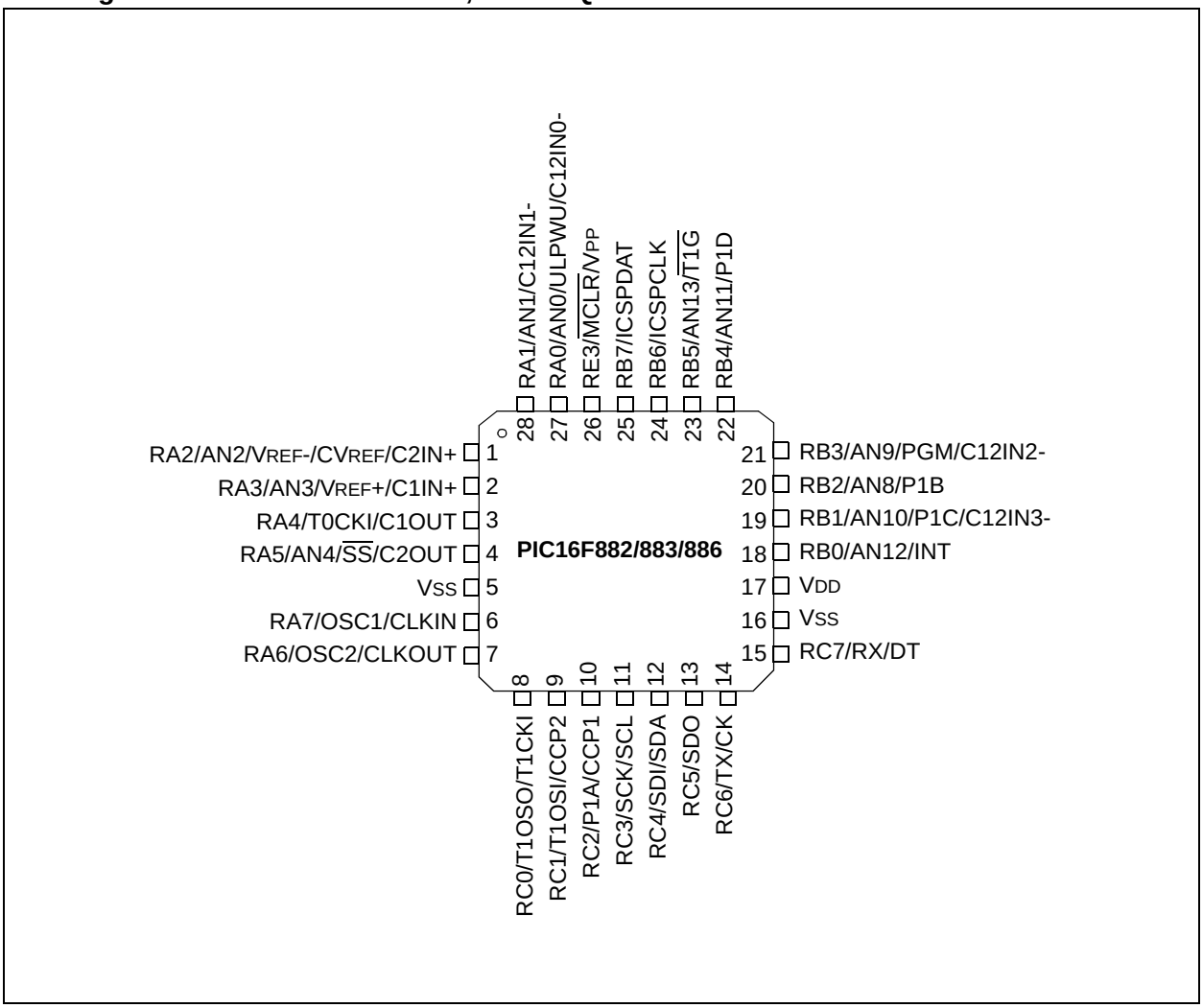


**TABLE 1-2: PIC16F884/887 PINOUT DESCRIPTION (CONTINUED)**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| RB4/AN11 | RB4 | TTL | CMOS | General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up. |
| | AN11 | AN | — | A/D Channel 11. |
| RB5/AN13/$\overline{T1G}$ | RB5 | TTL | CMOS | General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up. |
| | AN13 | AN | — | A/D Channel 13. |
| | $\overline{T1G}$ | ST | — | Timer1 Gate input. |
| RB6/ICSPCLK | RB6 | TTL | CMOS | General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up. |
| | ICSPCLK | ST | — | Serial Programming Clock. |
| RB7/ICSPDAT | RB7 | TTL | CMOS | General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up. |
| | ICSPDAT | ST | TTL | ICSP™ Data I/O. |
| RC0/T1OSO/T1CKI | RC0 | ST | CMOS | General purpose I/O. |
| | T1OSO | — | XTAL | Timer1 oscillator output. |
| | T1CKI | ST | — | Timer1 clock input. |
| RC1/T1OSI/CCP2 | RC1 | ST | CMOS | General purpose I/O. |
| | T1OSI | XTAL | — | Timer1 oscillator input. |
| | CCP2 | ST | CMOS | Capture/Compare/PWM2. |
| RC2/P1A/CCP1 | RC2 | ST | CMOS | General purpose I/O. |
| | P1A | ST | CMOS | PWM output. |
| | CCP1 | — | CMOS | Capture/Compare/PWM1. |
| RC3/SCK/SCL | RC3 | ST | CMOS | General purpose I/O. |
| | SCK | ST | CMOS | SPI clock. |
| | SCL | ST | OD | $I^2C$™ clock. |
| RC4/SDI/SDA | RC4 | ST | CMOS | General purpose I/O. |
| | SDI | ST | — | SPI data input. |
| | SDA | ST | OD | $I^2C$ data input/output. |
| RC5/SDO | RC5 | ST | CMOS | General purpose I/O. |
| | SDO | — | CMOS | SPI data output. |
| RC6/TX/CK | RC6 | ST | CMOS | General purpose I/O. |
| | TX | — | CMOS | EUSART asynchronous transmit. |
| | CK | ST | CMOS | EUSART synchronous clock. |
| RC7/RX/DT | RC7 | ST | CMOS | General purpose I/O. |
| | RX | ST | — | EUSART asynchronous input. |
| | DT | ST | CMOS | EUSART synchronous data. |
| RD0 | RD0 | TTL | CMOS | General purpose I/O. |
| RD1 | RD1 | TTL | CMOS | General purpose I/O. |
| RD2 | RD2 | TTL | CMOS | General purpose I/O. |
| RD3 | RD3 | TTL | CMOS | General purpose I/O. |
| RD4 | RD4 | TTL | CMOS | General purpose I/O. |
| RD5/P1B | RD5 | TTL | CMOS | General purpose I/O. |
| | P1B | — | CMOS | PWM output. |
| RD6/P1C | RD6 | TTL | CMOS | General purpose I/O. |
| | P1C | — | CMOS | PWM output. |

**Legend:** AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels
HV = High Voltage XTAL = Crystal

### 2.2.2.3 INTCON Register

The INTCON register, shown in Register 2-3, is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, PORTB change and external INT pin interrupts.

| | |
|---|---|
| **Note:** | Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. |

## REGISTER DEFINITIONS: INTERRUPT CONTROL

**REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-x |
|---|---|---|---|---|---|---|---|
| GIE | PEIE | T0IE | INTE | RBIE(1) | T0IF(2) | INTF | RBIF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **T0IE:** Timer0 Overflow Interrupt Enable bit
1 = Enables the Timer0 interrupt
0 = Disables the Timer0 interrupt

bit 4 **INTE:** INT External Interrupt Enable bit
1 = Enables the INT external interrupt
0 = Disables the INT external interrupt

bit 3 **RBIE:** PORTB Change Interrupt Enable bit(1)
1 = Enables the PORTB change interrupt
0 = Disables the PORTB change interrupt

bit 2 **T0IF:** Timer0 Overflow Interrupt Flag bit(2)
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INTF:** INT External Interrupt Flag bit
1 = The INT external interrupt occurred (must be cleared in software)
0 = The INT external interrupt did not occur

bit 0 **RBIF:** PORTB Change Interrupt Flag bit
1 = When at least one of the PORTB general purpose I/O pins changed state (must be cleared in software)
0 = None of the PORTB general purpose I/O pins have changed state

**Note 1:** IOCB register must also be enabled.
**2:** T0IF bit is set when Timer0 rolls over. Timer0 is unchanged on Reset and should be initialized before clearing T0IF bit.

#### 2.2.2.8 PCON Register

The Power Control (PCON) register (see Register 2-8) contains flag bits to differentiate between a:

- Power-on Reset ($\overline{POR}$)
- Brown-out Reset ($\overline{BOR}$)
- Watchdog Timer Reset (WDT)
- External $\overline{MCLR}$ Reset

The PCON register also controls the Ultra Low-Power Wake-up and software enable of the $\overline{BOR}$.

## REGISTER DEFINITIONS: PCON

**REGISTER 2-8: PCON: POWER CONTROL REGISTER**

| U-0 | U-0 | R/W-0 | R/W-1 | U-0 | U-0 | R/W-0 | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | ULPWUE | SBOREN(1) | — | — | $\overline{POR}$ | $\overline{BOR}$ |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **ULPWUE:** Ultra Low-Power Wake-up Enable bit
1 = Ultra Low-Power Wake-up enabled
0 = Ultra Low-Power Wake-up disabled

bit 4 **SBOREN:** Software BOR Enable bit(1)
1 = BOR enabled
0 = BOR disabled

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1 **$\overline{POR}$:** Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

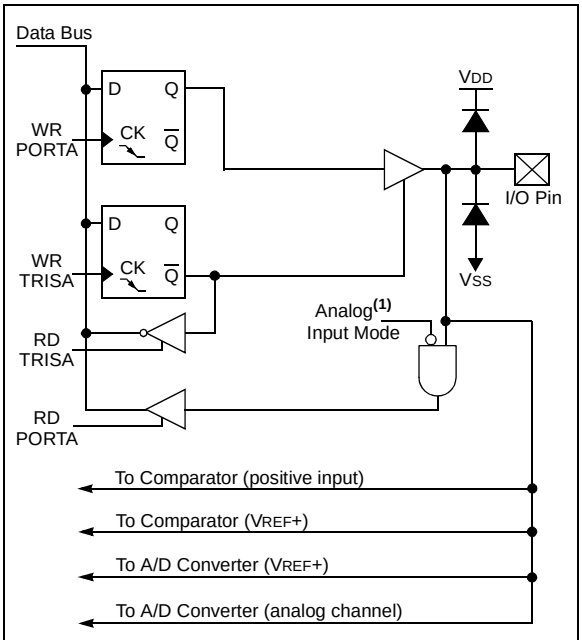
**Note 1:** BOREN<1:0> = 01 in the Configuration Word Register 1 for this bit to control the $\overline{BOR}$.

### 3.2.3.4 RA3/AN3/VREF+/C1IN+

Figure 3-4 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose input
- an analog input for the ADC
- a positive voltage reference input for the ADC and CVREF
- a positive analog input to Comparator C1

**FIGURE 3-4: BLOCK DIAGRAM OF RA3**



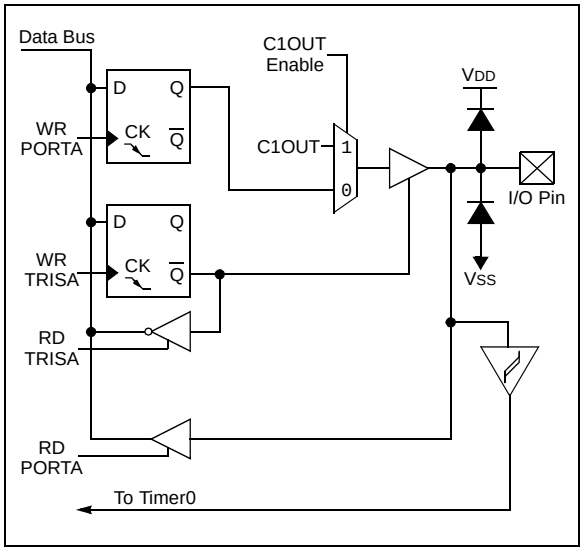

**Note 1:** ANSEL determines Analog Input mode.

### 3.2.3.5 RA4/T0CKI/C1OUT

Figure 3-5 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- a clock input for Timer0
- a digital output from Comparator C1

**FIGURE 3-5: BLOCK DIAGRAM OF RA4**

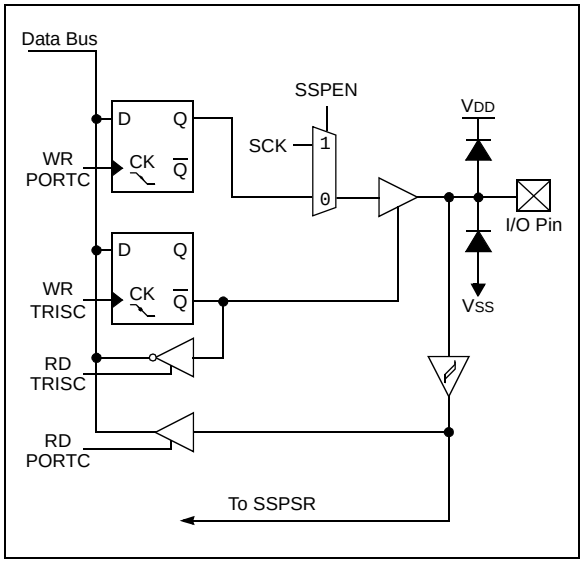


### 3.5.4 RC3/SCK/SCL

Figure 3-14 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- a SPI clock
- an $I^2C$™ clock

**FIGURE 3-14: BLOCK DIAGRAM OF RC3**

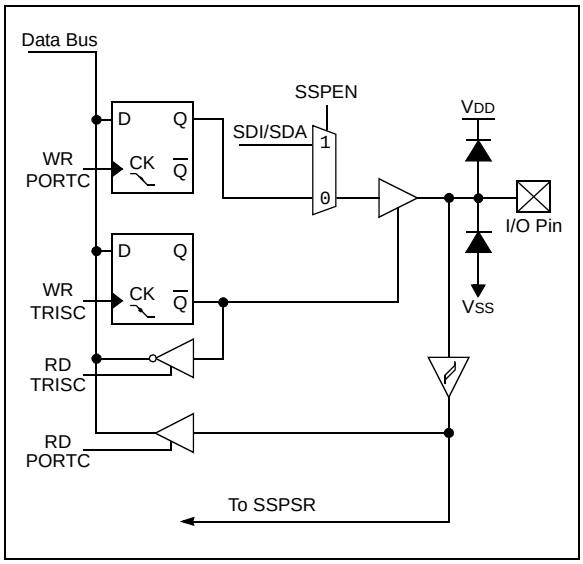



### 3.5.5 RC4/SDI/SDA

Figure 3-15 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- a SPI data I/O
- an $I^2C$ data I/O

**FIGURE 3-15: BLOCK DIAGRAM OF RC4**

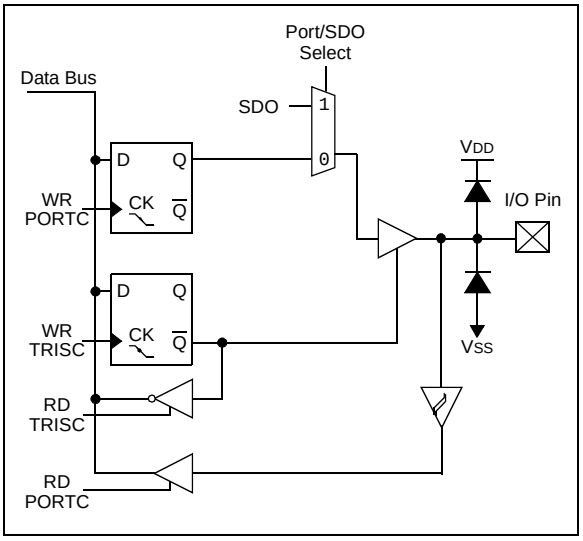



### 3.5.6 RC5/SDO

Figure 3-16 shows the diagram for this pin. This pin is configurable to function as one of the following:

- a general purpose I/O
- a serial data output

**FIGURE 3-16: BLOCK DIAGRAM OF RC5**



### 4.4.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 4-3). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

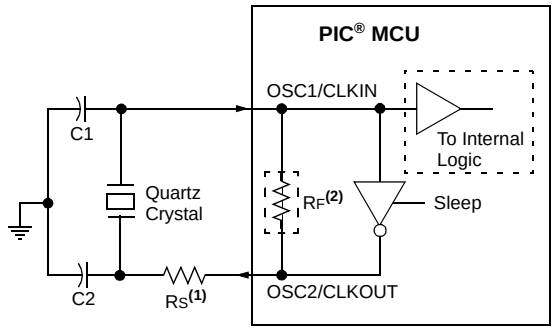
**LP** Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

**XT** Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

**HS** Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 4-3 and Figure 4-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

**FIGURE 4-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)**




**Note 1:** A series resistor (RS) may be required for quartz crystals with low drive level.

**2:** The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

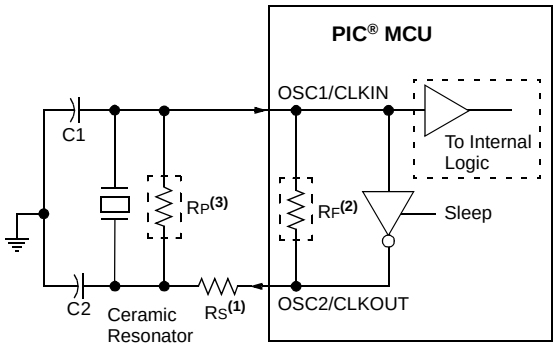
**Note 1:** Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

**2:** Always verify oscillator performance over the VDD and temperature range that is expected for the application.

**3:** For oscillator design assistance, reference the following Microchip Applications Notes:

- AN826, "*Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices*" (DS00826)
- AN849, "*Basic PIC® Oscillator Design*" (DS00849)
- AN943, "*Practical PIC® Oscillator Analysis and Design*" (DS00943)
- AN949, "*Making Your Oscillator Work*" (DS00949)

**FIGURE 4-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)**




**Note 1:** A series resistor (RS) may be required for ceramic resonators with low drive level.

**2:** The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

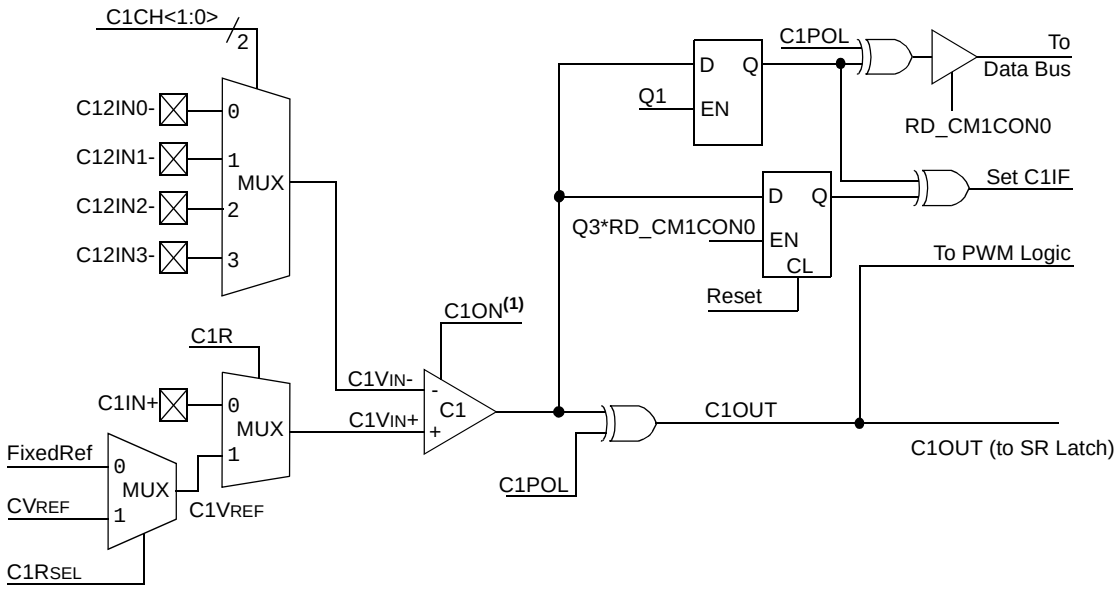
**3:** An additional parallel feedback resistor (RP) may be required for proper ceramic resonator operation.

**TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|
| CM2CON1 | MC1OUT | MC2OUT | C1RSEL | C2RSEL | — | — | T1GSS | C2SYNC | 92 |
| INTCON | GIE | PEIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 32 |
| PIE1 | — | ADIE | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMR1IE | 33 |
| PIR1 | — | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF | 35 |
| TMR1H | Holding Register for the Most Significant Byte of the 16-bit TMR1 Register | | | | | | | | 78 |
| TMR1L | Holding Register for the Least Significant Byte of the 16-bit TMR1 Register | | | | | | | | 78 |
| T1CON | T1GINV | TMR1GE | T1CKPS1 | T1CKPS0 | T1OSCEN | $\overline{\text{T1SYNC}}$ | TMR1CS | TMR1ON | 81 |

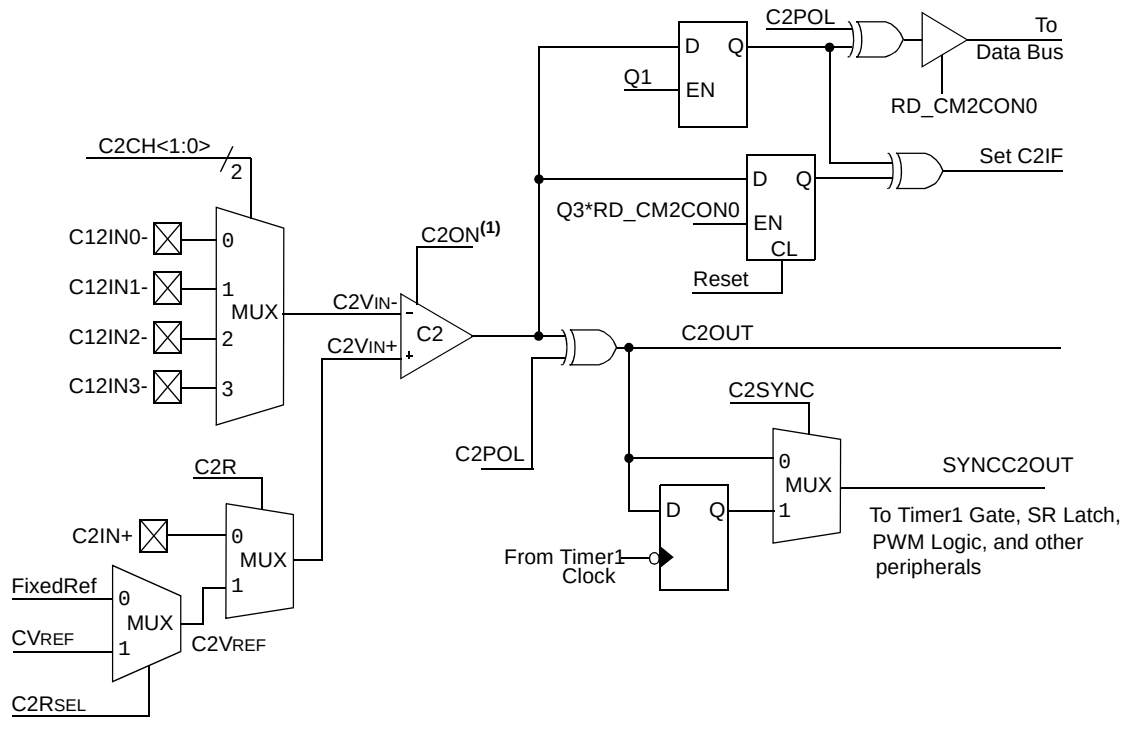
**Legend:** x = unknown, u = unchanged, – = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

**FIGURE 8-2: COMPARATOR C1 SIMPLIFIED BLOCK DIAGRAM**




**Note 1:** When C1ON = 0, the C1 comparator will produce a '0' output to the XOR Gate.
**2:** Q1 and Q3 are phases of the four-phase system clock (FOSC).
**3:** Q1 is held high during Sleep mode.

**FIGURE 8-3: COMPARATOR C2 SIMPLIFIED BLOCK DIAGRAM**




**Note 1:** When C2ON = 0, the C2 comparator will produce a '0' output to the XOR Gate.
**2:** Q1 and Q3 are phases of the four-phase system clock (FOSC).
**3:** Q1 is held high during Sleep mode.

### 9.2.6 A/D CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure Port:
   - Disable pin output driver (See TRIS register)
   - Configure pin as analog
2. Configure the ADC module:
   - Select ADC conversion clock
   - Configure voltage reference
   - Select ADC input channel
   - Select result format
   - Turn on ADC module
3. Configure ADC interrupt (optional):
   - Clear ADC interrupt flag
   - Enable ADC interrupt
   - Enable peripheral interrupt
   - Enable global interrupt**(1)**
4. Wait the required acquisition time**(2)**.
5. Start conversion by setting the GO/$\overline{\text{DONE}}$ bit.
6. Wait for ADC conversion to complete by one of the following:
   - Polling the GO/$\overline{\text{DONE}}$ bit
   - Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC Result
8. Clear the ADC interrupt flag (required if interrupt is enabled).

**Note 1:** The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

**2:** See **Section 9.3 "A/D Acquisition Requirements"**.

**EXAMPLE 9-1: A/D CONVERSION**

```
;This code block configures the ADC
;for polling, Vdd and Vss as reference, Frc
clock and AN0 input.
;
;Conversion start & polling for completion
; are included.
;
BANKSEL   ADCON1       ;
MOVLW     B'10000000'  ;right justify
MOVWF     ADCON1       ;Vdd and Vss as Vref
BANKSEL   TRISA        ;
BSF       TRISA,0      ;Set RA0 to input
BANKSEL   ANSEL        ;
BSF       ANSEL,0      ;Set RA0 to analog
BANKSEL   ADCON0       ;
MOVLW     B'11000001'  ;ADC Frc clock,
MOVWF     ADCON0       ;AN0, On
CALL      SampleTime   ;Acquisiton delay
BSF       ADCON0,GO    ;Start conversion
BTFSC     ADCON0,GO    ;Is conversion done?
GOTO      $-1          ;No, test again
BANKSEL   ADRESH       ;
MOVF      ADRESH,W     ;Read upper 2 bits
MOVWF     RESULTHI     ;store in GPR space
BANKSEL   ADRESL       ;
MOVF      ADRESL,W     ;Read lower 8 bits
MOVWF     RESULTLO     ;Store in GPR space
```

### 10.1.2 READING THE DATA EEPROM MEMORY

To read a data memory location, the user must write the address to the EEADR register, clear the EEPGD control bit of the EECON1 register, and then set control bit RD. The data is available at the very next cycle, in the EEDAT register; therefore, it can be read in the next instruction. EEDAT will hold this value until another read or until it is written to by the user (during a write operation).

**EXAMPLE 10-1: DATA EEPROM READ**

```
BANKSEL  EEADR          ;
MOVLW    DATA_EE_ADDR   ;
MOVWF    EEADR          ;Data Memory
                        ;Address to read
BANKSEL  EECON1         ;
BCF      EECON1, EEPGD  ;Point to DATA memory
BSF      EECON1, RD     ;EE Read
BANKSEL  EEDAT          ;
MOVF     EEDAT, W       ;W = EEDAT
BCF      STATUS, RP1    ;Bank 0
```

### 10.1.3 WRITING TO THE DATA EEPROM MEMORY

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDAT register. Then the user must follow a specific sequence to initiate the write for each byte.

The write will not initiate if the above sequence is not followed exactly (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. Interrupts should be disabled during this code segment.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. EEIF must be cleared by software.

**EXAMPLE 10-2: DATA EEPROM WRITE**

```
        BANKSEL  EEADR          ;
        MOVLW    DATA_EE_ADDR   ;
        MOVWF    EEADR          ;Data Memory Address to write
        MOVLW    DATA_EE_DATA   ;
        MOVWF    EEDAT          ;Data Memory Value to write
        BANKSEL  EECON1         ;
        BCF      EECON1, EEPGD  ;Point to DATA memory
        BSF      EECON1, WREN   ;Enable writes

        BCF      INTCON, GIE    ;Disable INTs.
        BTFSC    INTCON, GIE    ;SEE AN576
        GOTO     $-2
Required
Sequence
        MOVLW    55h            ;
        MOVWF    EECON2         ;Write 55h
        MOVLW    AAh            ;
        MOVWF    EECON2         ;Write AAh
        BSF      EECON1, WR     ;Set WR bit to begin write
        BSF      INTCON, GIE    ;Enable INTs.

        SLEEP                   ;Wait for interrupt to signal write complete
        BCF      EECON1, WREN   ;Disable writes
        BCF      STATUS, RP0    ;Bank 0
        BCF      STATUS, RP1
```

### 10.1.4 READING THE FLASH PROGRAM MEMORY

To read a program memory location, the user must write the Least and Most Significant address bits to the EEADR and EEADRH registers, set the EEPGD control bit of the EECON1 register, and then set control bit RD. Once the read control bit is set, the program memory Flash controller will use the second instruction cycle to read the data. This causes the second instruction immediately following the "BSF EECON1,RD" instruction to be ignored. The data is available in the very next cycle, in the EEDAT and EEDATH registers; therefore, it can be read as two bytes in the following instructions.

EEDAT and EEDATH registers will hold this value until another read or until it is written to by the user.

**Note 1:** The two instructions following a program memory read are required to be NOPs. This prevents the user from executing a 2-cycle instruction on the next instruction after the RD bit is set.

**2:** If the WR bit is set when EEPGD = 1, it will be immediately reset to '0' and no operation will take place.

**EXAMPLE 10-3: FLASH PROGRAM READ**

```
    BANKSEL EEADR               ;
    MOVLW   MS_PROG_EE_ADDR     ;
    MOVWF   EEADRH              ;MS Byte of Program Address to read
    MOVLW   LS_PROG_EE_ADDR     ;
    MOVWF   EEADR               ;LS Byte of Program Address to read
    BANKSEL EECON1              ;
    BSF     EECON1, EEPGD       ;Point to PROGRAM memory
    BSF     EECON1, RD          ;EE Read
                                ;
                                ;First instruction after BSF EECON1,RD executes normally
    NOP
    NOP                         ;Any instructions here are ignored as program
                                ;memory is read in second cycle after BSF EECON1,RD
;
    BANKSEL EEDAT               ;
    MOVF    EEDAT, W            ;W = LS Byte of Program Memory
    MOVWF   LOWPMBYTE           ;
    MOVF    EEDATH, W           ;W = MS Byte of Program EEDAT
    MOVWF   HIGHPMBYTE          ;
    BCF     STATUS, RP1         ;Bank 0
```

Required Sequence

**REGISTER 11-3: ECCPAS: ENHANCED CAPTURE/COMPARE/PWM AUTO-SHUTDOWN CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ECCPASE | ECCPAS2 | ECCPAS1 | ECCPAS0 | PSSAC1 | PSSAC0 | PSSBD1 | PSSBD0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **ECCPASE:** ECCP Auto-Shutdown Event Status bit
- 1 = A shutdown event has occurred; ECCP outputs are in shutdown state
- 0 = ECCP outputs are operating

bit 6-4 **ECCPAS<2:0>:** ECCP Auto-shutdown Source Select bits
- 000 = Auto-Shutdown is disabled
- 001 = Comparator C1 output high
- 010 = Comparator C2 output high(1)
- 011 = Either Comparators output is high
- 100 = VIL on INT pin
- 101 = VIL on INT pin or Comparator C1 output high
- 110 = VIL on INT pin or Comparator C2 output high
- 111 =VIL on INT pin or either Comparators output is high

bit 3-2 **PSSACn:** Pins P1A and P1C Shutdown State Control bits
- 00 = Drive pins P1A and P1C to '0'
- 01 = Drive pins P1A and P1C to '1'
- 1x = Pins P1A and P1C tri-state

bit 1-0 **PSSBDn:** Pins P1B and P1D Shutdown State Control bits
- 00 = Drive pins P1B and P1D to '0'
- 01 = Drive pins P1B and P1D to '1'
- 1x = Pins P1B and P1D tri-state

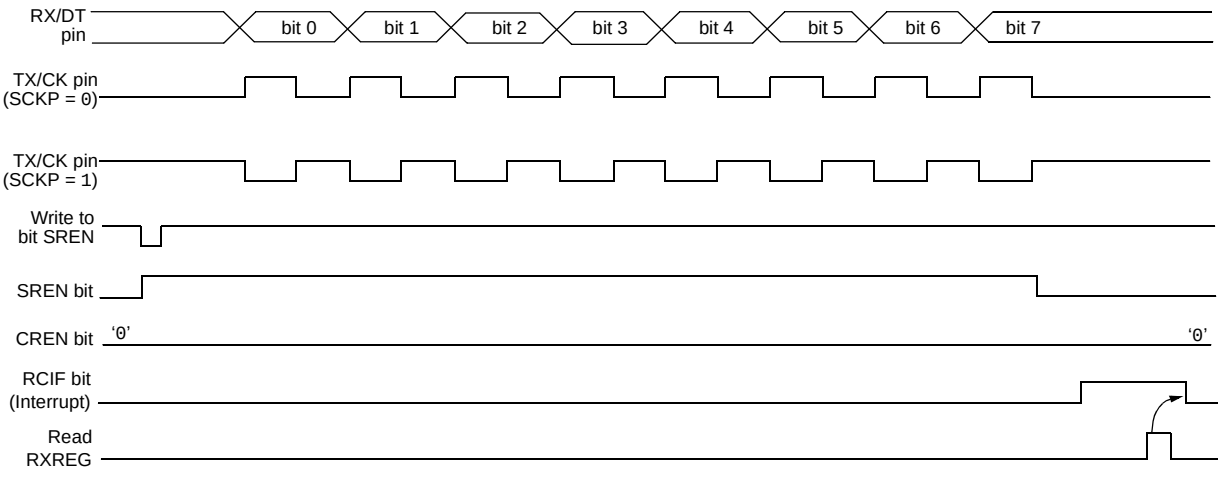
**Note 1:** If C2SYNC is enabled, the shutdown will be delayed by Timer1.

**Note 1:** The auto-shutdown condition is a level-based signal, not an edge-based signal. As long as the level is present, the auto-shutdown will persist.

**2:** Writing to the ECCPASE bit is disabled while an auto-shutdown condition persists.

**3:** Once the auto-shutdown condition has been removed and the PWM restarted (either through firmware or auto-restart) the PWM signal will always restart at the beginning of the next PWM period.

**FIGURE 12-12: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)**




**Note:** Timing diagram demonstrates Sync Master mode with bit SREN = 1 and bit BRGH = 0.

**TABLE 12-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|
| BAUDCTL | ABDOVF | RCIDL | — | SCKP | BRG16 | — | WUE | ABDEN | 159 |
| INTCON | GIE | PEIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 32 |
| PIE1 | — | ADIE | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMR1IE | 33 |
| PIR1 | — | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF | 35 |
| RCREG | EUSART Receive Data Register | | | | | | | | 155 |
| RCSTA | SPEN | RX9 | SREN | CREN | ADDEN | FERR | OERR | RX9D | 158 |
| SPBRG | BRG7 | BRG6 | BRG5 | BRG4 | BRG3 | BRG2 | BRG1 | BRG0 | 160 |
| SPBRGH | BRG15 | BRG14 | BRG13 | BRG12 | BRG11 | BRG10 | BRG9 | BRG8 | 160 |
| TRISC | TRISC7 | TRISC6 | TRISC5 | TRISC4 | TRISC3 | TRISC2 | TRISC1 | TRISC0 | 54 |
| TXREG | EUSART Transmit Data Register | | | | | | | | 150 |
| TXSTA | CSRC | TX9 | TXEN | SYNC | SENDB | BRGH | TRMT | TX9D | 157 |

**Legend:** x = unknown, – = unimplemented read as '0'. Shaded cells are not used for Synchronous Master Reception.

## 14.1 Configuration Bits

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations as shown in Register 14-1. These bits are mapped in program memory location 2007h and 2008h, respectively.

**Note:** Address 2007h and 2008h are beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "*PIC16F88X Memory Programming Specification*" (DS41287) for more information.

## REGISTER DEFINITIONS: CONFIGURATION WORDS

### REGISTER 14-1: CONFIG1: CONFIGURATION WORD REGISTER 1

| | | | | |
|---|---|---|---|---|
| $\overline{\text{DEBUG}}$ | LVP | FCMEN | IESO | BOREN<1:0> |
| bit 13 | | | | bit 8 |

| | | | | | |
|---|---|---|---|---|---|
| $\overline{\text{CPD}}$ | $\overline{\text{CP}}$ | MCLRE | $\overline{\text{PWRTE}}$ | WDTE | FOSC<2:0> |
| bit 7 | | | | | bit 0 |

bit 13 **$\overline{\text{DEBUG}}$:** In-Circuit Debugger Mode bit
1 = In-Circuit Debugger disabled, RB6/ICSPCLK and RB7/ICSPDAT are general purpose I/O pins
0 = In-Circuit Debugger enabled, RB6/ICSPCLK and RB7/ICSPDAT are dedicated to the debugger

bit 12 **LVP:** Low Voltage Programming Enable bit
1 = RB3/PGM pin has PGM function, low voltage programming enabled
0 = RB3 pin is digital I/O, HV on $\overline{\text{MCLR}}$ must be used for programming

bit 11 **FCMEN:** Fail-Safe Clock Monitor Enabled bit
1 = Fail-Safe Clock Monitor is enabled
0 = Fail-Safe Clock Monitor is disabled

bit 10 **IESO:** Internal External Switchover bit
1 = Internal/External Switchover mode is enabled
0 = Internal/External Switchover mode is disabled

bit 9-8 **BOREN<1:0>:** Brown-out Reset Selection bits(1)
11 = BOR enabled
10 = BOR enabled during operation and disabled in Sleep
01 = BOR controlled by SBOREN bit of the PCON register
00 = BOR disabled

bit 7 **$\overline{\text{CPD}}$:** Data Code Protection bit(2)
1 = Data memory code protection is disabled
0 = Data memory code protection is enabled

bit 6 **$\overline{\text{CP}}$:** Code Protection bit(3)
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 5 **MCLRE:** RE3/$\overline{\text{MCLR}}$ pin function select bit(4)
1 = RE3/$\overline{\text{MCLR}}$ pin function is $\overline{\text{MCLR}}$
0 = RE3/$\overline{\text{MCLR}}$ pin function is digital input, $\overline{\text{MCLR}}$ internally tied to $V_{DD}$

bit 4 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled and can be enabled by SWDTEN bit of the WDTCON register

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
111 = RC oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, RC on RA7/OSC1/CLKIN
110 = RCIO oscillator: I/O function on RA6/OSC2/CLKOUT pin, RC on RA7/OSC1/CLKIN
101 = INTOSC oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN
100 = INTOSCIO oscillator: I/O function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN
011 = EC: I/O function on RA6/OSC2/CLKOUT pin, CLKIN on RA7/OSC1/CLKIN
010 = HS oscillator: High-speed crystal/resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN
001 = XT oscillator: Crystal/resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN
000 = LP oscillator: Low-power crystal on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN

**Note 1:** Enabling Brown-out Reset does not automatically enable Power-up Timer.
**2:** The entire data EEPROM will be erased when the code protection is turned off.
**3:** The entire program memory will be erased when the code protection is turned off.
**4:** When $\overline{\text{MCLR}}$ is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.

**TABLE 14-4: INITIALIZATION CONDITION FOR REGISTER (CONTINUED)**

| Register | Address | Power-on Reset | $\overline{\text{MCLR}}$ Reset WDT Reset (Continued) Brown-out Reset(1) | Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out (Continued) |
|---|---|---|---|---|
| CM2CON1 | 109h | 0000 0--0 | 0000 0--0 | uuuu u--u |
| EEDAT | 10Ch | 0000 0000 | 0000 0000 | uuuu uuuu |
| EEADR | 10Dh | 0000 0000 | 0000 0000 | uuuu uuuu |
| EEDATH | 10Eh | --00 0000 | --00 0000 | --uu uuuu |
| EEADRH | 10Fh | ---0 0000 | ---0 0000 | ---u uuuu |
| SRCON | 185h | 0000 00-0 | 0000 00-0 | uuuu uu-u |
| BAUDCTL | 187h | 01-0 0-00 | 01-0 0-00 | uu-u u-uu |
| ANSEL | 188h | 1111 1111 | 1111 1111 | uuuu uuuu |
| ANSELH | 189h | 1111 1111 | 1111 1111 | uuuu uuuu |
| EECON1 | 18Ch | ---- x000 | ---- q000 | ---- uuuu |
| EECON2 | 18Dh | ---- ---- | ---- ---- | ---- ---- |

**Legend:** u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition.

**Note 1:** If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

**2:** One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

**3:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**4:** See Table 14-5 for Reset value for specific condition.

**5:** If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

**6:** Accessible only when SSPCON register bits SSPM<3:0> = 1001.

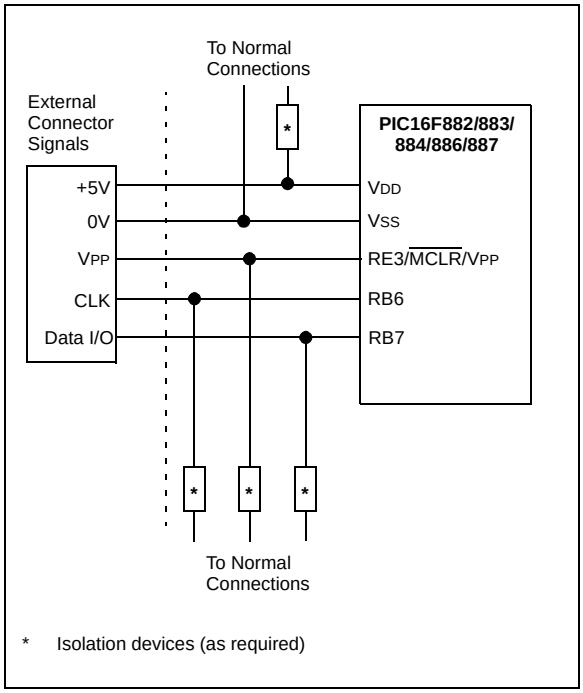
**TABLE 14-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS**

| Condition | Program Counter | Status Register | PCON Register |
|---|---|---|---|
| Power-on Reset | 000h | 0001 1xxx | --01 --0x |
| $\overline{\text{MCLR}}$ Reset during normal operation | 000h | 000u uuuu | --0u --uu |
| $\overline{\text{MCLR}}$ Reset during Sleep | 000h | 0001 0uuu | --0u --uu |
| WDT Reset | 000h | 0000 uuuu | --0u --uu |
| WDT Wake-up | PC + 1 | uuu0 0uuu | --uu --uu |
| Brown-out Reset | 000h | 0001 1uuu | --01 --u0 |
| Interrupt Wake-up from Sleep | PC + 1(1) | uuu1 0uuu | --uu --uu |

**Legend:** u = unchanged, x = unknown, – = unimplemented bit, reads as '0'.

**Note 1:** When the wake-up is due to an interrupt and Global Interrupt Enable bit, GIE, is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

**FIGURE 14-11: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING™ CONNECTION**




## 14.10 Low-Voltage (Single-Supply) ICSP Programming

The LVP bit of the Configuration Word enables low-voltage ICSP programming. This mode allows the microcontroller to be programmed via ICSP using a VDD source in the operating voltage range. This only means that VPP does not have to be brought to VIHH but can instead be left at the normal operating voltage. In this mode, the RB3/PGM pin is dedicated to the programming function and ceases to be a general purpose I/O pin. During programming, VDD is applied to the MCLR pin. To enter Programming mode, VDD must be applied to the RB3/PGM provided the LVP bit is set. The LVP bit defaults to on ('1') from the factory.

**Note 1:** The High-Voltage Programming mode is always available, regardless of the state of the LVP bit, by applying VIHH to the MCLR pin.

**2:** While in Low-Voltage ICSP mode, the RB3 pin can no longer be used as a general purpose I/O pin.

**3:** When using Low-Voltage ICSP Programming (LVP) and the pull-ups on PORTB are enabled, bit 3 in the TRISB register must be cleared to disable the pull-up on RB3 and ensure the proper operation of the device.

**4:** RB3 should not be allowed to float if LVP is enabled. An external pull-down device should be used to default the device to normal operating mode. If RB3 floats high, the PIC16F882/883/884/886/887 devices will enter Programming mode.

**5:** LVP mode is enabled by default on all devices shipped from Microchip. It can be disabled by clearing the LVP bit in the CONFIG register.

If Low-Voltage Programming mode is not used, the LVP bit can be programmed to a '0' and RB3/PGM becomes a digital I/O pin. However, the LVP bit may only be programmed when programming is entered with VIHH on MCLR. The LVP bit can only be charged when using high voltage on MCLR.

It should be noted, that once the LVP bit is programmed to '0', only the High-Voltage Programming mode is available and only High-Voltage Programming mode can be used to program the device.

When using low-voltage ICSP, the part must be supplied at 4.5V to 5.5V if a bulk erase will be executed. This includes reprogramming of the code-protect bits from an on state to an off state. For all other cases of low-voltage ICSP, the part may be programmed at the normal operating voltage. This means calibration values, unique user IDs or user code can be reprogrammed or added.

## 17.6 Thermal Considerations

| **Standard Operating Conditions (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +125°C | | | | | |
|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Typ.** | **Units** | **Conditions** |
| TH01 | θJA | Thermal Resistance Junction to Ambient | 47.2 | C/W | 40-pin PDIP package |
| | | | 24.4 | C/W | 44-pin QFN package |
| | | | 45.8 | C/W | 44-pin TQFP package |
| | | | 60.2 | C/W | 28-pin PDIP package |
| | | | 80.2 | C/W | 28-pin SOIC package |
| | | | 89.4 | C/W | 28-pin SSOP package |
| | | | 29 | C/W | 28-pin QFN package |
| TH02 | θJC | Thermal Resistance Junction to Case | 24.7 | C/W | 40-pin PDIP package |
| | | | 20.0 | C/W | 44-pin QFN package |
| | | | 14.5 | C/W | 44-pin TQFP package |
| | | | 29 | C/W | 28-pin PDIP package |
| | | | 23.8 | C/W | 28-pin SOIC package |
| | | | 23.9 | C/W | 28-pin SSOP package |
| | | | 20.0 | C/W | 28-pin QFN package |
| TH03 | TJ | Junction Temperature | 150 | C | For derated power calculations |
| TH04 | PD | Power Dissipation | — | W | PD = PINTERNAL + PI/O |
| TH05 | PINTERNAL | Internal Power Dissipation | — | W | PINTERNAL = IDD x VDD **(Note 1)** |
| TH06 | PI/O | I/O Power Dissipation | — | W | PI/O = Σ (IOL * VOL) + Σ (IOH * (VDD - VOH)) |
| TH07 | PDER | Derated Power | — | W | PDER = (TJ - TA)/θJA **(Note 2, 3)** |

**Note 1:** IDD is current to run the chip alone without driving any load on the output pins.

**2:** TA = Ambient Temperature.

**3:** Maximum allowable power dissipation is the lower value of either the absolute maximum total power dissipation or derated power (PDER).

**FIGURE 17-16: SPI SLAVE MODE TIMING (CKE = 0)**

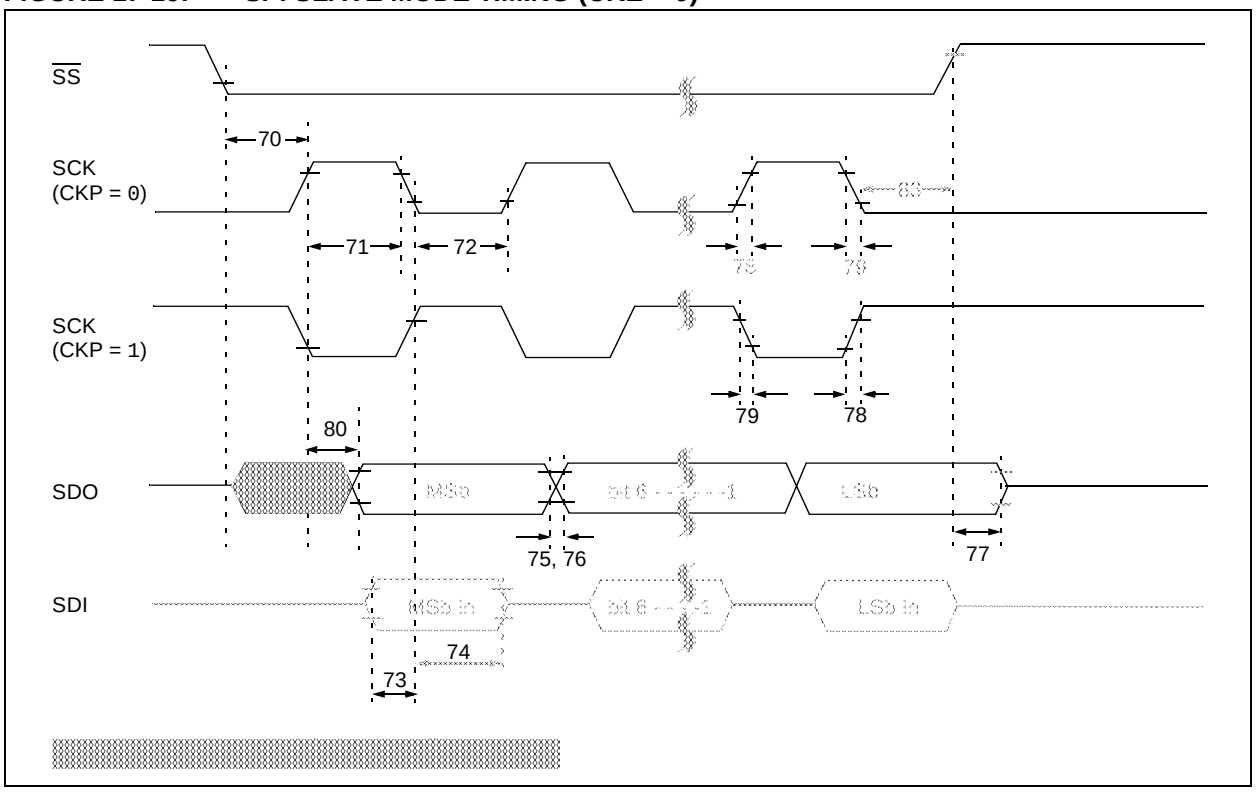



**FIGURE 17-17: SPI SLAVE MODE TIMING (CKE = 1)**