Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	36
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f423chu6

List of tables

2 Description

The STM32F423xH devices are based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 100 MHz. Their Cortex®-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F423xH devices belong to the STM32F423xH access product lines (with products combining power efficiency, performance and integration) while adding a new innovative feature called Batch Acquisition Mode (BAM) allowing to save even more power consumption during data batching.

The STM32F423xH devices incorporate high-speed embedded memories (1.5 Mbytes of Flash memory, 320 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses, three AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer a 12-bit ADC, two 12-bit DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timer for motor control, two general-purpose 32-bit timers and a low power timer.

They also feature standard and advanced communication interfaces.

- Up to four I^2Cs, including one I^2C supporting Fast-Mode Plus
- Five SPIs
- Five I^2Ss out of which two are full duplex. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicate internal audio PLL or via an external clock to allow synchronization.
- Four USARTs and six UARTs
- An SDIO/MMC interface
- An USB 2.0 OTG full-speed interface
- Three CANs
- An SAI.

In addition, the STM32F423xH devices embed advanced peripherals:

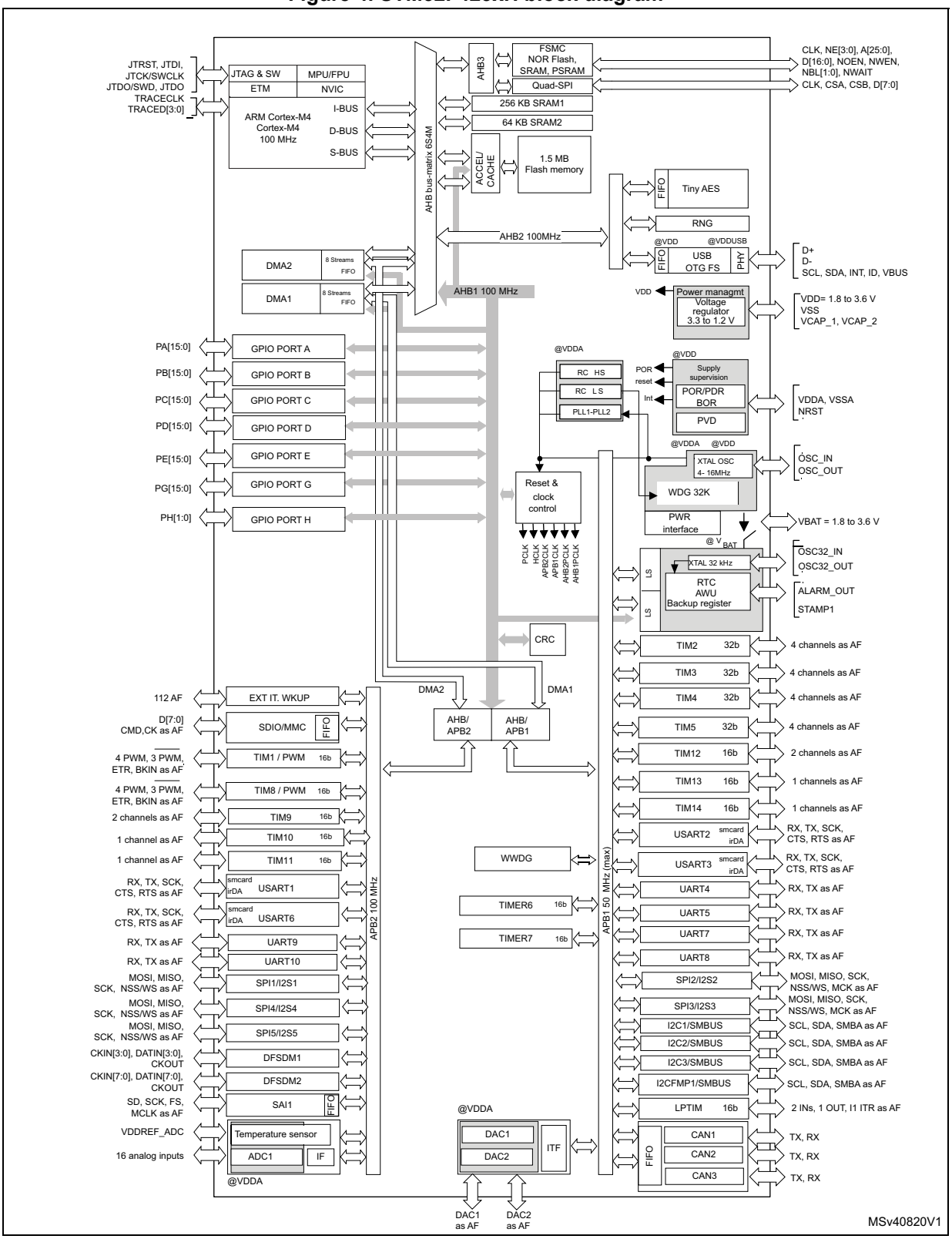
- A flexible static memory control interface (FSMC)
- A Quad-SPI memory interface
- Two digital filter for sigma modulator (DFSDM) supporting microphone MEMs and sound source localization, one with two filters and up to four inputs, and the second one with four filters and up to eight inputs

The STM32F423xH devices embed an AES hardware accelerator.

They are offered in 7 packages ranging from 48 to 144 pins. The set of available peripherals depends on the selected package. Refer to *Table 2: STM32F423xH features and peripheral counts* for the peripherals available for each part number.

The STM32F423xH operate in the – 40 to + 125 °C temperature range from a 1.7 (PDR OFF) to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

Figure 4. STM32F423xH block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 100 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 50 MHz.

Table 10. STM32F423xH pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
28	36	H1	54	K10	L12	76	PB15	I/O	FTf	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, I2CFMP1_SCL, SPI2_MOSI/I2S2_SD, DFSDM1_CKIN2, TIM12_CH2, SDIO_CK, EVENTOUT	-
-	-	NC	55	-	L9	77	PD8	I/O	FT	(2)	USART3_TX, FSMC_D13/FSMC_DA13, EVENTOUT	-
-	-	F2	56	K8	K9	78	PD9	I/O	FT	-	USART3_RX, FSMC_D14/FSMC_DA14, EVENTOUT	-
-	-	G1	57	J12	J9	79	PD10	I/O	FT	(7)	USART3_CK, UART4_TX, FSMC_D15/FSMC_DA15, EVENTOUT	-
-	-	NC	58	J11	H9	80	PD11	I/O	FT	(2)	DFSDM2_DATIN2, I2CFMP1_SMBA, USART3_CTS, QUADSPI_BK1_IO0, FSMC_A16, EVENTOUT	-
-	-	NC	59	J10	L10	81	PD12	I/O	FTf	(2)	TIM4_CH1, DFSDM2_CKIN2, I2CFMP1_SCL, USART3_RTS, QUADSPI_BK1_IO1, FSMC_A17, EVENTOUT	-
-	-	NC	60	H12	K10	82	PD13	I/O	FTf	(2)	TIM4_CH2, I2CFMP1_SDA, QUADSPI_BK1_IO3, FSMC_A18, EVENTOUT	-
-	-	-	-	-	G8	83	VSS	S	-	-	-	-
-	-	-	-	-	F8	84	VDD	S	-	-	-	-
-	-	NC	61	H11	K11	85	PD14	I/O	FTf	(2)	TIM4_CH3, I2CFMP1_SCL, DFSDM2_CKIN0, UART9_RX, FSMC_D0/FSMC_DA0, EVENTOUT	-

Table 10. STM32F423xH pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	39	E1	65	E10	F11	98	PC8	I/O	FT	-	TIM3_CH3, TIM8_CH3, DFSDM2_CKIN3, USART6_CK, QUADSPI_BK1_IO2, SDIO_D0, EVENTOUT	-
-	40	E2	66	D12	E11	99	PC9	I/O	FT	-	MCO_2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S2_CKIN, DFSDM2_DATIN3, QUADSPI_BK1_IO0, SDIO_D1, EVENTOUT	-
29	41	D3	67	D11	E12	100	PA8	I/O	FT	-	MCO_1, TIM1_CH1, I2C3_SCL, DFSDM1_CKOUT, USART1_CK, UART7_RX, USB_FS_SOF, CAN3_RX, SDIO_D1, EVENTOUT	-
30	42	D2	68	D10	D12	101	PA9	I/O	FT	-	TIM1_CH2, DFSDM2_CKIN3, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, USB_FS_VBUS, SDIO_D2, EVENTOUT	-
31	43	D1	69	C12	D11	102	PA10	I/O	FT	-	TIM1_CH3, DFSDM2_DATIN3, SPI2_MOSI/I2S2_SD, SPI5_MOSI/I2S5_SD, USART1_RX, USB_FS_ID, EVENTOUT	-
32	44	C3	70	B12	C12	103	PA11	I/O	FT	-	TIM1_CH4, DFSDM2_CKIN5, SPI2_NSS/I2S2_WS, SPI4_MISO, USART1_CTS, USART6_TX, CAN1_RX, USB_FS_DM, UART4_RX, EVENTOUT	-

Table 10. STM32F423xH pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	B8	-	H3	E5	143	PDR_ON	I	FT	-	-	-
48	64	A9	100	C4	F5	144	VDD	S	-	-	-	-

1. Function availability depends on the chosen device.
2. NC (Not Connected) pins are not bonded. They must be configured by software to output push-pull and forced to 0 in the output data register to avoid extra power consumption in low power mode.
3. Compatibility issue on alternate function pin PE4 SAI1_SD_A and PE6 SAI1_FS_A: Pins have been swapped versus other MCUs supporting those alternate SAI functions on those pins
4. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
5. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F423xHreference manual.
6. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
7. Incompatibility issue on alternate function with other MCUs supporting UART4: UART4_TX wrongly mapped to PD10 instead of PC10

Table 11. FSMC pin definition

Pins	FSMC		64 pins	81 pins	100 pins	144 pins
	LCD/NOR/ PSRAM/SRAM	NOR/PSRAM Mux				
PE2	A23	A23	-	-	Yes	Yes
PE3	A19	A19	-	-	Yes	Yes
PE4	A20	A20	-	-	Yes	Yes
PE5	A21	A21	-	-	Yes	Yes
PE6	A22	A22	-	-	Yes	Yes
PF0	A0	-	-	-	-	Yes
PF1	A1	-	-	-	-	Yes
PF2	A2	-	-	-	-	Yes
PF3	A3	-	-	-	-	Yes
PF4	A4	-	-	-	-	Yes
PF5	A5	-	-	-	-	Yes
PC2	NWE	NWE	Yes	Yes	Yes	Yes
PC3	A0	-	Yes	Yes	Yes	Yes
PA2	D4	DA4	Yes	Yes	Yes	Yes

8. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
9. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

Table 18. Features depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$)	Maximum Flash memory access frequency with wait states (1)(2)	I/O operation	Clock output frequency on I/O pins(3)	Possible Flash memory operations
V_{DD} =1.7 to 2.1 V(4)	Conversion time up to 1.2 Msps	16 MHz(5)	100 MHz with 6 wait states	– No I/O compensation	up to 30 MHz	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V	Conversion time up to 1.2 Msps	18 MHz	100 MHz with 5 wait states	– No I/O compensation	up to 30 MHz	16-bit erase and program operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2.4 Msps	20 MHz	100 MHz with 4 wait states	– I/O compensation works	up to 50 MHz	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V(6)	Conversion time up to 2.4 Msps	25 MHz	100 MHz with 3 wait states	– I/O compensation works	– up to 100 MHz when V_{DD} = 3.0 to 3.6 V – up to 50 MHz when V_{DD} = 2.7 to 3.0 V	32-bit erase and program operations

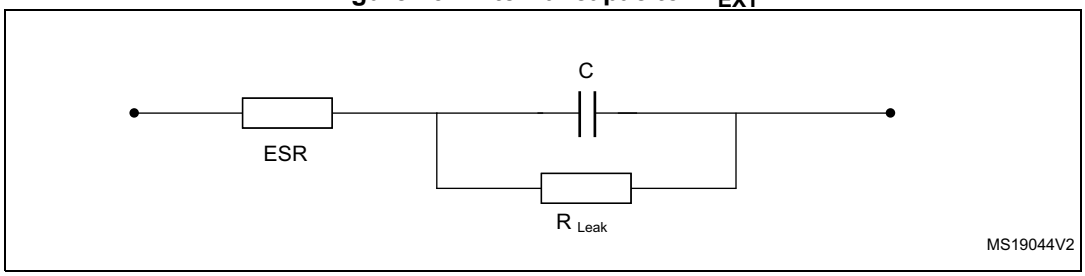
1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. Refer to *Table 61: I/O AC characteristics* for frequencies vs. external load.
4. V_{DD}/V_{DDA} minimum value of 1.7 V, with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
5. Prefetch available over the complete VDD supply range.
6. The voltage range for the USB full speed embedded PHY can drop down to 2.7 V. However the electrical characteristics of D- and D+ pins will be degraded between 2.7 and 3 V.

6.3.2 VCAP_1/VCAP_2 external capacitors

Stabilization for the main regulator is achieved by connecting the external capacitor C_{EXT} to the VCAP_1 and VCAP_2 pins. For packages supporting only 1 VCAP pin, the 2 CEXT capacitors are replaced by a single capacitor.

C_{EXT} is specified in *Table 19*.

Figure 23. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 19. VCAP_1/VCAP_2 operating conditions(1)

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor with the pins VCAP_1 and VCAP_2 available	2.2 µF
ESR	ESR of external capacitor with the pins VCAP_1 and VCAP_2 available	< 2 Ω
CEXT	Capacitance of external capacitor with a single VCAP pin available	4.7 µF
ESR	ESR of external capacitor with a single VCAP pin available	< 1 Ω

1. When bypassing the voltage regulator, the two 2.2 µF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

6.3.3 Operating conditions at power-up/power-down (regulator ON)

Subject to general operating conditions for T_A.

Table 20. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	µs/V
	V_{DD} fall time rate	20	∞	

Table 22. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	
V_{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	
		Rising edge	2.53	2.59	2.63	
V_{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	
		Rising edge	2.85	2.92	2.97	
$V_{BORhyst}$(2)	BOR hysteresis	-	-	100	-	mV
$T_{RSTTEMPO}$(2)(3)	POR reset timing	-	0.5	1.5	3.0	ms
I_{RUSH}(2)	In-Rush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	160	200	mA
E_{RUSH}(2)	In-Rush energy on voltage regulator power-on (POR or wakeup from Standby)	V_{DD} = 1.7 V, T_A = 125 °C, I_{RUSH} = 171 mA for 31 µs	-	-	5.4	µC

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design.
3. The reset timing is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is fetched by the user application code.

6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 22: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The ART accelerator is ON.
- Voltage Scale 2 mode selected, internal digital voltage V12 = 1.26 V.
- HCLK is the system clock at 100 MHz. $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off,
  - with only one peripheral clocked on,
  - scale 1 with f_{HCLK} = 100 MHz,
  - scale 2 with f_{HCLK} = 84 MHz,
  - scale 3 with f_{HCLK} = 64 MHz.
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 39. Peripheral current consumption

Peripheral		I_{DD} (Typ)			Unit
		Scale 1	Scale 2	Scale 3	
AHB1	GPIOA	1.89	1.82	1.64	µA/MHz
	GPIOB	1.75	1.68	1.52	
	GPIOC	1.70	1.64	1.48	
	GPIOD	1.72	1.65	1.48	
	GPIOE	1.78	1.71	1.55	
	GPIOF	1.68	1.62	1.45	
	GPIOG	1.66	1.61	1.44	
	GPIOH	0.72	0.69	0.63	
	CRC	0.30	0.30	0.28	
	DMA1(1)	1.75N + 3.14	1.66N + 3.00	1.49N + 2.70	
	DMA2(1)	1.79N + 3.29	1.71N + 3.14	1.53N + 2.82	
AHB2	RNG	0.72	0.70	0.63	µA/MHz
	USB_OTG_FS	19.26	18.37	16.47	
	AES	2.75	2.63	2.36	
AHB3	FSMC	5.42	5.18	4.64	µA/MHz
	QSPI	10.33	9.86	8.84	

Table 39. Peripheral current consumption (continued)

Peripheral		I_{DD} (Typ)			Unit
		Scale 1	Scale 2	Scale 3	
APB2	AHB-APB2 bridge	0.10	0.11	0.09	µA/MHz
	TIM1	6.78	6.46	5.80	
	TIM8	6.94	6.62	5.94	
	USART1	3.14	3.00	2.69	
	USART6	3.12	2.98	2.67	
	UART9	2.89	1.98	1.75	
	UART10	2.91	2.00	1.77	
	ADC1	3.45	3.29	2.95	
	SDIO	3.54	3.37	3.03	
	SPI1	1.52	1.46	1.31	
	SPI4	1.50	1.43	1.28	
	SYSCFG	0.58	0.55	0.50	
	EXT1	0.91	0.86	0.78	
	TIM9	2.95	2.81	2.53	
	TIM10	1.88	1.79	1.61	
	TIM11	1.86	1.77	1.59	
	SPI5	1.50	1.43	1.30	
	SAI	2.89	2.75	2.47	
	DFSDM1	4.43	4.21	3.80	
	DFSDM2	7.08	6.76	6.05	
Bus Matrix		4.06	3.87	3.45	

1. N is the number of stream enable (1...8).

6.3.7 Wakeup time from low-power modes

The wakeup times given in *Table 40* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0/PC0/PC1) pins are used to wakeup from Standby, Stop and Sleep modes.

Figure 45. SAI master timing waveforms

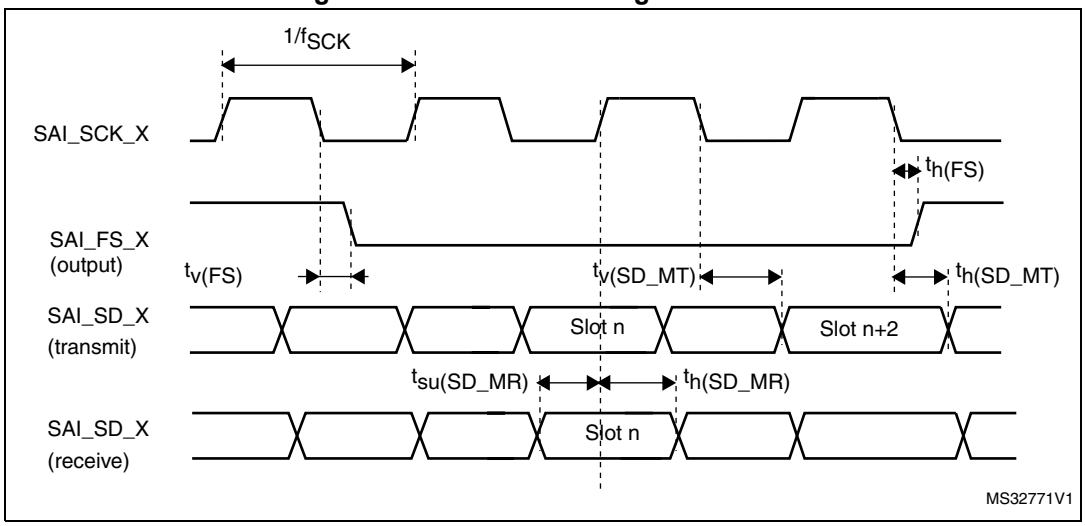
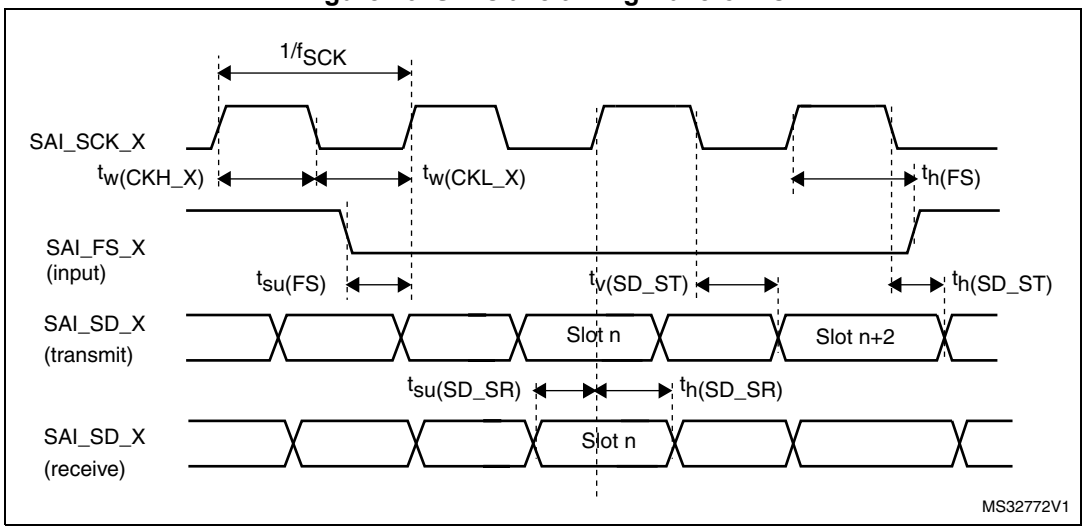


Figure 46. SAI slave timing waveforms



6.3.25 DFSDM characteristics

Unless otherwise specified, the parameters given in *Table 87* for DFSDM are derived from tests performed under the ambient temperature, f_{APB2} frequency and V_{DD} supply voltage conditions summarized in *Table 17: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 * V_{DD}

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDM_CKINy, DFSDM_DATINy, DFSDM_CKOUT for DFSDM).

Table 87. DFSDM characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	1.71 < V_{DD} < 3.6 V	-	-	f_{SYSCLK}	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0] = 0,1), External clock mode (SPICKSEL[1:0] = 0, 1.71 < V_{DD} < 3.6 V	-	-	20 ($f_{DFBDMCLK}$ / 4	
		SPI mode (SITP[1:0] = 0,1), External clock mode (SPICKSEL[1:0] = 0, 2.7 < V_{DD} < 3.6 V	-	-	20 ($f_{DFBDMCLK}$ / 4	
		SPI mode (SITP[1:0] = 0,1), Internal clock mode (SPICKSEL[1:0] ≠ 0, 1.71 < V_{DD} < 3.6 V	-	-	20 ($f_{DFBDMCLK}$ / 4	
		SPI mode (SITP[1:0] = 0,1), Internal clock mode (SPICKSEL[1:0] ≠ 0, 2.7 < V_{DD} < 3.6 V	-	-	20 ($f_{DFBDMCLK}$ / 4	
f_{CKOUT}	Output clock frequency	1.71 < V_{DD} < 3.6 V	-	-	20	
$DuCy_{CKOUT}$	Output clock frequency duty cycle	1.71 < V_{DD} < 3.6 V	45	50	55	%

Table 97. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period, V_{DD} range= 2.7 to 3.6 V	2 * T_{HCLK} - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x= 0...2)	-	2	
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high (x= 0…2)	T_{HCLK} + 0.5	-	
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	2.5	
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1.5	
$t_{(CLKH-NWEH)}$	FSMC_CLK high to FSMC_NWE high	T_{HCLK} + 0.5	-	
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FSMC_A/D[15:0] valid data after FSMC_CLK low	-	4	
$t_{d(CLKL-NBLL)}$	FSMC_CLK low to FSMC_NBL low	0	2	
$t_{d(CLKH-NBLH)}$	FSMC_CLK high to FSMC_NBL high	T_{HCLK} + 0.5	-	
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	3.5	-	

1. C_L = 30 pF.
2. Guaranteed by characterization results.

Figure 60. Synchronous non-multiplexed PSRAM write timings

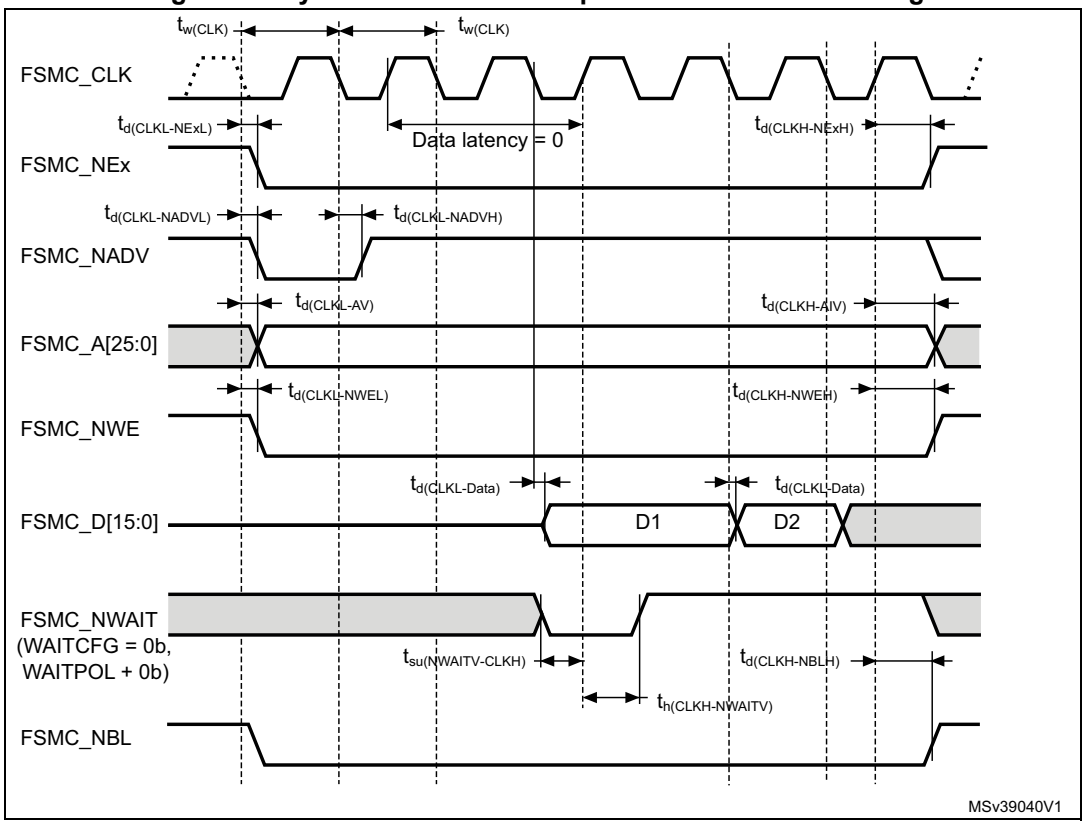


Table 99. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	2 * T_{HCLK} - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high (x= 0…2)	T_{HCLK} + 0.5	-	
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	2.5	
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FSMC_CLK high to FSMC_NWE high	T_{HCLK} + 1	-	
$t_{d(CLKL-Data)}$	FSMC_D[15:0] valid data after FSMC_CLK low	-	4	
$t_{d(CLKL-NBLL)}$	FSMC_CLK low to FSMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FSMC_CLK high to FSMC_NBL high	T_{HCLK} + 1	-	
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	3.5	-	

1. C_L = 30 pF.
2. Guaranteed by characterization results.

Table 106. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Appendix B Application block diagrams

B.1 Sensor Hub application example

Figure 84. Sensor Hub application example

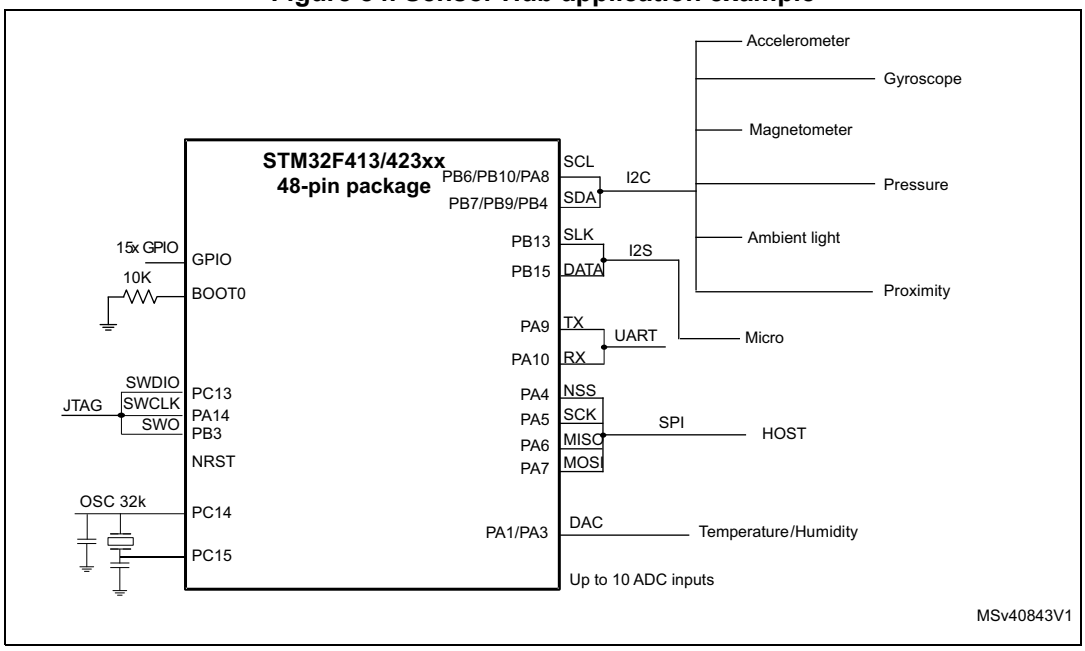
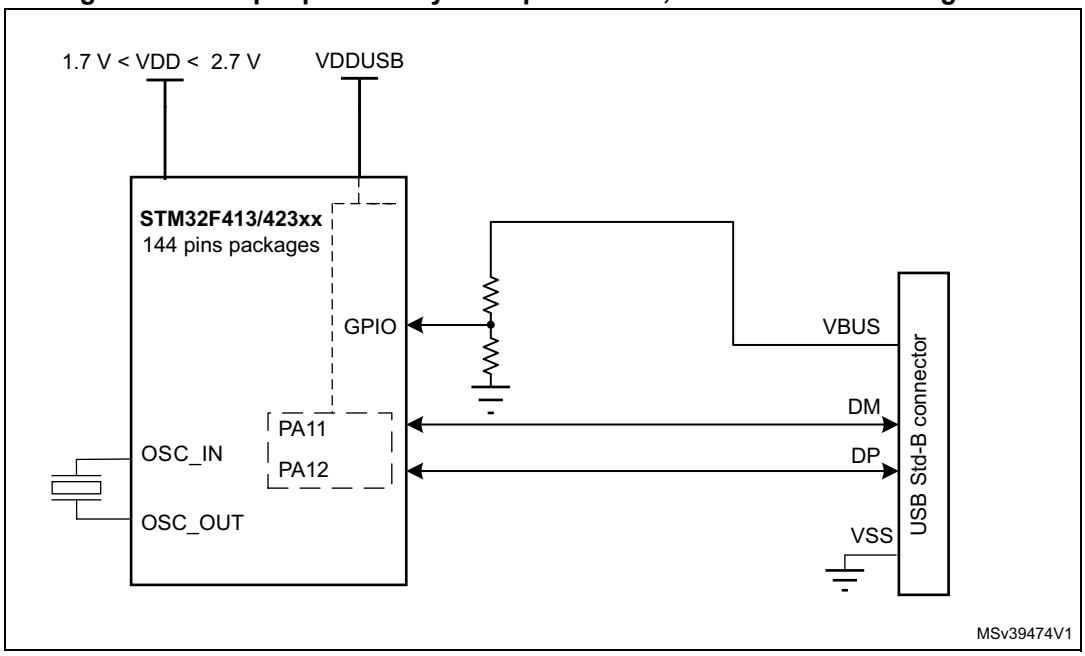
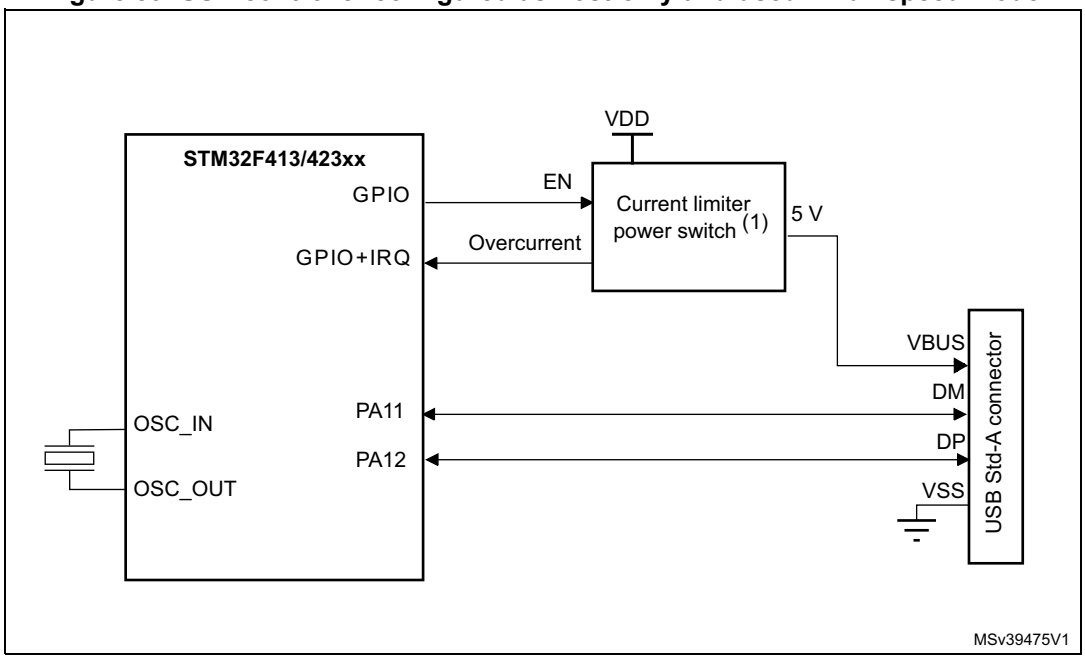


Figure 88. USB peripheral-only Full speed mode, VBUS detection using GPIO



1. External voltage regulator only needed when building a V_{BUS} powered device.

Figure 89. USB controller configured as host-only and used in full speed mode



2. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.

Revision history

Table 115. Document revision history

Date	Revision	Changes
02-Sep-2016	1	Initial release.
24-Oct-2016	2	Updated *Figure 65: WLCSP81 marking example (package top view)*
13-Dec-2016	3	Updated: – *Table 55: EMI characteristics for LQFP144* – *Table 56: ESD absolute maximum ratings* – *Table 70: QSPI dynamic characteristics in SDR mode* – *Table 111: UFBGA144 - 144-ball, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data* – *Figure 81: UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package outline*
12-Jan-2017	4	Added: – *Table 1: Device summary*
07-Mar-2017	5	Updated: – *Table 2: STM32F423xH features and peripheral counts* – *Table 12: STM32F423xH alternate functions* Added: – *Table 11: FSMC pin definition*