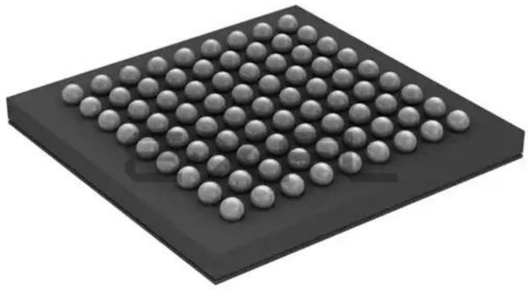

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### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 60 |
| Program Memory Size | 1.5MB (1.5M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 320K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 81-UFBGA, WLCSP |
| Supplier Device Package | 81-WLCSP (4.04x3.95) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f423mhy6tr |

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# 1 Introduction

This datasheet provides the description of the STM32F423xH microcontrollers.

For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214) available from *www.st.com*.

## 3.16 Power supply schemes

- $V_{DD}$ = 1.7 to 3.6 V: external power supply for I/Os with the internal supervisor (POR/PDR) disabled, provided externally through $V_{DD}$ pins. Requires the use of an external power supply supervisor connected to the $V_{DD}$ and NRST pins.
- $V_{SSA}$, $V_{DDA}$ = 1.7 to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL. $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively, with decoupling technique.

*Note: The $V_{DD}$/$V_{DDA}$ minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to Section 3.17.2: Internal reset OFF). Refer to Table 4: Regulator ON/OFF and internal power supply supervisor availability to identify the packages supporting this option.*

- $V_{BAT}$ = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.
- $V_{DDUSB}$ can be connected either to VDD or an external independent power supply (3.0 to 3.6 V) for USB transceivers.

  For example, when device is powered at 1.8 V, an independent power supply 3.3V can be connected to $V_{DDUSB}$. When the $V_{DDUSB}$ is connected to a separated power supply, it is independent from $V_{DD}$ or $V_{DDA}$ but it must be the last supply to be provided and the first to disappear.

The following conditions VDDUSB must be respected:

- During power-on phase ($V_{DD} < V_{DD\_MIN}$), $V_{DDUSB}$ should be always lower than $V_{DD}$
- During power-down phase ($V_{DD} < V_{DD\_MIN}$), $V_{DDUSB}$ should be always lower than $V_{DD}$
- $V_{DDUSB}$ rising and falling time rate specifications must be respected.
- In operating mode phase, $V_{DDUSB}$ could be lower or higher than VDD:
  - If USB is used, the associated GPIOs powered by $V_{DDUSB}$ are operating between $V_{DDUSB\_MIN}$ and $V_{DDUSB\_MAX}$.
  - If USB is not used, the associated GPIOs powered by $V_{DDUSB}$ are operating between $V_{DD\_MIN}$ and $V_{DD\_MAX}$.

### 3.18.1 Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when the regulator is ON:

- MR is used in the nominal regulation mode (With different voltage scaling in Run mode)
  In Main regulator mode (MR mode), different voltage scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption.
- LPR is used in the Stop mode
  The LP regulator mode is configured by software when entering Stop mode.
- Power-down is used in Standby mode.
  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Depending on the package, one or two external ceramic capacitors should be connected on the $V_{CAP\_1}$ and $V_{CAP\_2}$ pins. The $V_{CAP\_2}$ pin is only available on 100- and 144-pin packages.

All packages have the regulator ON feature.

### 3.18.2 Regulator OFF

This feature is available only on UFBGA100 and UFBGA144 packages, which feature the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a $V_{12}$ voltage source through $V_{CAP\_1}$ and $V_{CAP\_2}$ pins.

Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency.

The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on $V_{12}$. An external power supply supervisor should be used to monitor the $V_{12}$ of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on $V_{12}$ power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the $V_{12}$ logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.

### 3.18.3 Regulator ON/OFF and internal reset ON/OFF availability

**Table 4. Regulator ON/OFF and internal power supply supervisor availability**

| Package | Regulator ON | Regulator OFF | Power supply supervisor ON | Power supply supervisor OFF |
|---|---|---|---|---|
| UFQFPN48 | Yes | No | Yes | No |
| LQFP64 | Yes | No | Yes | No |
| WLCSP81 | Yes<br>BYPASS_REG<br>set to $V_{SS}$ | Yes<br>BYPASS_REG<br>set to $V_{DD}$ | Yes<br>PDR_ON<br>set to $V_{DD}$ | Yes<br>PDR_ON<br>set to $V_{SS}$ |
| LQFP100 | Yes | No | Yes | No |
| LQFP144 | Yes | No | Yes<br>PDR_ON<br>set to $V_{DD}$ | Yes<br>PDR_ON<br>set to $V_{SS}$ |
| UFBGA100 | Yes<br>BYPASS_REG<br>set to $V_{SS}$ | Yes<br>BYPASS_REG<br>set to $V_{DD}$ | | |
| UFBGA144 | Yes<br>BYPASS_REG<br>set to $V_{SS}$ | Yes<br>BYPASS_REG<br>set to $V_{DD}$ | | |

## 3.19 Real-time clock (RTC) and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC features a reference clock detection, a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The backup registers are 32-bit registers used to store 80 byte of user application data when $V_{DD}$ power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see *Section 3.20: Low-power modes*).

The main USB OTG FS features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Support of session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed when bus-powered devices are connected
- Link Power Management (LPM)
- Battery Charging Detection (BCD) supporting DCP, CDP and SDP

## 3.34 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

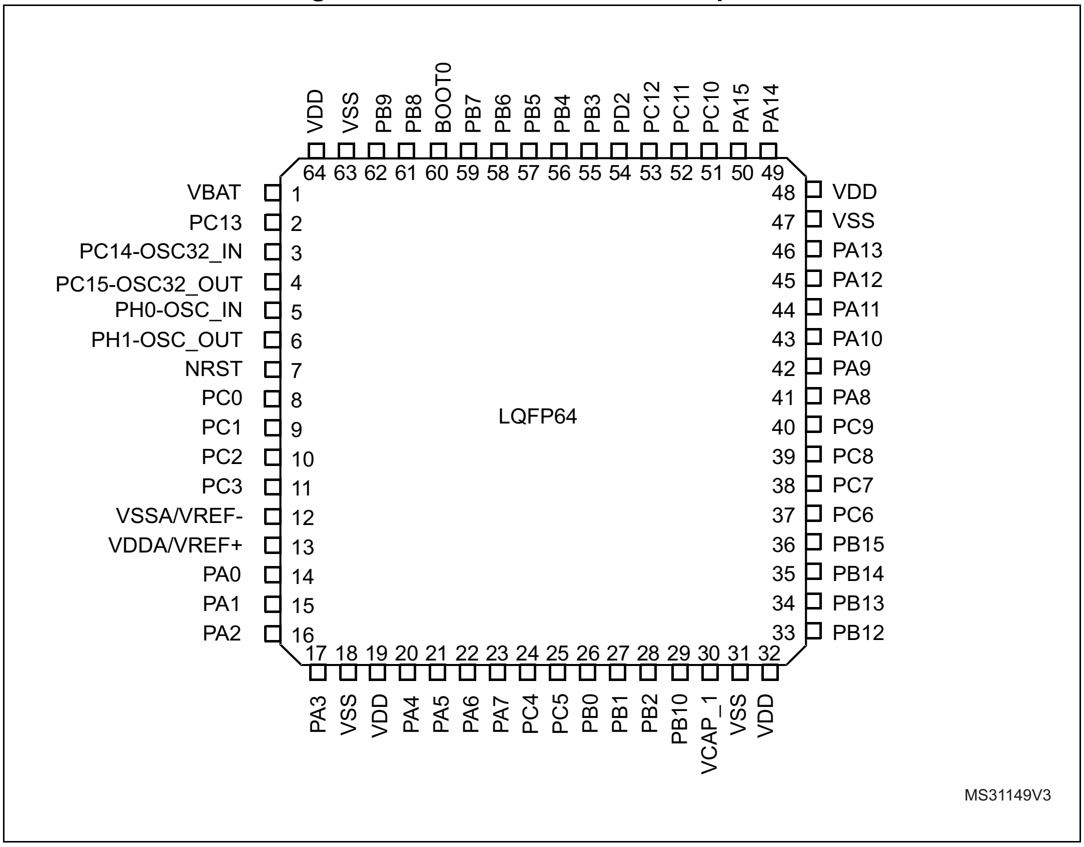
## 3.35 Advanced encryption standard hardware accelerator (AES)

The devices embed an AES hardware accelerator can be used to both encipher and decipher data using AES algorithm.

The AES peripheral supports:

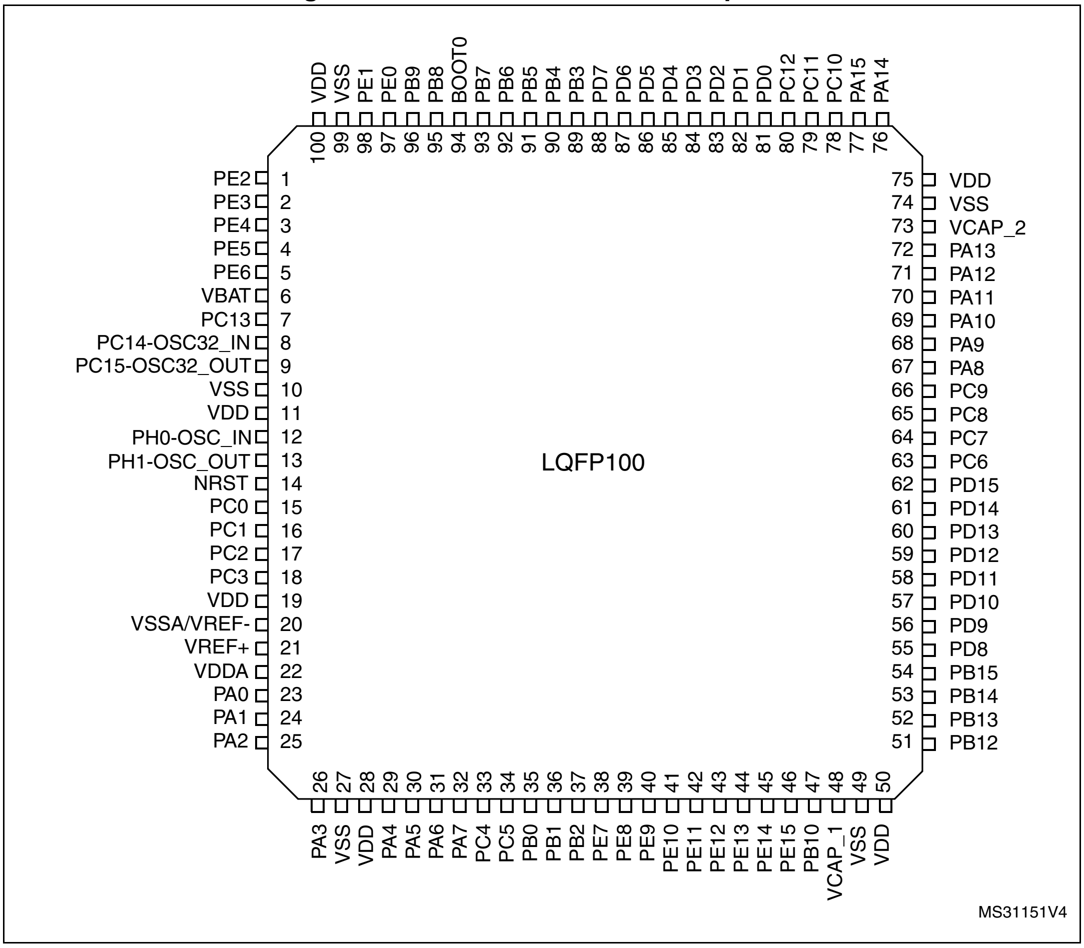
- Encryption/Decryption using AES Rijndael Block Cipher algorithm
- NIST FIPS 197 compliant implementation of AES encryption/decryption algorithm
- 128-bit and 256-bit register for storing the encryption, decryption or derivation key (4x 32-bit registers)
- Electronic codebook (ECB), Cipher block chaining (CBC), Counter mode (CTR), Galois Counter Mode (GCM), Galois Message Authentication Code mode (GMAC) and Cipher Message Authentication Code mode (CMAC) supported.
- Key scheduler
- Key derivation for decryption
- 128-bit data block processing
- 128-bit, 256-bit key length
- 1x32-bit INPUT buffer and 1x32-bit OUTPUT buffer.
- Register access supporting 32-bit data width only.
- One 128-bit Register for the initialization vector when AES is configured in CBC mode or for the 32-bit counter initialization when CTR mode is selected, GCM mode or CMAC mode.
- Automatic data flow control with support of direct memory access (DMA) using 2 channels, one for incoming data, and one for outcoming data.
- Suspend a message if another message with a higher priority needs to be processed.

**Figure 13. STM32F423xH LQFP64 pinout**




1. The above figure shows the package top view.

**Figure 14. STM32F423xH LQFP100 pinout**




1. The above figure shows the package top view.

**Table 10. STM32F423xH pin definition (continued)**

| Pin Number | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UFQFPN48 | LQFP64 | WLCSP81 | LQFP100 | UFBGA100 | UFBGA144 | LQFP144 | | | | | | |
| - | 9 | C7 | 16 | J2 | H2 | 27 | PC1 | I/O | FT | - | LPTIM1_OUT, DFSDM2_DATIN4, SAI1_SD_B, EVENTOUT | ADC1_IN11, WKUP3 |
| - | 10 | D7 | 17 | J3 | H3 | 28 | PC2 | I/O | FT | - | LPTIM1_IN2, DFSDM2_DATIN7, SPI2_MISO, I2S2ext_SD, SAI1_SCK_B, DFSDM1_CKOUT, FSMC_NWE, EVENTOUT | ADC1_IN12 |
| - | 11 | E7 | 18 | K2 | H4 | 29 | PC3 | I/O | FT | - | LPTIM1_ETR, DFSDM2_CKIN7, SPI2_MOSI/I2S2_SD, SAI1_FS_B, FSMC_A0, EVENTOUT | ADC1_IN13 |
| - | - | - | 19 | - | - | 30 | VDD | S | - | - | - | - |
| 8 | 12 | H9 | 20 | J1 | J1 | 31 | VSSA | S | - | - | - | - |
| - | - | - | - | K1 | K1 | - | VREF- | S | - | - | - | - |
| - | - | G8 | 21 | L1 | L1 | 32 | VREF+ | S | - | - | - | - |
| 9 | 13 | F7 | 22 | M1 | M1 | 33 | VDDA | S | - | - | - | - |
| 10 | 14 | G7 | 23 | L2 | J2 | 34 | PA0 | I/O | FT | - | TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, EVENTOUT | ADC1_IN0, WKUP1 |
| 11 | 15 | H8 | 24 | M2 | K2 | 35 | PA1 | I/O | FT | - | TIM2_CH2, TIM5_CH2, SPI4_MOSI/I2S4_SD, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, EVENTOUT | ADC1_IN1 |
| 12 | 16 | J9 | 25 | K3 | L2 | 36 | PA2 | I/O | FT | - | TIM2_CH3, TIM5_CH3, TIM9_CH1, I2S2_CKIN, USART2_TX, FSMC_D4/FSMC_DA4, EVENTOUT | ADC1_IN2 |
| 13 | 17 | E6 | 26 | L3 | M2 | 37 | PA3 | I/O | FT | - | TIM2_CH4, TIM5_CH4, TIM9_CH2, I2S2_MCK, USART2_RX, SAI1_SD_B, FSMC_D5/FSMC_DA5, EVENTOUT | ADC1_IN3 |

Table 11. FSMC pin definition (continued)

| Pins | FSMC | | 64 pins | 81 pins | 100 pins | 144 pins |
|---|---|---|---|---|---|---|
| | LCD/NOR/ PSRAM/SRAM | NOR/PSRAM Mux | | | | |
| PA3 | D5 | DA5 | Yes | Yes | Yes | Yes |
| PA4 | D6 | DA6 | Yes | Yes | Yes | Yes |
| PA5 | D7 | DA7 | Yes | Yes | Yes | Yes |
| PC4 | NE4 | NE4 | Yes | Yes | Yes | Yes |
| PC5 | NOE | NOE | Yes | Yes | Yes | Yes |
| PF12 | A6 | - | - | - | - | Yes |
| PF13 | A7 | - | - | - | - | Yes |
| PF14 | A8 | - | - | - | - | Yes |
| PF15 | A9 | - | - | - | - | Yes |
| PG0 | A10 | - | - | - | - | Yes |
| PG1 | A11 | - | - | - | - | Yes |
| PE7 | D4 | DA4 | - | - | Yes | Yes |
| PE8 | D5 | DA5 | - | - | Yes | Yes |
| PE9 | D6 | DA6 | - | Yes | Yes | Yes |
| PE10 | D7 | DA7 | - | Yes | Yes | Yes |
| PE11 | D8 | DA8 | - | Yes | Yes | Yes |
| PE12 | D9 | DA9 | - | Yes | Yes | Yes |
| PE13 | D10 | DA10 | - | Yes | Yes | Yes |
| PE14 | D11 | DA11 | - | Yes | Yes | Yes |
| PE15 | D12 | DA12 | - | Yes | Yes | Yes |
| PB12 | D13 | DA13 | Yes | Yes | Yes | Yes |
| PB14 | D0 | DA0 | Yes | Yes | Yes | Yes |
| PD8 | D13 | DA13 | - | - | - | Yes |
| PD9 | D14 | DA14 | - | Yes | Yes | Yes |
| PD10 | D15 | DA15 | - | Yes | Yes | Yes |
| PD11 | A16 | A16 | - | - | Yes | Yes |
| PD12 | A17 | A17 | - | - | Yes | Yes |
| PD13 | A18 | A18 | - | - | Yes | Yes |
| PD14 | D0 | DA0 | - | - | Yes | Yes |
| PD15 | D1 | DA1 | - | - | Yes | Yes |
| PG2 | A12 | - | - | - | - | Yes |
| PG3 | A13 | - | - | - | - | Yes |
| PG4 | A14 | - | - | - | - | Yes |

**Table 11. FSMC pin definition (continued)**

| Pins | FSMC | | 64 pins | 81 pins | 100 pins | 144 pins |
|---|---|---|---|---|---|---|
| | LCD/NOR/ PSRAM/SRAM | NOR/PSRAM Mux | | | | |
| PG5 | A15 | - | - | - | - | Yes |
| PC6 | D1 | DA1 | Yes | Yes | Yes | Yes |
| PC11 | D2 | DA2 | Yes | Yes | Yes | Yes |
| PC12 | D3 | DA3 | Yes | Yes | Yes | Yes |
| PD0 | D2 | DA2 | - | Yes | Yes | Yes |
| PD1 | D3 | DA3 | - | - | Yes | Yes |
| PD2 | NWE | NWE | Yes | Yes | Yes | Yes |
| PD3 | CLK | CLK | - | - | Yes | Yes |
| PD4 | NOE | NOE | - | - | Yes | Yes |
| PD5 | NWE | NWE | - | - | Yes | Yes |
| PD6 | NWAIT | NWAIT | - | - | Yes | Yes |
| PD7 | NE1 | NE1 | - | - | Yes | Yes |
| PG9 | NE2 | NE2 | - | - | - | Yes |
| PG10 | NE3 | NE3 | - | - | - | Yes |
| PG12 | NE4 | NE4 | - | - | - | Yes |
| PG13 | A24 | A24 | - | - | - | Yes |
| PG14 | A25 | A25 | - | - | - | Yes |
| PB7 | NL | NL | Yes | Yes | Yes | Yes |
| PE0 | NBL0 | NBL0 | - | - | Yes | Yes |
| PE1 | NBL1 | NBL1 | - | - | Yes | Yes |

**Table 38. Switching output I/O current consumption**

| Symbol | Parameter | Conditions(1) | I/O toggling frequency ($f_{SW}$) | Typ | Unit |
|---|---|---|---|---|---|
| IDDIO | I/O switching current | $V_{DD}$ = 3.3 V<br>C = $C_{INT}$ | 2 MHz | 0.05 | mA |
| | | | 8 MHz | 0.15 | |
| | | | 25 MHz | 0.45 | |
| | | | 50 MHz | 0.85 | |
| | | | 60 MHz | 1.00 | |
| | | | 84 MHz | 1.40 | |
| | | | 90 MHz | 1.67 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ = 0 pF<br>C = $C_{INT}$ + $C_{EXT}$ + $C_S$ | 2 MHz | 0.10 | |
| | | | 8 MHz | 0.35 | |
| | | | 25 MHz | 1.05 | |
| | | | 50 MHz | 2.20 | |
| | | | 60 MHz | 2.40 | |
| | | | 84 MHz | 3.55 | |
| | | | 90 MHz | 4.23 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ =10 pF<br>C = $C_{INT}$ + $C_{EXT}$ + $C_S$ | 2 MHz | 0.20 | |
| | | | 8 MHz | 0.65 | |
| | | | 25 MHz | 1.85 | |
| | | | 50 MHz | 2.45 | |
| | | | 60 MHz | 4.70 | |
| | | | 84 MHz | 8.80 | |
| | | | 90 MHz | 10.47 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ = 22 pF<br>C = $C_{INT}$ + $C_{EXT}$ + $C_S$ | 2 MHz | 0.25 | |
| | | | 8 MHz | 1.00 | |
| | | | 25 MHz | 3.45 | |
| | | | 50 MHz | 7.15 | |
| | | | 60 MHz | 11.55 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ = 33 pF<br>C = $C_{INT}$ + $C_{EXT}$ + $C_S$ | 2 MHz | 0.32 | |
| | | | 8 MHz | 1.27 | |
| | | | 25 MHz | 3.88 | |
| | | | 50 MHz | 12.34 | |

1. CS is the PCB board capacitance including the pad pin. CS = 7 pF (estimated value).

### On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The ART accelerator is ON.
- Voltage Scale 2 mode selected, internal digital voltage V12 = 1.26 V.
- HCLK is the system clock at 100 MHz. $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off,
  - with only one peripheral clocked on,
  - scale 1 with $f_{HCLK}$ = 100 MHz,
  - scale 2 with $f_{HCLK}$ = 84 MHz,
  - scale 3 with $f_{HCLK}$ = 64 MHz.
- Ambient operating temperature is 25 °C and $V_{DD}$=3.3 V.

**Table 39. Peripheral current consumption**

| Peripheral | | $I_{DD}$ (Typ) | | | Unit |
|---|---|---|---|---|---|
| | | Scale 1 | Scale 2 | Scale 3 | |
| AHB1 | GPIOA | 1.89 | 1.82 | 1.64 | µA/MHz |
| | GPIOB | 1.75 | 1.68 | 1.52 | |
| | GPIOC | 1.70 | 1.64 | 1.48 | |
| | GPIOD | 1.72 | 1.65 | 1.48 | |
| | GPIOE | 1.78 | 1.71 | 1.55 | |
| | GPIOF | 1.68 | 1.62 | 1.45 | |
| | GPIOG | 1.66 | 1.61 | 1.44 | |
| | GPIOH | 0.72 | 0.69 | 0.63 | |
| | CRC | 0.30 | 0.30 | 0.28 | |
| | DMA1(1) | 1.75N + 3.14 | 1.66N + 3.00 | 1.49N + 2.70 | |
| | DMA2(1) | 1.79N + 3.29 | 1.71N + 3.14 | 1.53N + 2.82 | |
| AHB2 | RNG | 0.72 | 0.70 | 0.63 | µA/MHz |
| | USB_OTG_FS | 19.26 | 18.37 | 16.47 | |
| | AES | 2.75 | 2.63 | 2.36 | |
| AHB3 | FSMC | 5.42 | 5.18 | 4.64 | µA/MHz |
| | QSPI | 10.33 | 9.86 | 8.84 | |

**Table 71. QSPI dynamic characteristics in DDR mode(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{w(CKH)}$ | QSPI clock high and low time | - | $t_{(CK)}$ / 2 - 1 | - | $t_{(CK)}$ / 2 | ns |
| $t_{w(CKL)}$ | | | $t_{(CK)}$ / 2 | - | $t_{(CK)}$ / 2 + 1 | |
| $t_{sr(IN)}$, $t_{sf(IN)}$ | Data input setup time | 2.7 V < $V_{DD}$ < 3.6 V | 0.5 | - | - | |
| | | 1.71 V < $V_{DD}$ < 3.6 V | 0.5 | - | - | |
| $t_{hr(IN)}$, $t_{hf(IN)}$ | Data input hold time | 2.7 V<$V_{DD}$<3.6 V | 2 | - | - | |
| | | 1.71 V<$V_{DD}$<3.6 V | 2 | - | - | |
| $t_{vr(OUT)}$, $t_{vf(OUT)}$ | Data output valid time | 2.7 V<$V_{DD}$<3.6 V | - | 8.5 | 9 | |
| | | 1.71 V<$V_{DD}$<3.6 V | - | 8.5 | 11.5 | |
| $t_{hr(OUT)}$, $t_{hf(OUT)}$ | Data output hold time | - | 7.5 | - | - | |

1. Guaranteed by characterization results.

### USB OTG full speed (FS) characteristics

This interface is present in USB OTG FS controller.

**Table 72. USB OTG FS startup time**

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $t_{STARTUP}$(1) | USB OTG FS transceiver startup time | 1 | µs |

1. Guaranteed by design.

**Table 73. USB OTG FS DC electrical characteristics**

| Symbol | | Parameter | Conditions | Min.(1) | Typ. | Max.(1) | Unit |
|---|---|---|---|---|---|---|---|
| Input levels | $V_{DD}$ | USB OTG FS operating voltage | | 3.0(2) | - | 3.6 | V |
| | $V_{DI}$(3) | Differential input sensitivity | I(USB_FS_DP/DM) | 0.2 | - | - | V |
| | $V_{CM}$(3) | Differential common mode range | Includes $V_{DI}$ range | 0.8 | - | 2.5 | |
| | $V_{SE}$(3) | Single ended receiver threshold | | 1.3 | - | 2.0 | |
| Output levels | $V_{OL}$ | Static output level low | $R_L$ of 1.5 kΩ to 3.6 V(4) | - | - | 0.3 | V |
| | $V_{OH}$ | Static output level high | $R_L$ of 15 kΩ to $V_{SS}$(4) | 2.8 | - | 3.6 | |
| $R_{PD}$ | | PA11, PA12 (USB_FS_DM/DP) | $V_{IN}$ = $V_{DD}$ | 17 | 21 | 24 | kΩ |
| | | PA9 (OTG_FS_VBUS) | | 0.65 | 1.1 | 2.0 | |
| $R_{PU}$ | | PA11, PA12 (USB_FS_DM/DP) | $V_{IN}$ = $V_{SS}$ | 1.5 | 1.8 | 2.1 | |
| | | PA9 (OTG_FS_VBUS) | $V_{IN}$ = $V_{SS}$ | 0.25 | 0.37 | 0.55 | |

1. All the voltages are measured from the local ground potential.

### 6.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 75* are derived from tests performed under the ambient temperature, $f_{PCLK2}$ frequency and $V_{DDA}$ supply voltage conditions summarized in *Table 17*.

**Table 75. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Power supply | $V_{DDA} - V_{REF+} < 1.2$ V | 1.7(1) | - | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | | 1.7(1) | - | $V_{DDA}$ | |
| $V_{REF-}$ | Negative reference voltage | - | - | 0 | - | |
| $f_{ADC}$ | ADC clock frequency | $V_{DDA}$ = 1.7(1) to 2.4 V | 0.6 | 15 | 18 | MHz |
| | | $V_{DDA}$ = 2.4 to 3.6 V | 0.6 | 30 | 36 | MHz |
| $f_{TRIG}$(2) | External trigger frequency | $f_{ADC}$ = 30 MHz, 12-bit resolution | - | - | 1764 | kHz |
| | | - | - | - | 17 | $1/f_{ADC}$ |
| $V_{AIN}$ | Conversion voltage range(3) | - | 0 ($V_{SSA}$ or $V_{REF-}$ tied to ground) | - | $V_{REF+}$ | V |
| $R_{AIN}$(2) | External input impedance | See *Equation 1* for details | - | - | 50 | kΩ |
| $R_{ADC}$(2)(4) | Sampling switch resistance | - | - | - | 6 | kΩ |
| $C_{ADC}$(2) | Internal sample and hold capacitor | - | - | 4 | 7 | pF |
| $t_{lat}$(2) | Injection trigger conversion latency | $f_{ADC}$ = 30 MHz | - | - | 0.100 | µs |
| | | - | - | - | 3(5) | $1/f_{ADC}$ |
| $t_{latr}$(2) | Regular trigger conversion latency | $f_{ADC}$ = 30 MHz | - | - | 0.067 | µs |
| | | - | - | - | 2(5) | $1/f_{ADC}$ |
| $t_S$(2) | Sampling time | $f_{ADC}$ = 30 MHz | 0.100 | - | 16 | µs |
| | | - | 3 | - | 480 | $1/f_{ADC}$ |
| $t_{STAB}$(2) | Power-up time | - | - | 2 | 3 | µs |
| $t_{CONV}$(2) | Total conversion time (including sampling time) | $f_{ADC}$ = 30 MHz 12-bit resolution | 0.50 | - | 16.40 | µs |
| | | $f_{ADC}$ = 30 MHz 10-bit resolution | 0.43 | - | 16.34 | µs |
| | | $f_{ADC}$ = 30 MHz 8-bit resolution | 0.37 | - | 16.27 | µs |
| | | $f_{ADC}$ = 30 MHz 6-bit resolution | 0.30 | - | 16.20 | µs |
| | | 9 to 492 ($t_S$ for sampling +n-bit resolution for successive approximation) | | | | $1/f_{ADC}$ |

### 6.3.22 $V_{BAT}$ monitoring characteristics

**Table 83. $V_{BAT}$ monitoring characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| R | Resistor bridge for $V_{BAT}$ | - | 50 | - | KΩ |
| Q | Ratio on $V_{BAT}$ measurement | - | 4 | - | |
| Er[1] | Error on Q | –1 | - | +1 | % |
| $T_{S\_vbat}$[2][2] | ADC sampling time when reading the $V_{BAT}$ 1 mV accuracy | 5 | - | - | µs |

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

### 6.3.23 Embedded reference voltage

The parameters given in *Table 84* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 17*.

**Table 84. Embedded internal reference voltage**

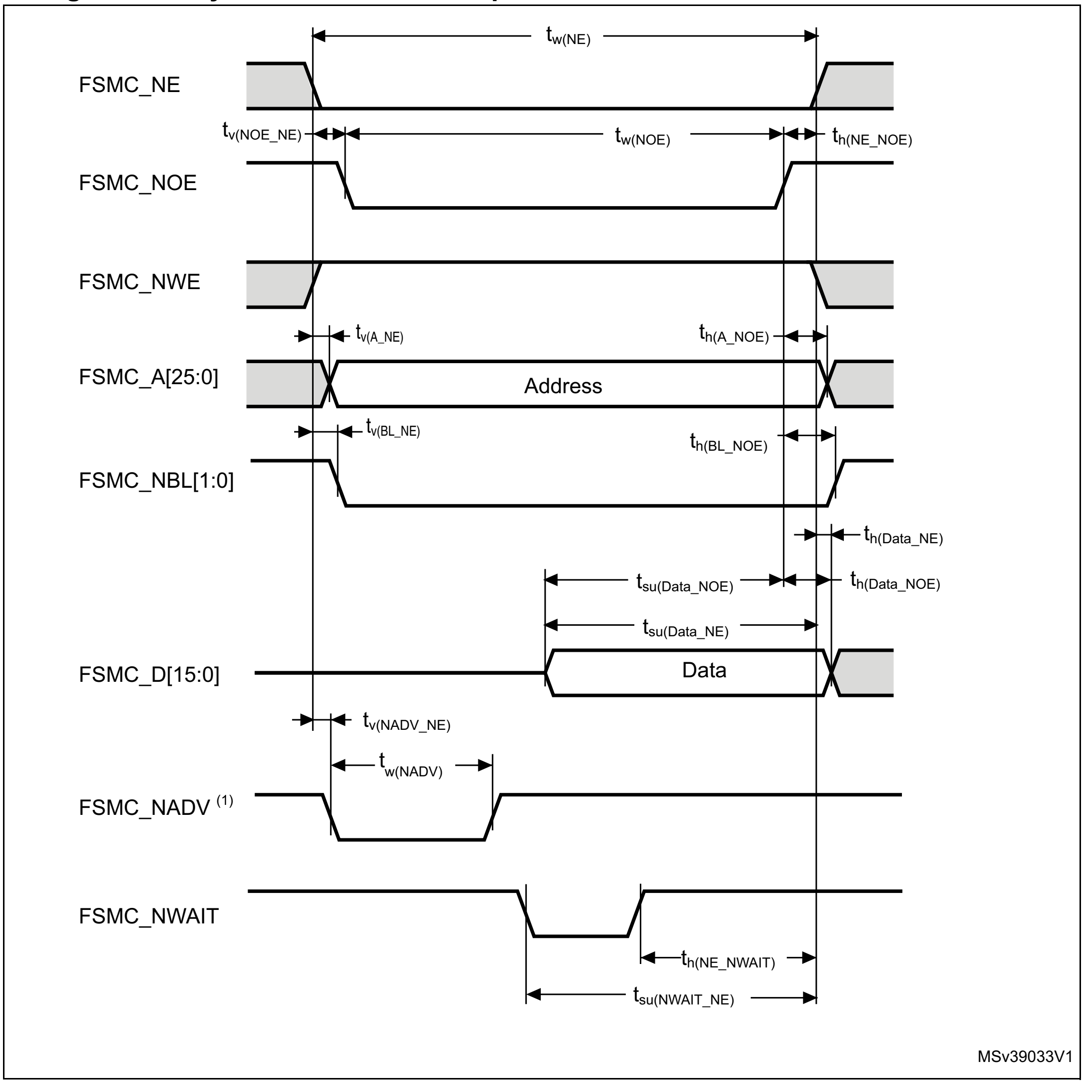
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | –40 °C < $T_A$ < +125 °C | 1.18 | 1.21 | 1.24 | V |
| $T_{S\_vrefint}$[1] | ADC sampling time when reading the internal reference voltage | - | 10 | - | - | µs |
| $V_{RERINT\_s}$[2] | Internal reference voltage spread over the temperature range | $V_{DD}$ = 3V ± 10mV | - | 3 | 5 | mV |
| $T_{Coeff}$[2] | Temperature coefficient | - | - | 30 | 50 | ppm/°C |
| $t_{START}$[2] | Startup time | - | - | 6 | 10 | µs |

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design

**Table 85. Internal reference voltage calibration values**

| Symbol | Parameter | Memory address |
|---|---|---|
| $V_{REFIN\_CAL}$ | Raw data acquired at temperature of 30 °C $V_{DDA}$ = 3.3 V | 0x1FFF 7A2A - 0x1FFF 7A2B |

**Figure 53. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms**




1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

**Table 106. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[(1)] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | - | 12.000 | - | - | 0.4724 | - |
| D1 | - | 10.000 | - | - | 0.3937 | - |
| D3 | - | 7.500 | - | - | 0.2953 | - |
| E | - | 12.000 | - | - | 0.4724 | - |
| E1 | - | 10.000 | - | - | 0.3937 | - |
| E3 | - | 7.500 | - | - | 0.2953 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| K | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| ccc | - | - | 0.080 | - | - | 0.0031 |

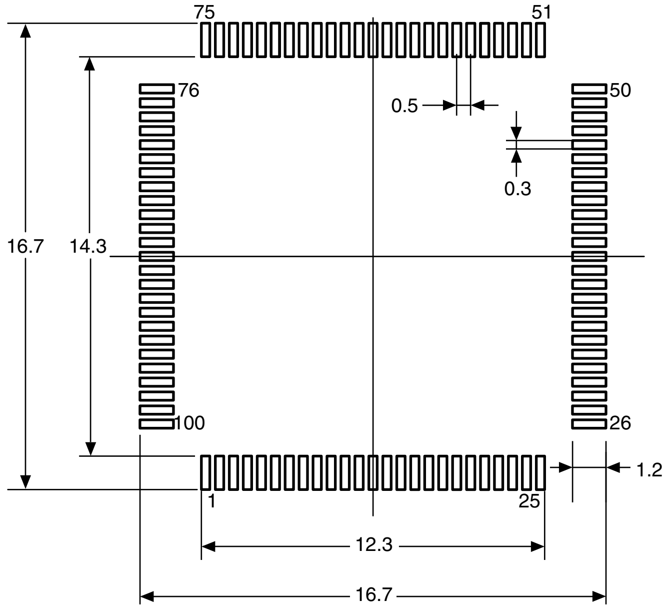
1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Table 107. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| E3 | - | 12.000 | - | - | 0.4724 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0.0° | 3.5° | 7.0° | 0.0° | 3.5° | 7.0° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

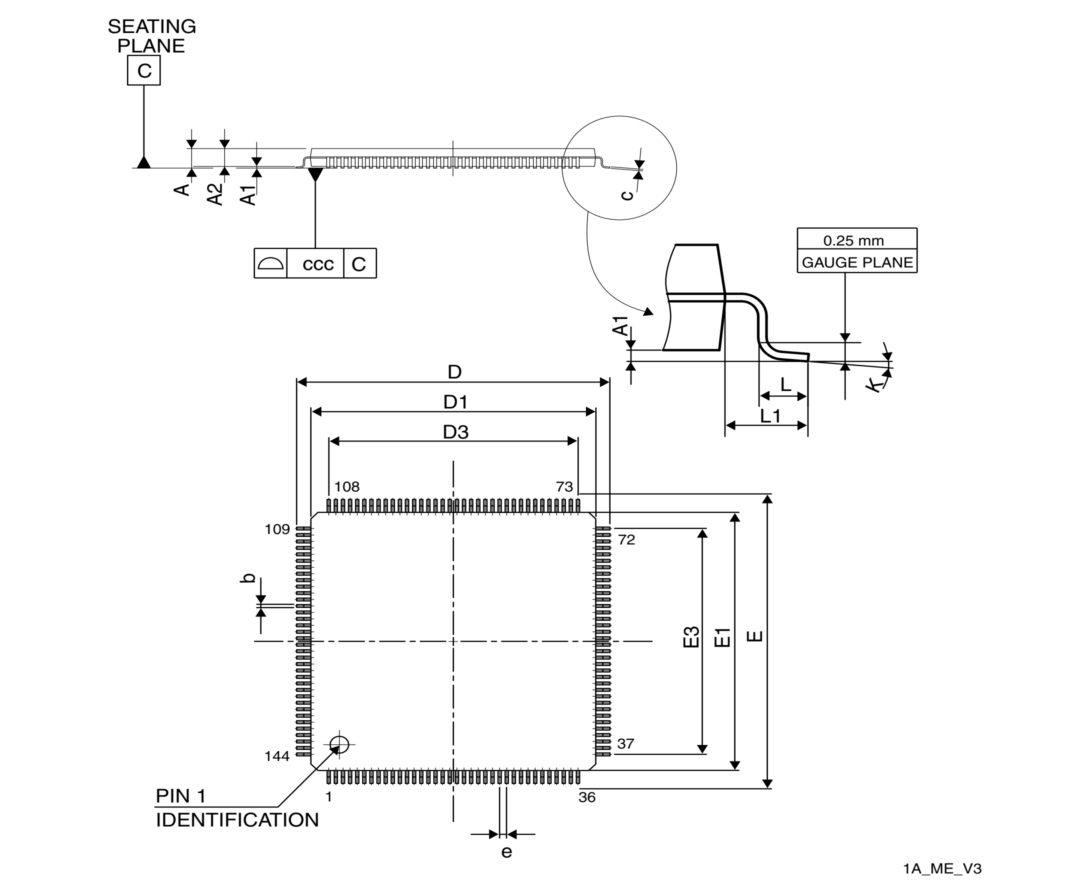
**Figure 73. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint**




1. Dimensions are in millimeters.

## 7.5 LQFP144 package information

**Figure 75. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline**




1. Drawing is not to scale.