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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f423rht6

1 Introduction

This datasheet provides the description of the STM32F423xH microcontrollers.

For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214) available from *www.st.com*.

These features make the STM32F423xH microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile phone sensor hub
- Wearable devices
- Connected objects
- Wifi modules

Figure 4 shows the general block diagram of the devices.

Table 2. STM32F423xH features and peripheral counts

Peripherals		STM32F423xH				
Flash memory (Kbyte)		1536				
SRAM (Kbyte)	System	320 (256 + 64)				
FSMC memory controller		-	1(1)	1(1)	1(1)	1
FSMC LCD parallel interface Data bus size		-	8	16		
Quad-SPI memory interface		-	1			
Timers	General-purpose	10(2)	10	10(3)	10	
	Advanced-control	2(4)	2			
	Basic	2				
	Low-power timer	1				
Random number generator		1				
AES		1				
Comm. interfaces	SPI/ I^2S	5/5 (2 full duplex)				
	I^2C	3				
	I^2CFMP	1				
	USART/UART	3/3	4/3		4/6	
	SDIO/MMC	1				
	USB/OTG FS Dual power rail	1 No		1 Yes	1 No	1 Yes
	CAN	3				
	SAI	1				
Number of digital Filtersfor Sigma-delta modulator		6				
Number of channels		7	11	12		
GPIOs		36	50	60	81	114
12-bit ADC		1				
Number of channels		10	16			
12-bit DAC		Yes				
Number of channels		2				
Maximum CPU frequency		100 MHz				
Operating voltage		1.7 to 3.6 V				
Operating temperatures		Ambient temperatures: – 40 to + 85 °C/– 40 to + 105 °C / – 40 to + 125 °C				
		Junction temperature: – 40 to + 130 °C				
Package		UFQFPN48	LQFP64	WLCSP81	UFBGA100 LQFP100	UFBGA144 LQFP144

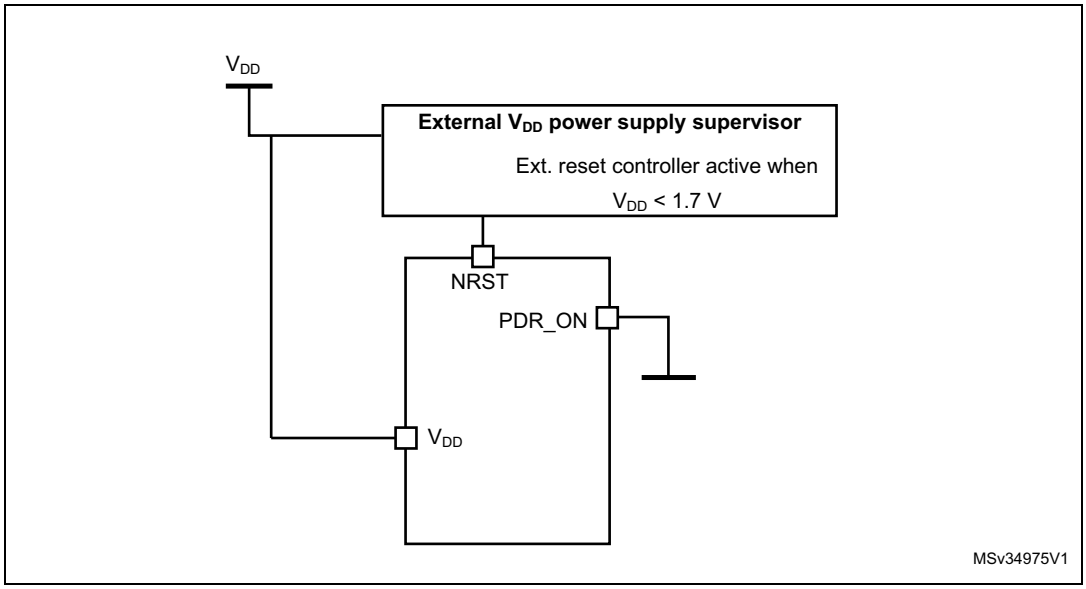
1. 64 pins packages support only 8 bits multiplexed mode interface
   81 pins packages support 1 external memory of up to 64KB in multiplexed mode
   100 pins packages support 2 external memories of up to 64MB in multiplexed mode
   Refer to *Table 11: FSMC pin definition* for more detailed information.
2. 48 pins packages: TIM3 and TIM4: ETR pin not available.

3.17.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled by setting the PDR_ON pin to low.

An external power supply supervisor should monitor V_{DD} and should set the device in reset mode when V_{DD} is below 1.7 V. NRST should be connected to this external power supply supervisor. Refer to *Figure 7: Power supply supervisor interconnection with internal reset OFF*.

Figure 7. Power supply supervisor interconnection with internal reset OFF(1)



1. The PRD_ON pin is available only on WLCSP81, UFBGA100, UFBGA144 and LQFP144 packages.

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.

3.18 Voltage regulator

The regulator has three operating modes:

– Main regulator mode (MR)
– Low power regulator (LPR)
– Power-down

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

The RTC and backup registers are supplied through a switch that is powered either from the V_{DD} supply when present or from the VBAT pin.

3.20 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

  To further reduce the power consumption, the Flash memory can be switched off before entering in Sleep mode. Note that this requires a code execution from the RAM.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm/ wakeup/ tamper/ time stamp events).

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain when selected.

  The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on one of the WKUP pins, or an RTC alarm/ wakeup/ tamper/time stamp event occurs.

  Standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

3.21 V_{BAT} operation

The VBAT pin allows to power the device V_{BAT} domain from an external battery, an external super-capacitor, or from V_{DD} when no external battery and an external super-capacitor are present.

V_{BAT} operation is activated when V_{DD} is not present.

The VBAT pin supplies the RTC and the backup registers.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation. When PDR_ON pin is not connected to V_{DD} (internal Reset OFF), the V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.

Different sources can also be selected for the SAI. The different possible sources are the main PLL, the PLLI2S, HSE or HSI clocks or an external clock provided through a pin (external PLL or CODEC output).

The PLLI2S configuration can be modified to manage an I^2S/SAI sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

3.29 Digital filter for sigma-delta modulators (DFSDM)

The device embeds two DFSDMs:

- DFSDM1 has 2 digital filters modules and 4 external input serial channels (transceivers) or alternately 2 internal parallel inputs support.
- DFSDM2 features 4 digital filters modules and 8 external input serial channels (transceivers) or alternately 4 internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs). DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in hardware. It is also possible to introduce a programmable delay between different microphones (beamforming feature). DFSDM features optional parallel data stream inputs from microcontrollers memory (through DMA/CPU transfers into DFSDM).

DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators). DFSDM digital filter modules perform digital processing according user selected filter parameters with up to 24-bit final ADC resolution.

Table 8. DFSDM feature comparison

DFSDM instance	External input serial channels	External input parallel channels	Digital filters
DFSDM1	4	2	2
DFSDM2	8	4	4

3.30 Dynamic tuning of PDM delays for sound source localization

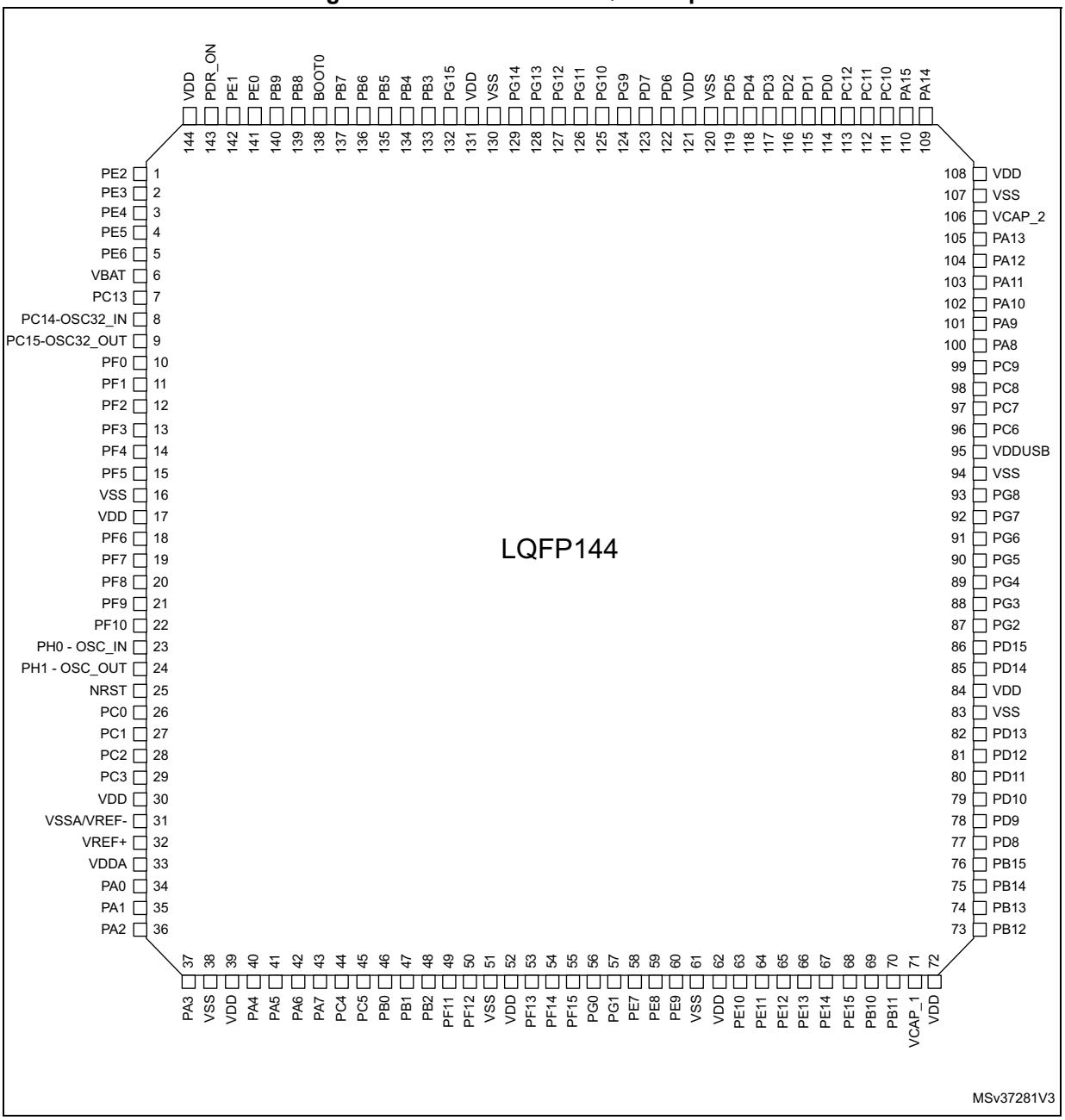
A mechanism is implemented on top of the DFSDM allowing to dynamically tune PDM delays of each microphone without the need to add external delay lines.

Audio application with several microphones require strong microphones placement constraints, as the distance between the microphones must be a multiple of v/F where v is the speed of the sound and F is the PCM sampling frequency.

The designed mechanism removes this constraint by programming delays for each digital microphone with the granularity of the PDM clock rate prior to the conversion into PCM rate.

The tuning delay is performed by a clock skipping technique.

Figure 15. STM32F423xH LQFP144 pinout



1. The above figure shows the package top view.

Table 10. STM32F423xH pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
28	36	H1	54	K10	L12	76	PB15	I/O	FTf	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, I2CFMP1_SCL, SPI2_MOSI/I2S2_SD, DFSDM1_CKIN2, TIM12_CH2, SDIO_CK, EVENTOUT	-
-	-	NC	55	-	L9	77	PD8	I/O	FT	(2)	USART3_TX, FSMC_D13/FSMC_DA13, EVENTOUT	-
-	-	F2	56	K8	K9	78	PD9	I/O	FT	-	USART3_RX, FSMC_D14/FSMC_DA14, EVENTOUT	-
-	-	G1	57	J12	J9	79	PD10	I/O	FT	(7)	USART3_CK, UART4_TX, FSMC_D15/FSMC_DA15, EVENTOUT	-
-	-	NC	58	J11	H9	80	PD11	I/O	FT	(2)	DFSDM2_DATIN2, I2CFMP1_SMBA, USART3_CTS, QUADSPI_BK1_IO0, FSMC_A16, EVENTOUT	-
-	-	NC	59	J10	L10	81	PD12	I/O	FTf	(2)	TIM4_CH1, DFSDM2_CKIN2, I2CFMP1_SCL, USART3_RTS, QUADSPI_BK1_IO1, FSMC_A17, EVENTOUT	-
-	-	NC	60	H12	K10	82	PD13	I/O	FTf	(2)	TIM4_CH2, I2CFMP1_SDA, QUADSPI_BK1_IO3, FSMC_A18, EVENTOUT	-
-	-	-	-	-	G8	83	VSS	S	-	-	-	-
-	-	-	-	-	F8	84	VDD	S	-	-	-	-
-	-	NC	61	H11	K11	85	PD14	I/O	FTf	(2)	TIM4_CH3, I2CFMP1_SCL, DFSDM2_CKIN0, UART9_RX, FSMC_D0/FSMC_DA0, EVENTOUT	-

Table 12. STM32F423xH alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/2/ LPTIM1	TIM3/4/5	DFSDM2/ TIM8/9/10/11	I2C1/2/3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2	SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3	DFSDM1/ USART3/4/ 5/6/7/8/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI	SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS	UART4/ UART5/ UART9/ UART10 /CAN3	FSMC /SDIO	-	RNG	SYS_AF
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	SPI5_SCK/I2S5_CK	-	-	-	-	-	-	-	-	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	SPI5_NSS/I2S5_WS	-	DFSDM1_DATIN0	QUADSPI_CLK	-	-	-	-	-	EVENTOUT
	PB2	-	LPTIM1_OUT	-	-	-	-	DFSDM1_CKIN0	-	-	QUADSPI_CLK	-	-	-	-	-	EVENTOUT
	PB3	JTDO-SWO	TIM2_CH2	-	-	I2CFMP1_SDA	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	USART1_RX	UART7_RX	I2C2_SDA	SAI1_SD_A	CAN3_RX	-	-	-	EVENTOUT
	PB4	JTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	I2S3ext_SD	UART7_TX	I2C3_SDA	SAI1_SCK_A	CAN3_TX	SDIO_D0	-	-	EVENTOUT
	PB5	-	LPTIM1_IN1	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI/I2S1_SD	SPI3_MOSI/I2S3_SD	-	-	CAN2_RX	SAI1_FS_A	UART5_RX	SDIO_D3	-	-	EVENTOUT
	PB6	-	LPTIM1_ETR	TIM4_CH1	-	I2C1_SCL	-	DFSDM2_CKIN7	USART1_TX	-	CAN2_TX	QUADSPI_BK1_NCS	UART5_TX	SDIO_D0	-	-	EVENTOUT
	PB7	-	LPTIM1_IN2	TIM4_CH2	-	I2C1_SDA	-	DFSDM2_DATIN7	USART1_RX	-	-	-	-	FSMC_NL	-	-	EVENTOUT
	PB8	-	LPTIM1_OUT	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	SPI5_MOSI/I2S5_SD	DFSDM2_CKIN1	CAN1_RX	I2C3_SDA	-	UART5_RX	SDIO_D4	-	-	EVENTOUT
	PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS/I2S2_WS	DFSDM2_DATIN1	-	CAN1_TX	I2C2_SDA	-	UART5_TX	SDIO_D5	-	-	EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK/I2S2_CK	I2S3_MCK	USART3_TX	-	I2CFMP4_SCL	DFSDM2_CKOUT	-	SDIO_D7	-	-	EVENTOUT
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	I2S2_CKIN	-	USART3_RX	-	-	-	-	-	-	-	EVENTOUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS/I2S2_WS	SPI4_NSS/I2S4_WS	SPI3_SCK/I2S3_CK	USART3_CK	CAN2_RX	DFSDM1_DATIN1	UART5_RX	FSMC_D13/FSMC_DA13	-	-	EVENTOUT
	PB13	-	TIM1_CH1N	-	-	I2CFMP1_SMBA	SPI2_SCK/I2S2_CK	SPI4_SCK/I2S4_CK	-	USART3_CTS	CAN2_TX	DFSDM1_CKIN1	UART5_TX	-	-	-	EVENTOUT
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	I2CFMP1_SDA	SPI2_MISO	I2S2ext_SD	USART3_RTS	DFSDM1_DATIN2	TIM12_CH1	FSMC_D0/FSMC_DA0	-	SDIO_D6	-	-	EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	I2CFMP1_SCL	SPI2_MOSI/I2S2_SD	-	-	DFSDM1_CKIN2	TIM12_CH2	-	-	SDIO_CK	-	-	EVENTOUT

Table 27. Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON(2), all peripherals enabled(3)	100	39.9	42.46	43.17	45.32	49.19	mA
			84	32.6	34.71	35.45	37.58	41.24	
			64	24.2	25.86	26.73	28.47	31.96	
			50	19.7	21.01	22.00	23.74	27.26	
			25	10.8	11.55	12.83	14.66	18.03	
			20	9.2	9.82	11.16	13.09	16.36	
		HSI, PLL OFF, all peripherals enabled(3)	16	6.8	7.33	8.77	10.69	14.00	
			1	1.2	1.83	3.08	4.83	8.19	
		External clock, PLL ON(2) all peripherals disabled(3)	100	22.3	24.11	25.26	27.35	31.11	
			84	18.5	20.00	21.15	23.20	26.87	
			64	14.6	15.81	17.02	18.74	22.20	
			50	12.2	13.14	14.45	16.18	19.66	
			25	7.0	7.52	8.95	10.84	14.19	
			20	6.0	6.58	7.95	9.74	13.07	
		HSI, PLL OFF, all peripherals disabled(3)	16	4.5	4.97	6.40	8.30	11.59	
			1	1.0	1.61	2.94	4.65	8.05	

1. Guaranteed by characterization results.
2. Refer to *Table 47* and RM0383 for the possible PLL VCO setting
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 59. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
I_{lkg}	I/O input leakage current (4)		$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA
	I/O FT/TC input leakage current (5)		V_{IN} = 5 V	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(6)	All pins except for PA10 (OTG_FS_ID)	$V_{IN} = V_{SS}$	30	40	50	kΩ
		PA10 (OTG_FS_ID)	-	7	10	14	
R_{PD}	Weak pull-down equivalent resistor(7)	All pins except for PA10 (OTG_FS_ID)	$V_{IN} = V_{DD}$	30	40	50	
		PA10 (OTG_FS_ID)	-	7	10	14	
C_{IO}(8)	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by test in production.
2. Guaranteed by design.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 58: I/O current injection susceptibility*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 58: I/O current injection susceptibility*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT and TC I/Os is shown in *Figure 35*.

Table 75. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_S(2)	Sampling rate (f_{ADC} = 30 MHz, and t_S = 3 ADC cycles)	12-bit resolution Single ADC	-	-	2	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	3.75	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	6	Msps
I_{VREF+}(2)	ADC V_{REF} DC current consumption in conversion mode	-	-	300	500	µA
I_{VDDA}(2)	ADC V_{DDA} DC current consumption in conversion mode	-	-	1.6	1.8	mA

1. V_{DDA} minimum value of 1.7 V is possible with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
2. Guaranteed by characterization results.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. R_{ADC} maximum value is given for V_{DD}=1.7 V, and minimum value for V_{DD}=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 75*.

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 76. ADC accuracy at f_{ADC} = 18 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} =18 MHz V_{DDA} = 1.7 to 3.6 V V_{REF} = 1.7 to 3.6 V $V_{DDA} - V_{REF}$ < 1.2 V	±3	±4	LSB
EO	Offset error		±2	±3	
EG	Gain error		±1	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±2	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization results.

6.3.22 V_{BAT} monitoring characteristics

Table 83. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat}(2)(2)	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.23 Embedded reference voltage

The parameters given in *Table 84* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 84. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +125 °C	1.18	1.21	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	10	-	-	µs
V_{RERINT_s}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3V ± 10mV	-	3	5	mV
T_{Coeff}(2)	Temperature coefficient	-	-	30	50	ppm/°C
t_{START}(2)	Startup time	-	-	6	10	µs

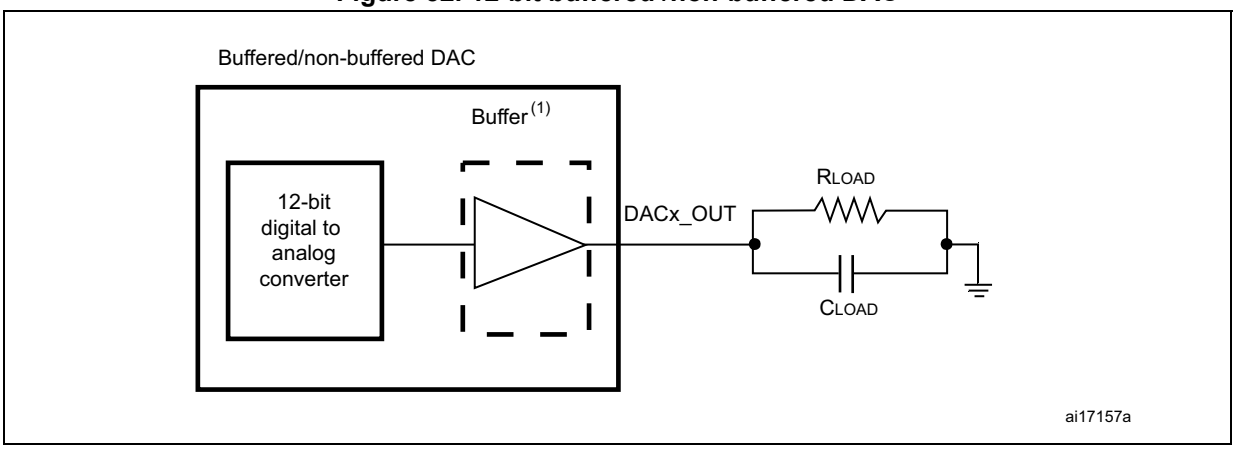
1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design

Table 85. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C V_{DDA} = 3.3 V	0x1FFF 7A2A - 0x1FFF 7A2B

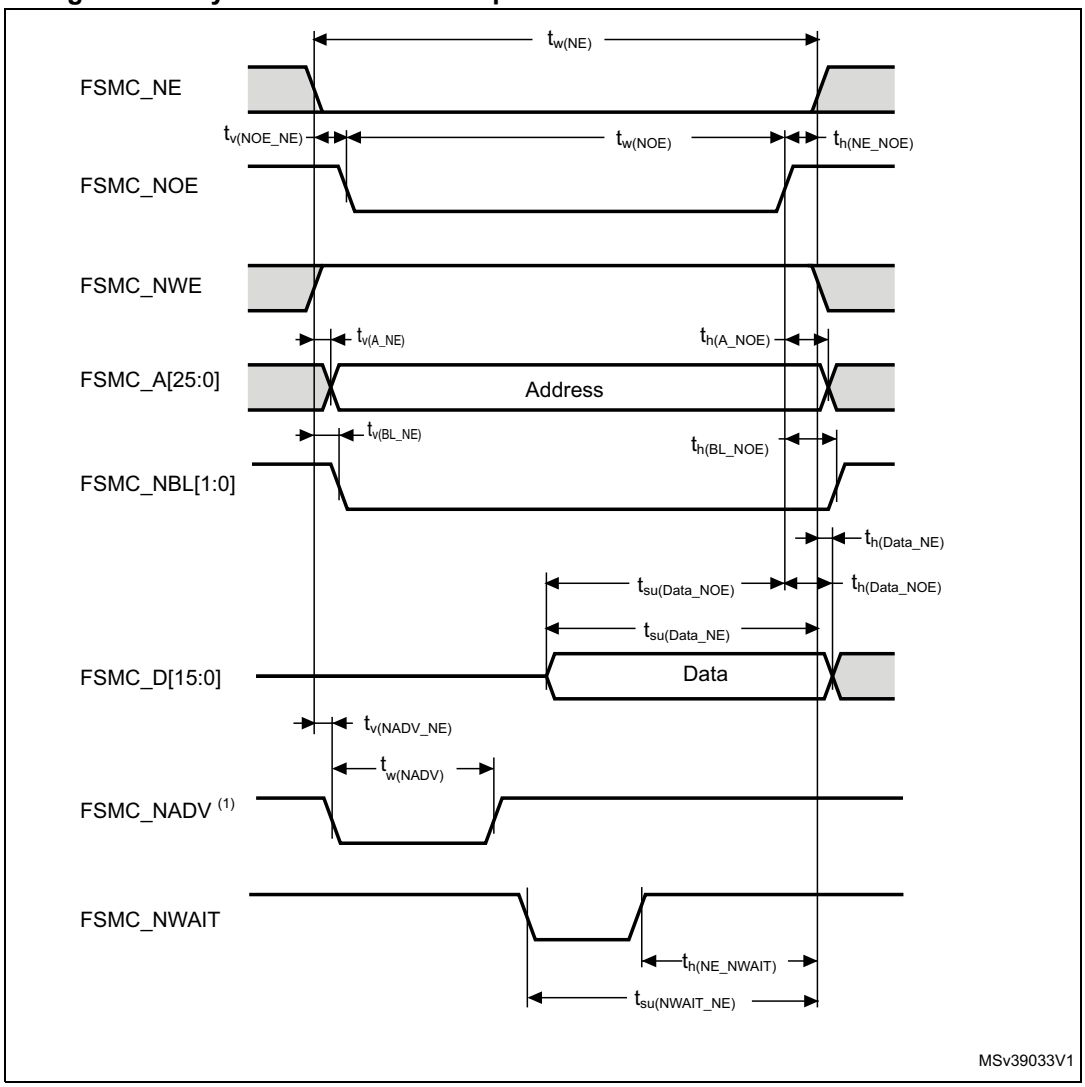
1. V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
2. Guaranteed by design.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization results.

Figure 52. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Figure 53. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 92. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3 * t_{HCLK} - 1$	$3 * t_{HCLK} + 1$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	$2 * t_{HCLK}$	$2 * t_{HCLK} + 0.5$	
$t_{w(NOE)}$	FSMC_NOE low time	$t_{HCLK} - 1$	$t_{HCLK} + 1$	
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0.5	
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	0	0.5	
$t_{w(NADV)}$	FSMC_NADV low time	$t_{HCLK} - 0.5$	$t_{HCLK} + 1$	
$t_{h(AD\_NADV)}$	FSMC_AD(address) valid hold time after FSMC_NADV high)	$t_{HCLK} + 0.5$	-	
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	$t_{HCLK} - 0.5$	-	
$t_{h(BL\_NOE)}$	FSMC_BL time after FSMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$t_{HCLK} - 2$	-	
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	$t_{HCLK} - 2$	-	
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	

1. C_L = 30 pF.
2. Based on characterization.

Table 93. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$8 * t_{HCLK} - 1$	$8 * t_{HCLK} + 1$	ns
$t_{w(NOE)}$	FSMC_NWE low time	$5 * t_{HCLK} - 1.5$	$5 * t_{HCLK} + 0.5$	
$t_{su(NWAIT\_NE)}$	FSMC_NWAIT valid before FSMC_NEx high	$5 * t_{HCLK} + 1.5$	-	
$t_{h(NE\_NWAIT)}$	FSMC_NEx hold time after FSMC_NWAIT invalid	$4 * t_{HCLK} + 1$	-	

1. C_L = 30 pF.
2. Based on characterization.

In all timing tables, the T_{HCLK} is the HCLK clock period (with maximum FSMC_CLK = 90 MHz).

Figure 57. Synchronous multiplexed NOR/PSRAM read timings

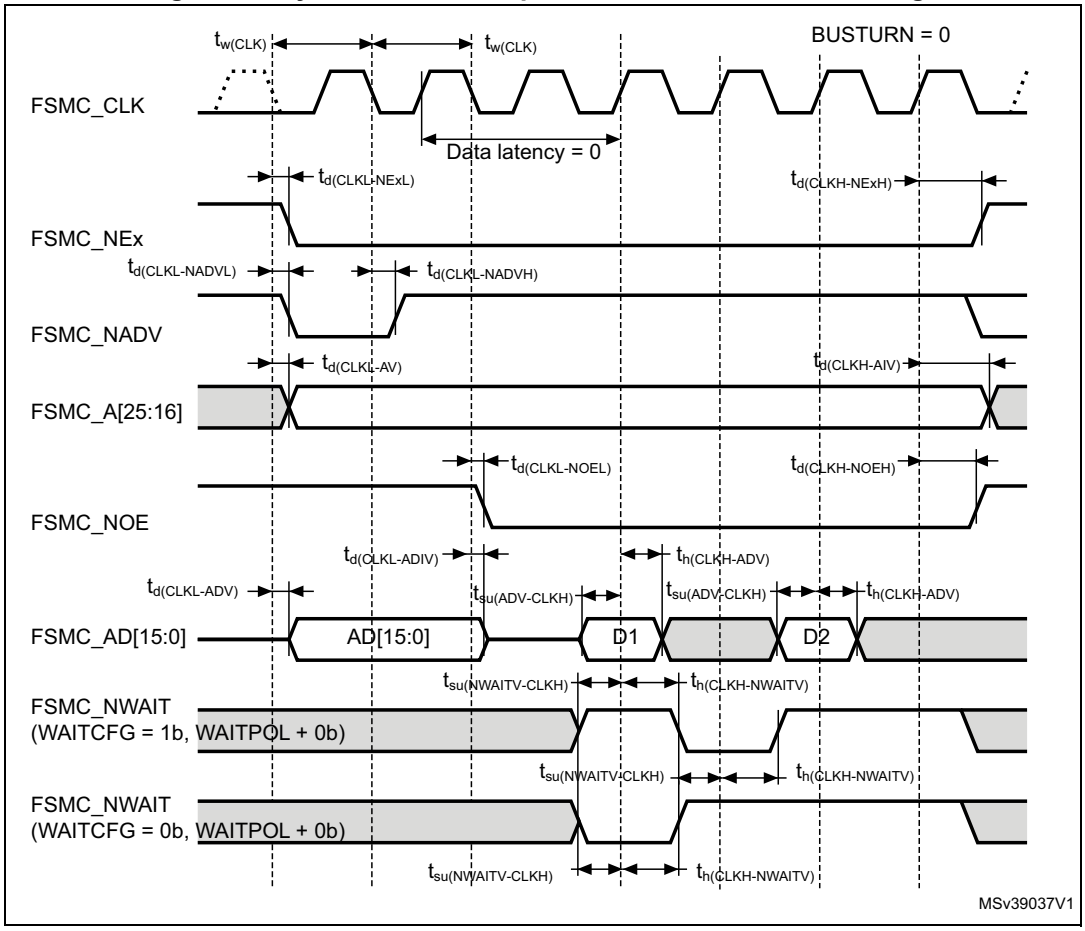
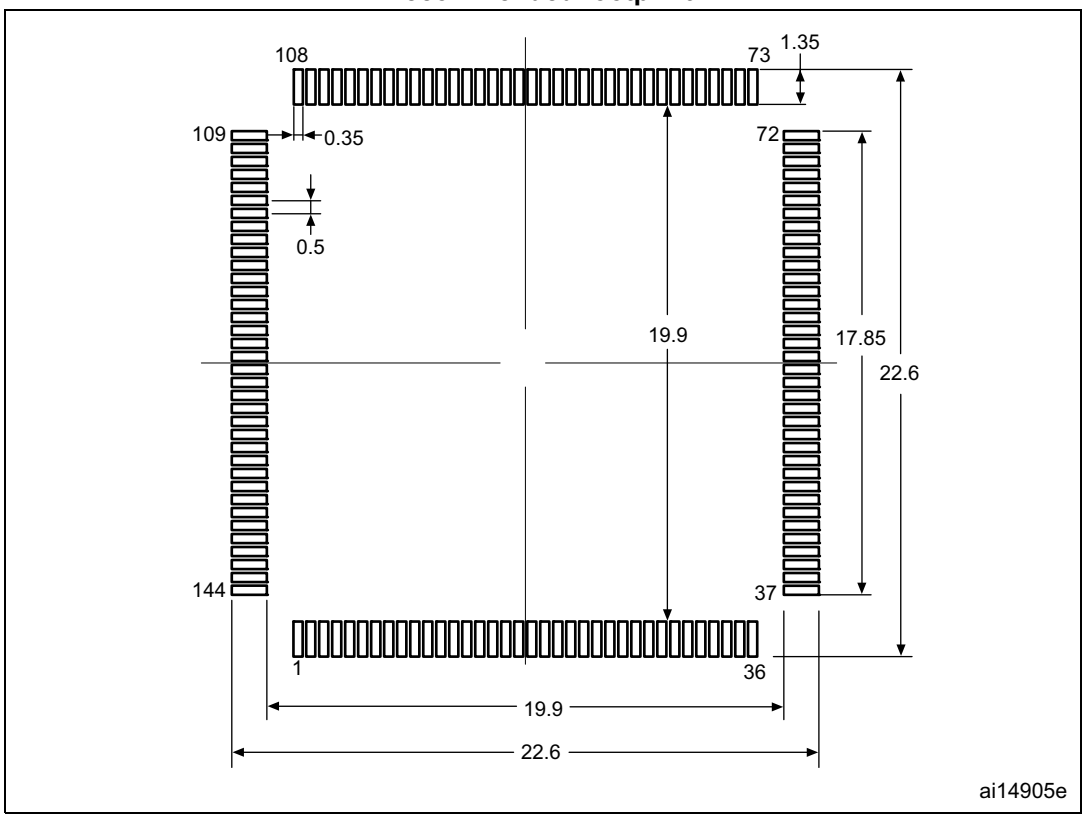


Figure 76. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Appendix B Application block diagrams

B.1 Sensor Hub application example

Figure 84. Sensor Hub application example