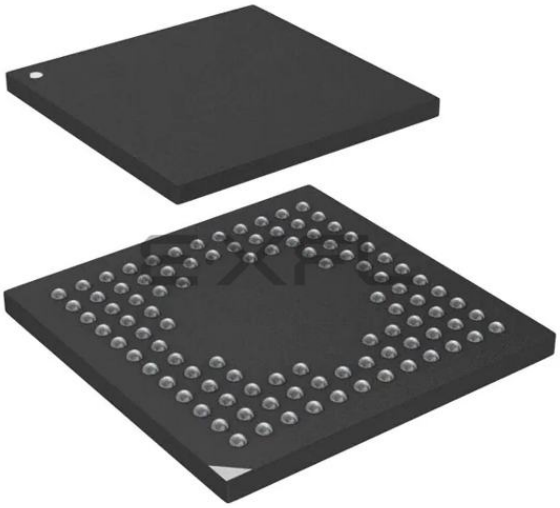

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f423vhh6

Contents

3 Functional overview

3.1 ARM® Cortex®-M4 with FPU core with embedded Flash and SRAM

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F423xH devices are compatible with all ARM tools and software.

Figure 4 shows the general block diagram of the STM32F423xH.

Note: Cortex®-M4 with FPU is binary compatible with Cortex®-M3.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 125 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 100 MHz.

3.3 Enhanced Batch Acquisition mode (eBAM)

The Batch acquisition mode allows enhanced power efficiency during data batching. It enables data acquisition through any communication peripherals directly to memory using the DMA in reduced power consumption as well as data processing while the rest of the system is in low-power mode (including the Flash and ART). For example in an audio system, a smart combination of PDM audio sample acquisition and processing from the DFSDM directly to RAM (Flash and ART™ stopped) with the DMA using BAM followed by some very short processing from Flash allows to drastically reduce the power consumption of the application.

The BAM has been enhanced by adding SRAM2 that allows SRAM code to be executed through the Ibus and Dbus, thus improving code execution performance.

3.16 Power supply schemes

- V_{DD} = 1.7 to 3.6 V: external power supply for I/Os with the internal supervisor (POR/PDR) disabled, provided externally through V_{DD} pins. Requires the use of an external power supply supervisor connected to the V_{DD} and NRST pins.
- V_{SSA}, V_{DDA} = 1.7 to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively, with decoupling technique.

Note: The V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to Section 3.17.2: Internal reset OFF). Refer to Table 4: Regulator ON/OFF and internal power supply supervisor availability to identify the packages supporting this option.

- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- V_{DDUSB} can be connected either to VDD or an external independent power supply (3.0 to 3.6 V) for USB transceivers.

  For example, when device is powered at 1.8 V, an independent power supply 3.3V can be connected to V_{DDUSB}. When the V_{DDUSB} is connected to a separated power supply, it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to disappear.

The following conditions VDDUSB must be respected:

- During power-on phase (V_{DD} < V_{DD_MIN}), V_{DDUSB} should be always lower than V_{DD}
- During power-down phase (V_{DD} < V_{DD_MIN}), V_{DDUSB} should be always lower than V_{DD}
- V_{DDUSB} rising and falling time rate specifications must be respected.
- In operating mode phase, V_{DDUSB} could be lower or higher than VDD:
  - If USB is used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DDUSB_MIN} and V_{DDUSB_MAX}.
  - If USB is not used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DD_MIN} and V_{DD_MAX}.

Table 10. STM32F423xH pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	9	C7	16	J2	H2	27	PC1	I/O	FT	-	LPTIM1_OUT, DFSDM2_DATIN4, SAI1_SD_B, EVENTOUT	ADC1_IN11, WKUP3
-	10	D7	17	J3	H3	28	PC2	I/O	FT	-	LPTIM1_IN2, DFSDM2_DATIN7, SPI2_MISO, I2S2ext_SD, SAI1_SCK_B, DFSDM1_CKOUT, FSMC_NWE, EVENTOUT	ADC1_IN12
-	11	E7	18	K2	H4	29	PC3	I/O	FT	-	LPTIM1_ETR, DFSDM2_CKIN7, SPI2_MOSI/I2S2_SD, SAI1_FS_B, FSMC_A0, EVENTOUT	ADC1_IN13
-	-	-	19	-	-	30	VDD	S	-	-	-	-
8	12	H9	20	J1	J1	31	VSSA	S	-	-	-	-
-	-	-	-	K1	K1	-	VREF-	S	-	-	-	-
-	-	G8	21	L1	L1	32	VREF+	S	-	-	-	-
9	13	F7	22	M1	M1	33	VDDA	S	-	-	-	-
10	14	G7	23	L2	J2	34	PA0	I/O	FT	-	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, EVENTOUT	ADC1_IN0, WKUP1
11	15	H8	24	M2	K2	35	PA1	I/O	FT	-	TIM2_CH2, TIM5_CH2, SPI4_MOSI/I2S4_SD, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, EVENTOUT	ADC1_IN1
12	16	J9	25	K3	L2	36	PA2	I/O	FT	-	TIM2_CH3, TIM5_CH3, TIM9_CH1, I2S2_CKIN, USART2_TX, FSMC_D4/FSMC_DA4, EVENTOUT	ADC1_IN2
13	17	E6	26	L3	M2	37	PA3	I/O	FT	-	TIM2_CH4, TIM5_CH4, TIM9_CH2, I2S2_MCK, USART2_RX, SAI1_SD_B, FSMC_D5/FSMC_DA5, EVENTOUT	ADC1_IN3

Table 10. STM32F423xH pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
28	36	H1	54	K10	L12	76	PB15	I/O	FTf	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, I2CFMP1_SCL, SPI2_MOSI/I2S2_SD, DFSDM1_CKIN2, TIM12_CH2, SDIO_CK, EVENTOUT	-
-	-	NC	55	-	L9	77	PD8	I/O	FT	(2)	USART3_TX, FSMC_D13/FSMC_DA13, EVENTOUT	-
-	-	F2	56	K8	K9	78	PD9	I/O	FT	-	USART3_RX, FSMC_D14/FSMC_DA14, EVENTOUT	-
-	-	G1	57	J12	J9	79	PD10	I/O	FT	(7)	USART3_CK, UART4_TX, FSMC_D15/FSMC_DA15, EVENTOUT	-
-	-	NC	58	J11	H9	80	PD11	I/O	FT	(2)	DFSDM2_DATIN2, I2CFMP1_SMBA, USART3_CTS, QUADSPI_BK1_IO0, FSMC_A16, EVENTOUT	-
-	-	NC	59	J10	L10	81	PD12	I/O	FTf	(2)	TIM4_CH1, DFSDM2_CKIN2, I2CFMP1_SCL, USART3_RTS, QUADSPI_BK1_IO1, FSMC_A17, EVENTOUT	-
-	-	NC	60	H12	K10	82	PD13	I/O	FTf	(2)	TIM4_CH2, I2CFMP1_SDA, QUADSPI_BK1_IO3, FSMC_A18, EVENTOUT	-
-	-	-	-	-	G8	83	VSS	S	-	-	-	-
-	-	-	-	-	F8	84	VDD	S	-	-	-	-
-	-	NC	61	H11	K11	85	PD14	I/O	FTf	(2)	TIM4_CH3, I2CFMP1_SCL, DFSDM2_CKIN0, UART9_RX, FSMC_D0/FSMC_DA0, EVENTOUT	-

Table 12. STM32F423xH alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/2/ LPTIM1	TIM3/4/5	DFSDM2/ TIM8/9/10/11	I2C1/2/3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2	SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3	DFSDM1/ USART3/4/ 5/6/7/8/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI	SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS	UART4/ UART5/ UART9/ UART10 /CAN3	FSMC /SDIO	-	RNG	SYS_AF
PortH	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.
4. Tested in production.

Table 39. Peripheral current consumption (continued)

Peripheral		I_{DD} (Typ)			Unit
		Scale 1	Scale 2	Scale 3	
APB2	AHB-APB2 bridge	0.10	0.11	0.09	µA/MHz
	TIM1	6.78	6.46	5.80	
	TIM8	6.94	6.62	5.94	
	USART1	3.14	3.00	2.69	
	USART6	3.12	2.98	2.67	
	UART9	2.89	1.98	1.75	
	UART10	2.91	2.00	1.77	
	ADC1	3.45	3.29	2.95	
	SDIO	3.54	3.37	3.03	
	SPI1	1.52	1.46	1.31	
	SPI4	1.50	1.43	1.28	
	SYSCFG	0.58	0.55	0.50	
	EXT1	0.91	0.86	0.78	
	TIM9	2.95	2.81	2.53	
	TIM10	1.88	1.79	1.61	
	TIM11	1.86	1.77	1.59	
	SPI5	1.50	1.43	1.30	
	SAI	2.89	2.75	2.47	
	DFSDM1	4.43	4.21	3.80	
	DFSDM2	7.08	6.76	6.05	
Bus Matrix		4.06	3.87	3.45	

1. N is the number of stream enable (1...8).

6.3.7 Wakeup time from low-power modes

The wakeup times given in *Table 40* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0/PC0/PC1) pins are used to wakeup from Standby, Stop and Sleep modes.

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with IEC61967-2 standard which specifies the test board and the pin loading.

Table 55. EMI characteristics for LQFP144

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				8/100 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP144 package, conforming to IEC 61967-2, EEMBC, ART ON, all peripheral clocks enabled, clock dithering disabled.	0.1 to 30 MHz	13	dBµV
			30 to 130 MHz	21	
			130 MHz to 1 GHz	25	
			1 GHz to 2 GHz	19	
			EMI Level	4	-

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 71. QSPI dynamic characteristics in DDR mode(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(CKH)}$	QSPI clock high and low time	-	$t_{(CK)}$ / 2 - 1	-	$t_{(CK)}$ / 2	ns
$t_{w(CKL)}$			$t_{(CK)}$ / 2	-	$t_{(CK)}$ / 2 + 1	
$t_{sr(IN)}$, $t_{sf(IN)}$	Data input setup time	2.7 V < V_{DD} < 3.6 V	0.5	-	-	
		1.71 V < V_{DD} < 3.6 V	0.5	-	-	
$t_{hr(IN)}$, $t_{hf(IN)}$	Data input hold time	2.7 V<V_{DD}<3.6 V	2	-	-	
		1.71 V<V_{DD}<3.6 V	2	-	-	
$t_{vr(OUT)}$, $t_{vf(OUT)}$	Data output valid time	2.7 V<V_{DD}<3.6 V	-	8.5	9	
		1.71 V<V_{DD}<3.6 V	-	8.5	11.5	
$t_{hr(OUT)}$, $t_{hf(OUT)}$	Data output hold time	-	7.5	-	-	

1. Guaranteed by characterization results.

USB OTG full speed (FS) characteristics

This interface is present in USB OTG FS controller.

Table 72. USB OTG FS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG FS transceiver startup time	1	µs

1. Guaranteed by design.

Table 73. USB OTG FS DC electrical characteristics

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input levels	V_{DD}	USB OTG FS operating voltage		3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I(USB_FS_DP/DM)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold		1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}		PA11, PA12 (USB_FS_DM/DP)	V_{IN} = V_{DD}	17	21	24	kΩ
		PA9 (OTG_FS_VBUS)		0.65	1.1	2.0	
R_{PU}		PA11, PA12 (USB_FS_DM/DP)	V_{IN} = V_{SS}	1.5	1.8	2.1	
		PA9 (OTG_FS_VBUS)	V_{IN} = V_{SS}	0.25	0.37	0.55	

1. All the voltages are measured from the local ground potential.

2. The USB OTG FS functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design.
4. R_L is the load connected on the USB OTG FS drivers.

Note: When VBUS sensing feature is enabled, PA9 should be left at their default state (floating input), not as alternate function. A typical 200 µA current consumption of the embedded sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 when the feature is enabled.

Figure 47. USB OTG FS timings: definition of data signal rise and fall time

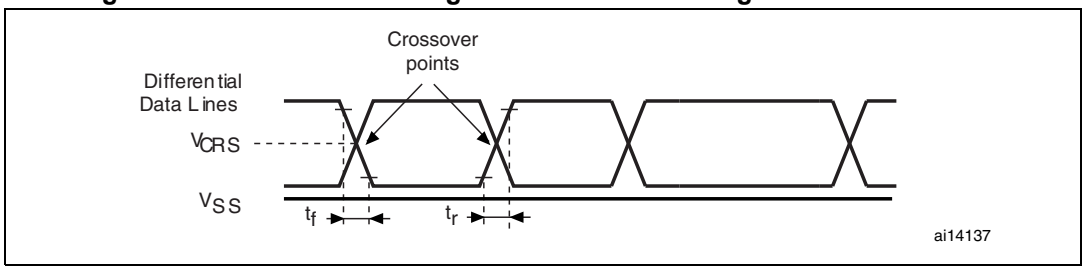


Table 74. USB OTG FS electrical characteristics(1)

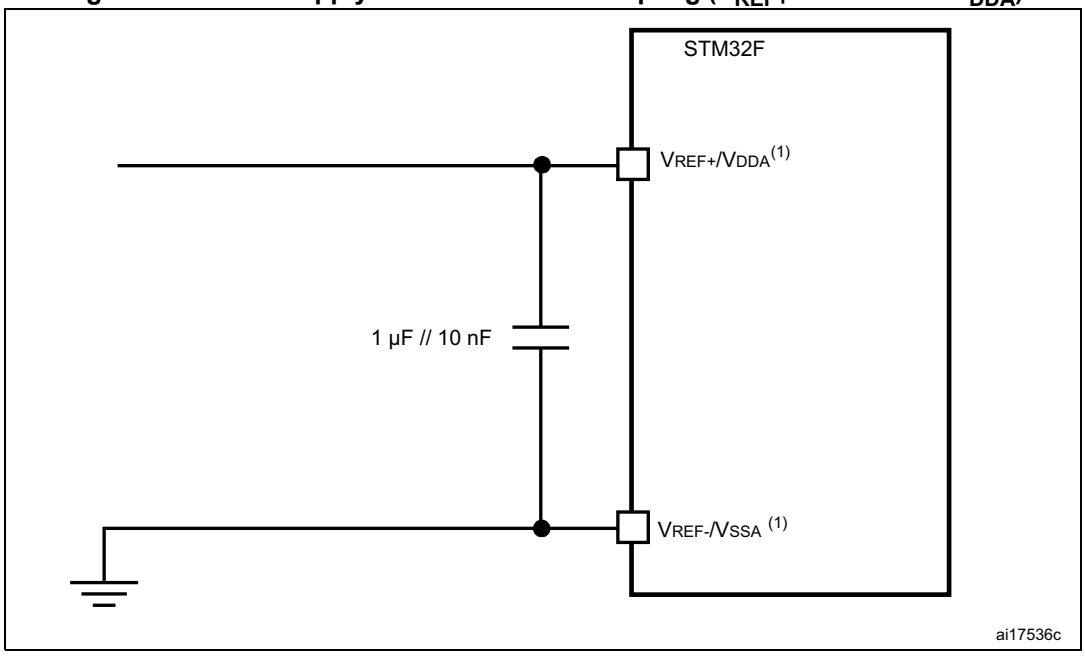
Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, refer to USB Specification - Chapter 7 (version 2.0).

CAN (controller area network) interface

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

Figure 51. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA100. V_{REF+} is also available on LQFP100. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

6.3.21 Temperature sensor characteristics

Table 81. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5	-	mV/°C
V_{25}(1)	Voltage at 25 °C	-	0.76	-	V
t_{START}(2)	Startup time	-	6	10	µs
T_{S_temp}(2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	µs

1. Guaranteed by characterization results.
2. Guaranteed by design.

Table 82. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF 7A2C - 0x1FFF 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C, V_{DDA}= 3.3 V	0x1FFF 7A2E - 0x1FFF 7A2F

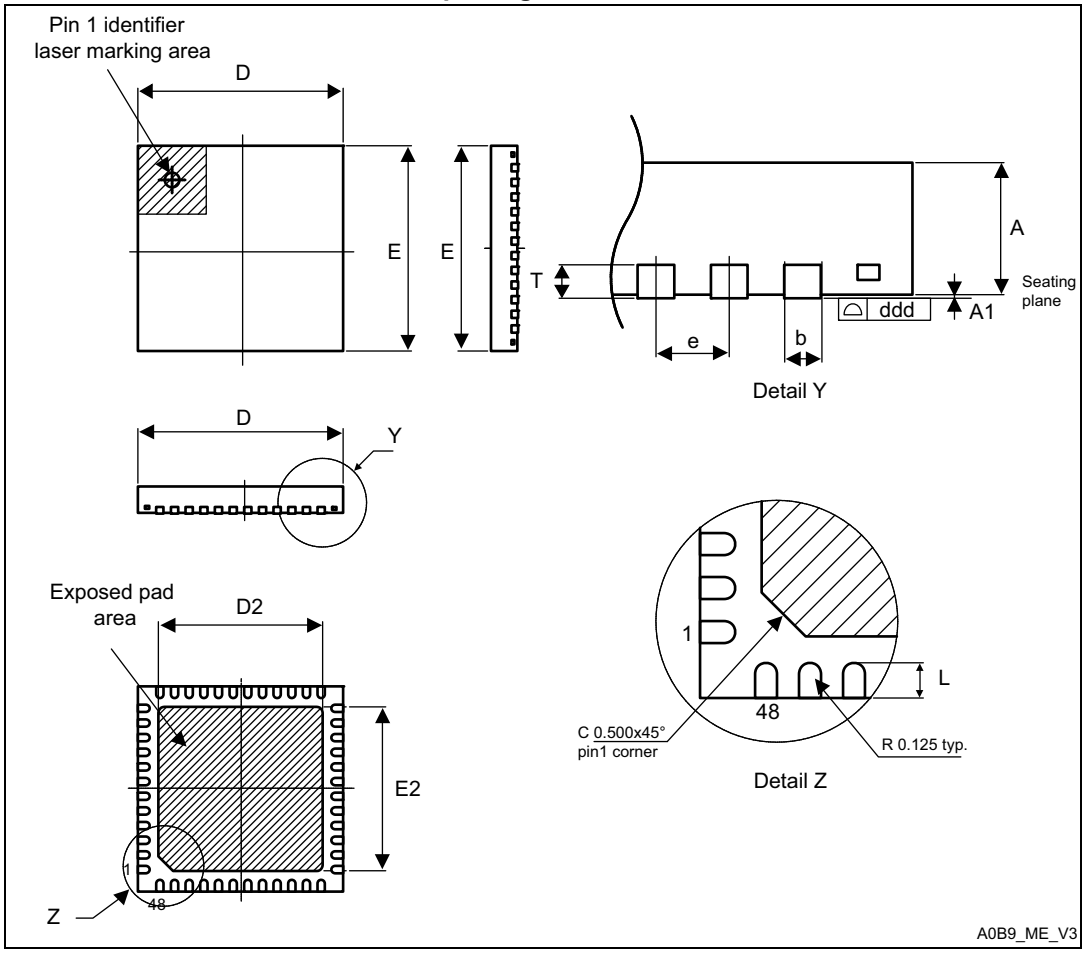
Table 97. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period, V_{DD} range= 2.7 to 3.6 V	2 * T_{HCLK} - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x= 0...2)	-	2	
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high (x= 0…2)	T_{HCLK} + 0.5	-	
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	2.5	
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1.5	
$t_{(CLKH-NWEH)}$	FSMC_CLK high to FSMC_NWE high	T_{HCLK} + 0.5	-	
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FSMC_A/D[15:0] valid data after FSMC_CLK low	-	4	
$t_{d(CLKL-NBLL)}$	FSMC_CLK low to FSMC_NBL low	0	2	
$t_{d(CLKH-NBLH)}$	FSMC_CLK high to FSMC_NBL high	T_{HCLK} + 0.5	-	
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	3.5	-	

1. C_L = 30 pF.
2. Guaranteed by characterization results.

7.2 UFQFPN48 package information

Figure 66. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



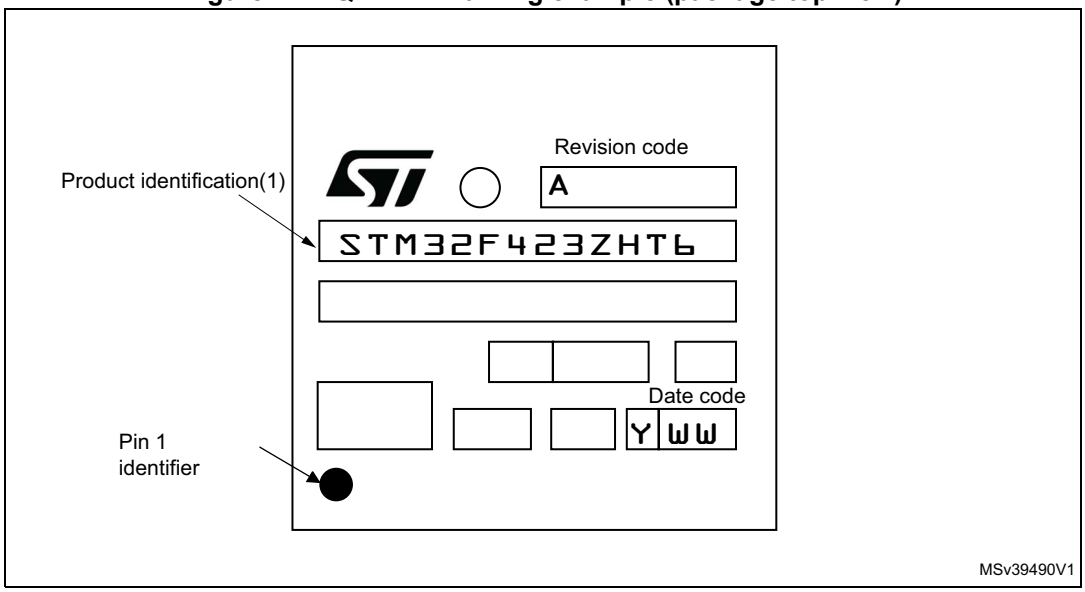
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Device marking for LQFP144

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

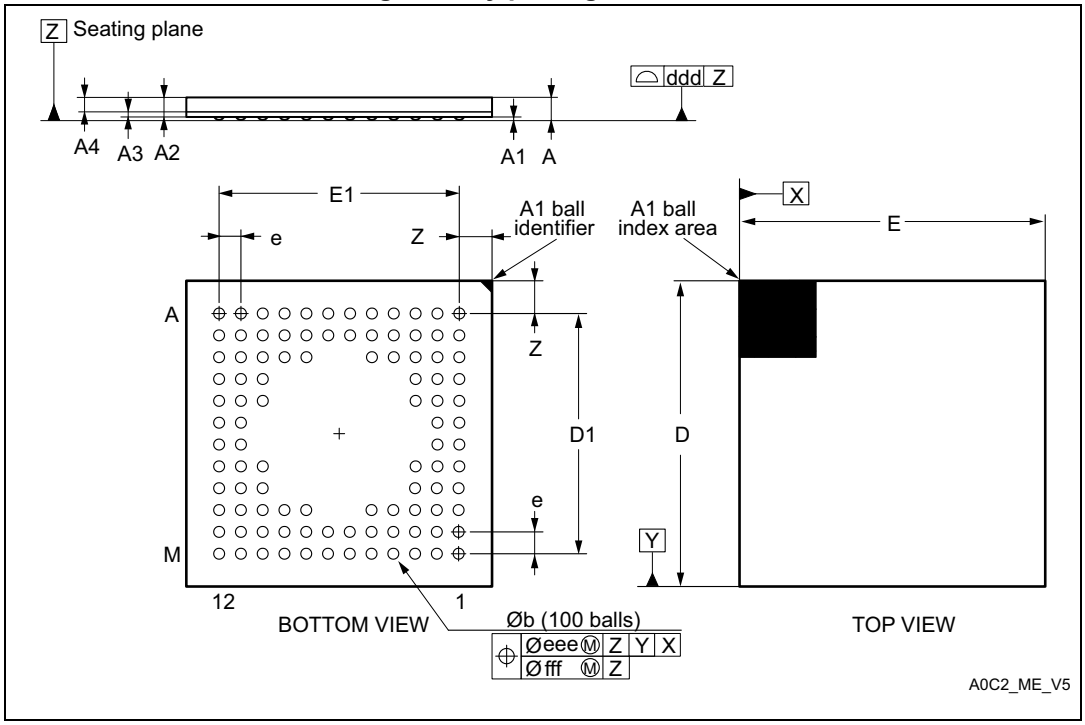
Figure 77. LQFP144 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.6 UFBGA100 package information

Figure 78. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 109. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-

Table 111. UFBGA144 - 144-ball, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
F	0.550	0.600	0.650	0.0177	0.0197	0.0217
ddd	-	-	0.080	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 82. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array recommended footprint

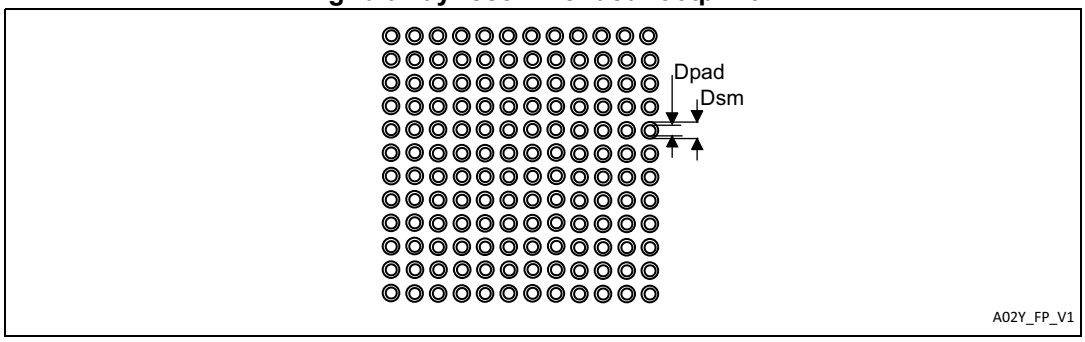


Table 112. UFBGA144 recommended PCB design rules (0.80 mm pitch BGA)

Dimension	Recommended values
Pitch	0.80 mm
Dpad	0.400 mm
Dsm	0.550 mm typ. (depends on the soldermask registration tolerance)

Note: Non solder mask defined (NSMD) pads are recommended.

4 to 6 mils solder paste screen printing process.

Stencil opening is 0.400 mm.

Stencil thickness is between 0.100 mm and 0.125 mm.

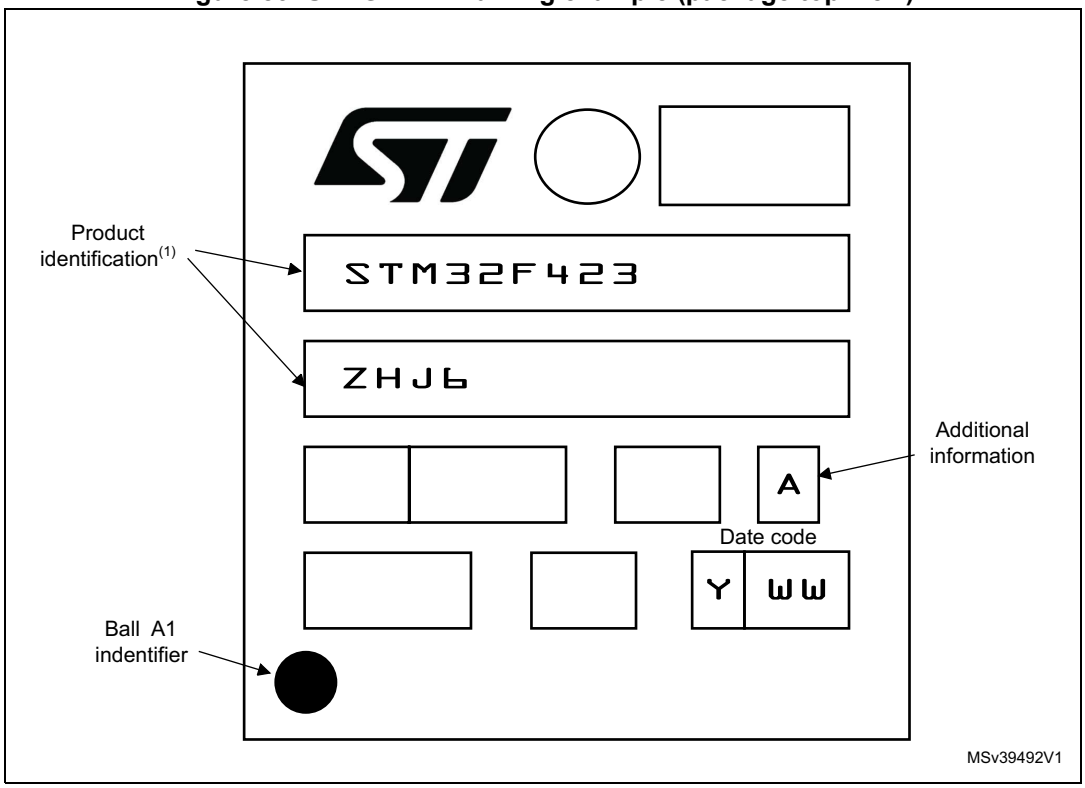
Pad trace width is 0.120 mm.

Device marking for UFBGA144

The following figure gives an example of topside marking and ball A1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

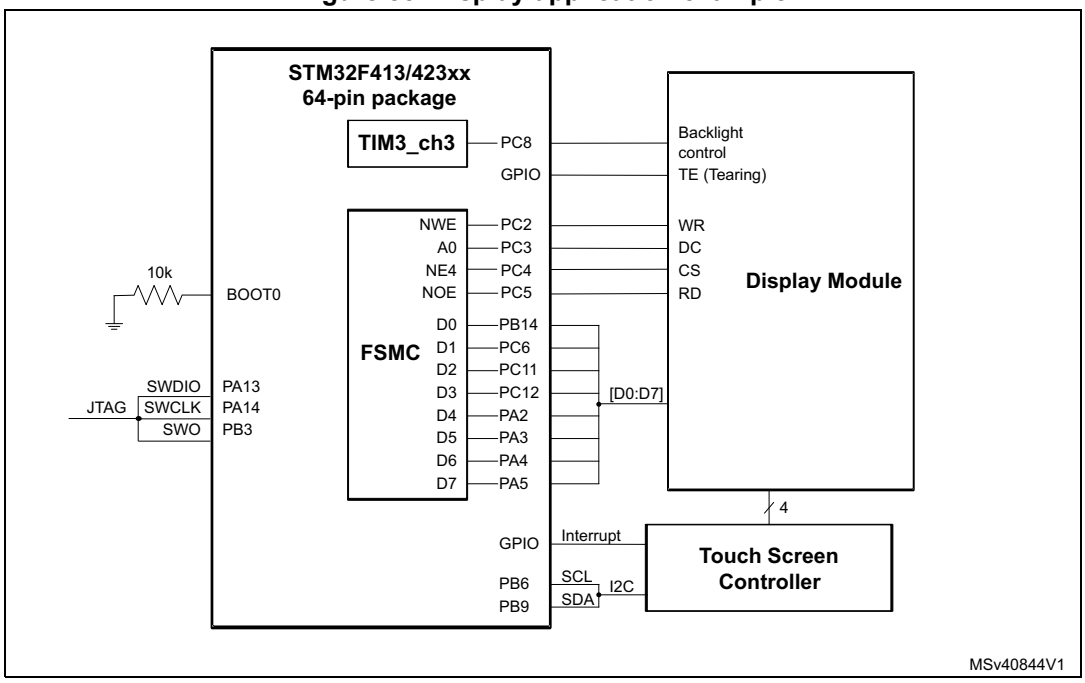
Figure 83. UFBGA144 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

B.2 Display application example

Figure 85. Display application example



Note: 16 bit displays interfaces can be addressed with 100 and 144 pins packages.

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