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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f423vht6

1 Introduction

This datasheet provides the description of the STM32F423xH microcontrollers.

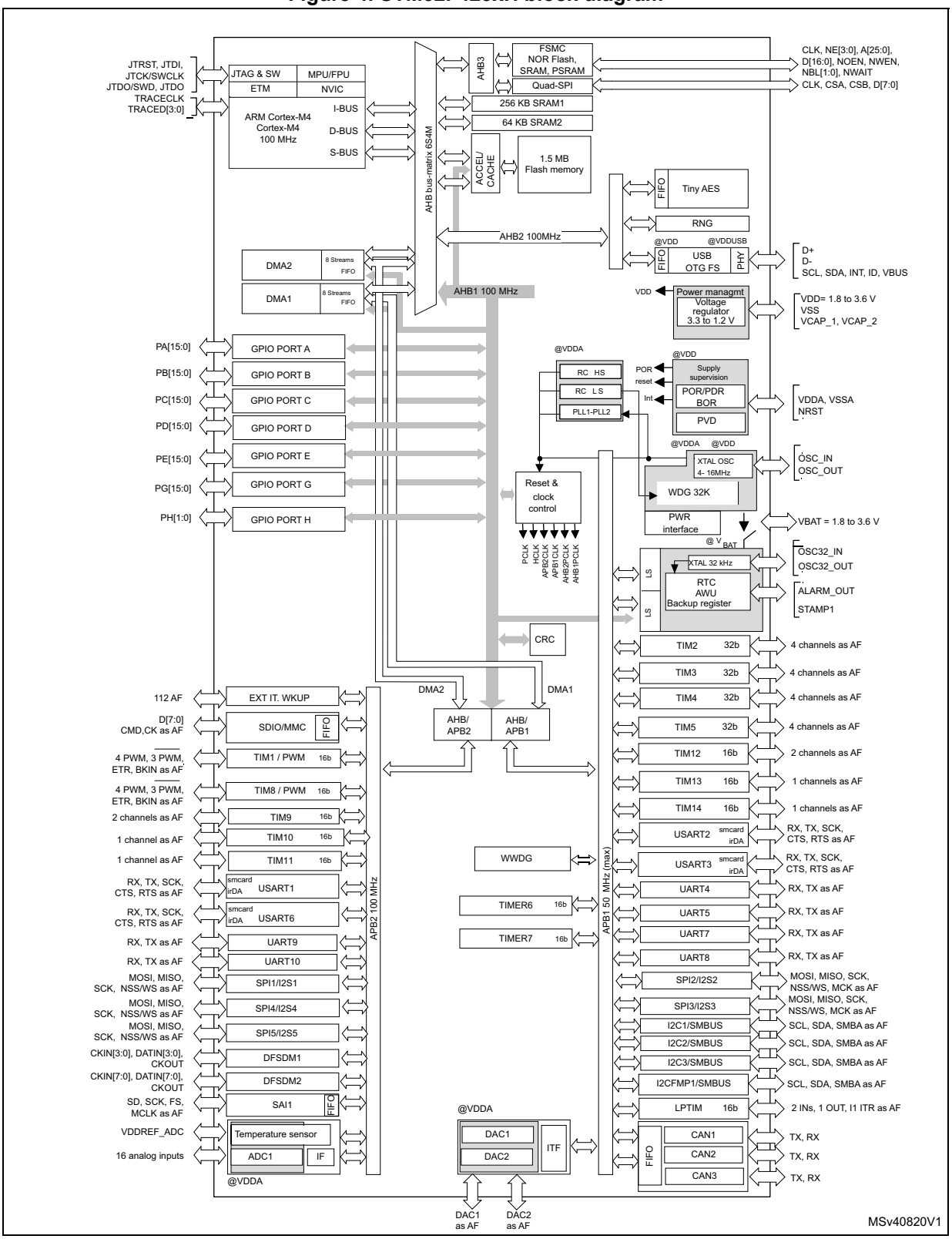
For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214) available from *www.st.com*.

These features make the STM32F423xH microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile phone sensor hub
- Wearable devices
- Connected objects
- Wifi modules

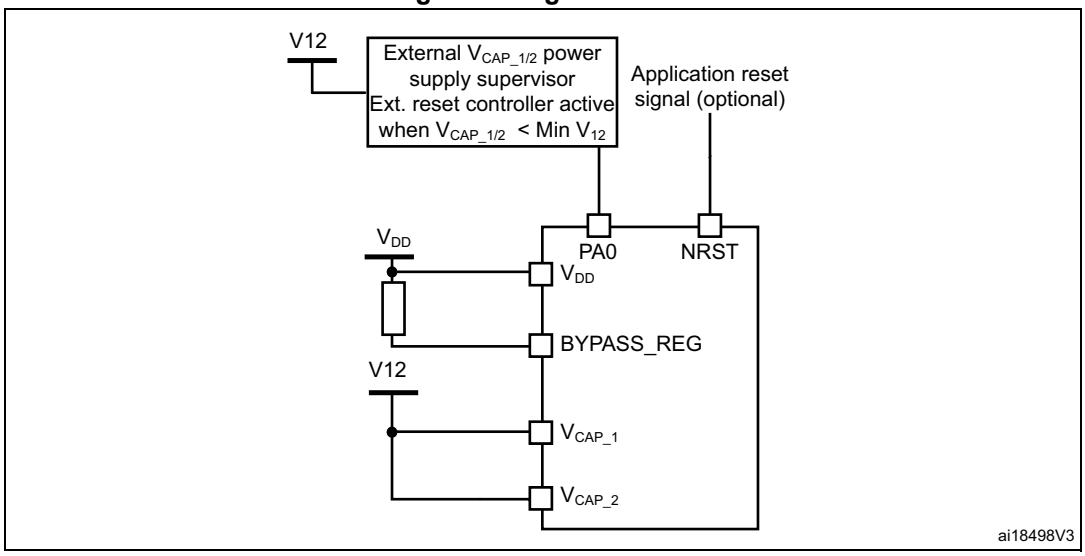
Figure 4 shows the general block diagram of the devices.

Figure 4. STM32F423xH block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 100 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 50 MHz.

Figure 8. Regulator OFF



The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V_{12} minimum value and until V_{DD} reaches 1.7 V (see *Figure 9*).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally (see *Figure 10*).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application.

Table 10. STM32F423xH pin definition (continued)

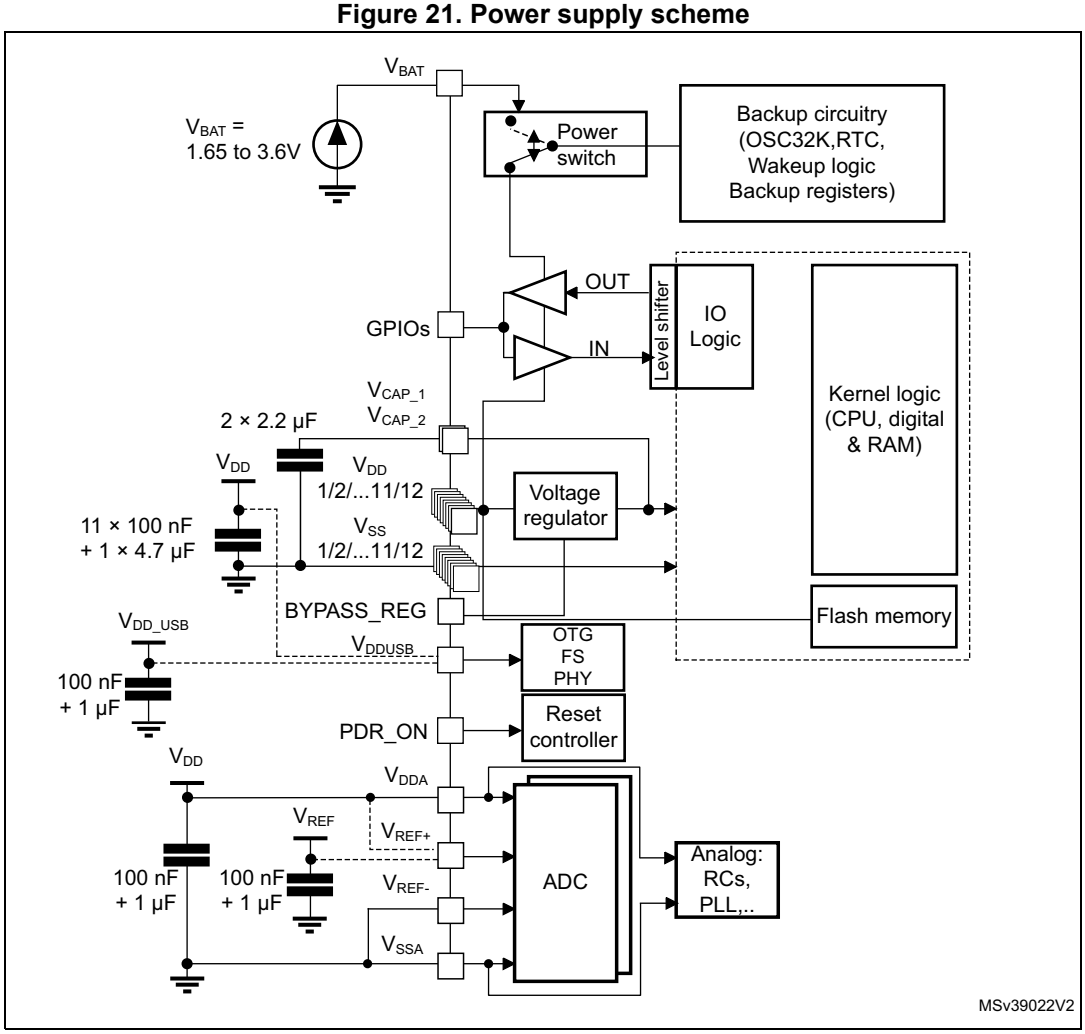
Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	39	E1	65	E10	F11	98	PC8	I/O	FT	-	TIM3_CH3, TIM8_CH3, DFSDM2_CKIN3, USART6_CK, QUADSPI_BK1_IO2, SDIO_D0, EVENTOUT	-
-	40	E2	66	D12	E11	99	PC9	I/O	FT	-	MCO_2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S2_CKIN, DFSDM2_DATIN3, QUADSPI_BK1_IO0, SDIO_D1, EVENTOUT	-
29	41	D3	67	D11	E12	100	PA8	I/O	FT	-	MCO_1, TIM1_CH1, I2C3_SCL, DFSDM1_CKOUT, USART1_CK, UART7_RX, USB_FS_SOF, CAN3_RX, SDIO_D1, EVENTOUT	-
30	42	D2	68	D10	D12	101	PA9	I/O	FT	-	TIM1_CH2, DFSDM2_CKIN3, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, USB_FS_VBUS, SDIO_D2, EVENTOUT	-
31	43	D1	69	C12	D11	102	PA10	I/O	FT	-	TIM1_CH3, DFSDM2_DATIN3, SPI2_MOSI/I2S2_SD, SPI5_MOSI/I2S5_SD, USART1_RX, USB_FS_ID, EVENTOUT	-
32	44	C3	70	B12	C12	103	PA11	I/O	FT	-	TIM1_CH4, DFSDM2_CKIN5, SPI2_NSS/I2S2_WS, SPI4_MISO, USART1_CTS, USART6_TX, CAN1_RX, USB_FS_DM, UART4_RX, EVENTOUT	-

Table 12. STM32F423xH alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/2/ LPTIM1	TIM3/4/5	DFSDM2/ TIM8/9/10/11	I2C1/2/3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2	SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3	DFSDM1/ USART3/4/ 5/6/7/8/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI	SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS	UART4/ UART5/ UART9/ UART10 /CAN3	FSMC /SDIO	-	RNG	SYS_AF
Port C	PC0	-	LPTIM1_IN1	-	DFSDM2_CKIN4	-	-	-	SAI1_MCLK_B	-	-	-	-	-	-	-	EVENTOUT
	PC1	-	LPTIM1_OUT	-	DFSDM2_DATIN4	-	-	-	SAI1_SD_B	-	-	-	-	-	-	-	EVENTOUT
	PC2	-	LPTIM1_IN2	-	DFSDM2_DATIN7	-	SPI2_MISO	I2S2ext_SD	SAI1_SCK_B	DFSDM1_CKOUT	-	-	-	FSMC_NWE	-	-	EVENTOUT
	PC3	-	LPTIM1_ETR	-	DFSDM2_CKIN7	-	SPI2_MOSI/ I2S2_SD	-	SAI1_FS_B	-	-	-	-	FSMC_A0	-	-	EVENTOUT
	PC4	-	-	-	DFSDM2_CKIN2	-	I2S1_MCK	-	-	-	-	QUADSPI_BK2_IO2	-	FSMC_NE4	-	-	EVENTOUT
	PC5	-	-	-	DFSDM2_DATIN2	I2CFMP1_SMBA	-	-	USART3_RX	-	-	QUADSPI_BK2_IO3	-	FSMC_NOE	-	-	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	I2CFMP1_SCL	I2S2_MCK	DFSDM1_CKIN3	DFSDM2_DATIN6	USART6_TX	-	FSMC_D1/ FSMC_DA1	-	SDIO_D6	-	-	EVENTOUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	I2CFMP1_SDA	SPI2_SCK/ I2S2_CK	I2S3_MCK	DFSDM2_CKIN6	USART6_RX	-	DFSDM1_DATIN3	-	SDIO_D7	-	-	EVENTOUT
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	DFSDM2_CKIN3	USART6_CK	QUADSPI_BK1_IO2	-	-	SDIO_D0	-	-	EVENTOUT
	PC9	MCO_2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S2_CKIN	-	DFSDM2_DATIN3	-	QUADSPI_BK1_IO0	-	-	SDIO_D1	-	-	EVENTOUT
	PC10	-	-	-	DFSDM2_CKIN5	-	-	SPI3_SCK/ I2S3_CK	USART3_TX	-	QUADSPI_BK1_IO1	-	-	SDIO_D2	-	-	EVENTOUT
	PC11	-	-	-	DFSDM2_DATIN5	-	I2S3ext_SD	SPI3_MISO	USART3_RX	UART4_RX	QUADSPI_BK2_NCS	FSMC_D2/ FSMC_DA2	-	SDIO_D3	-	-	EVENTOUT
	PC12	-	-	-	-	-	-	SPI3_MOSI/ I2S3_SD	USART3_CK	UART5_TX	-	FSMC_D3/ FSMC_DA3	-	SDIO_CK	-	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

6.1.6 Power supply scheme

Figure 21. Power supply scheme



1. To connect PDR_ON pin, refer to Section: Power supply supervisor.
2. The 4.7 µF ceramic capacitor must be connected to one of the V_{DD} pin.
3. VCAP_2 pad is only available on 100-pin and 144-pin packages.
4. V_{DDA}=V_{DD} and V_{SSA}=V_{SS}.
5. V_{DDUSB} is a dedicated independent USB power supply for the on-chip full-speed OTG PHY module and associated DP/DM GPIOs. V_{DDUSB} value does not depend on the V_{DD} and V_{DDA} values, but it must be the last supply to be provided and the first to disappear.

Caution: Each power supply pair (for example V_{DD}/V_{SS}, V_{DDA}/V_{SSA}) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

Table 17. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage on RST, FT and TC pins(7)	2 V ≤ V_{DD} ≤ 3.6 V	–0.3	-	5.5	V
		V_{DD} ≤ 2 V	–0.3	-	5.2	
	Input voltage on TTa pins	-	- 0.3	-	V_{DDA} + 0.3	
	Input voltage on BOOT0 pin	-	0	-	9	
P_D	Power dissipation at TA = 85°C for range 6 or TA = 105°C for range 7(8)	UFQFPN48	-	-	625	mW
		WLCSP81	-	-	504	
		LQFP64	-	-	426	
		LQFP100	-	-	465	
		LQFP144		-	571	
		UFBGA100	-	-	351	
		UFBGA144	-	-	417	
	Power dissipation at TA = 125°C for range 3(8)	UFQFPN48	-	-	156	
		WLCSP81	-	-	126	
		LQFP64	-	-	106	
		LQFP100	-	-	116	
		LQFP144	-	-	143	
		UFBGA100	-	-	088	
		UFBGA144	-	-	104	
T_A	Ambient temperature for range 6	Maximum power dissipation	–40	-	85	°C
		Low power dissipation(9)	–40	-	105	
	Ambient temperature for range 7	Maximum power dissipation	–40	-	105	
		Low power dissipation(9)	–40	-	125	
	Ambient temperature for range 3	Maximum power dissipation	–40	-	125	
		Low power dissipation(9)	–40	-	130	
T_J	Junction temperature range	Range 6	–40	-	105	
		Range 7	–40	-	125	
		Range 3	–40	-	130	

1. V_{DD}/V_{DDA} minimum value of 1.7 V with the use of an external power supply supervisor (refer to *Section 3.17.2: Internal reset OFF*).
2. When the ADC is used, refer to *Table 75: ADC characteristics*.
3. If V_{REF+} pin is present, it must respect the following condition: V_{DDA}-V_{REF}+ < 1.2 V.
4. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
5. Only the DM (P_{A11}) and DP (P_{A12}) pads are supplied through V_{DDUSB}. For application where the V_{BUS} (P_{A9}) is directly connected to the chip, a minimum V_{DD} supply of 2.7V is required.
(some application examples are shown in appendix B)
6. Guaranteed by test in production
7. To sustain a voltage higher than V_{DD}+0.3, the internal Pull-up and Pull-Down resistors must be disabled

Table 22. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	
V_{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	
		Rising edge	2.53	2.59	2.63	
V_{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	
		Rising edge	2.85	2.92	2.97	
$V_{BORhyst}$(2)	BOR hysteresis	-	-	100	-	mV
$T_{RSTTEMPO}$(2)(3)	POR reset timing	-	0.5	1.5	3.0	ms
I_{RUSH}(2)	In-Rush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	160	200	mA
E_{RUSH}(2)	In-Rush energy on voltage regulator power-on (POR or wakeup from Standby)	V_{DD} = 1.7 V, T_A = 125 °C, I_{RUSH} = 171 mA for 31 µs	-	-	5.4	µC

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design.
3. The reset timing is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is fetched by the user application code.

6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 22: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Table 25. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory- V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)(3)	100	30.2	32.03	32.71	34.69	38.46	mA
			84	24.3	25.77	26.58	28.47	32.16	
			64	16.8	17.80	18.66	20.53	23.85	
			50	13.2	14.05	15.12	16.85	20.27	
			25	7.1	7.62	8.92	10.81	14.11	
			20	6.1	6.69	7.95	9.72	13.09	
		HSI, PLL OFF, all peripherals enabled(2)	16	4.4	4.99	6.28	8.18	11.45	
			1	0.9	1.50	2.88	4.58	8.00	
		External clock, PLL ON(4) all peripherals disabled(2)	100	12.6	13.46	14.75	16.68	20.54	
			84	10.2	10.90	12.25	14.10	17.84	
			64	7.2	7.70	8.95	10.81	14.14	
			50	5.7	6.26	7.56	9.26	12.72	
			25	3.2	3.77	5.11	6.82	10.26	
			20	2.9	3.41	4.79	6.49	9.92	
		HSI, PLL OFF, all peripherals disabled(2)	16	2.1	2.63	3.91	5.80	9.06	
			1	0.8	1.34	2.72	4.42	7.86	

1. Guaranteed by characterization results..
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.
4. Refer to *Table 47* and RM0383 for the possible PLL VCO setting

Table 31. Typical and maximum current consumption in Sleep mode - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Sleep mode**	All peripherals enabled(2)(3), External clock, PLL ON, Flash deep power down	100	21.6	22.97(4)	23.91	25.99	29.72	mA
			84	17.4	18.50	19.59	21.42	25.09	
			64	12.0	12.81	13.87	15.73	19.00	
			50	9.5	10.15	11.33	13.22	16.44	
			25	5.2	5.79	7.11	8.82	12.18	
			20	4.6	5.17	6.41	8.28	11.48	
		All peripherals enabled(2)(3), HSI, PLL OFF, Flash deep power down	16	3.0	3.24	4.78	6.60	9.94	
			1	0.7	0.76	2.41	4.23	7.55	
		All peripherals enabled(2)(3), External clock, PLL ON Flash ON	100	22.0	23.42	24.45	26.41	30.24	
			84	17.7	18.91	19.98	21.85	25.56	
			64	12.4	13.17	14.30	16.07	19.48	
			50	9.8	10.48	11.72	13.53	16.90	
			25	5.5	6.05	7.41	9.11	12.55	
			20	4.9	5.42	6.72	8.57	11.89	
		All peripherals enabled(2)(3), HSI, PLL ON, Flash ON	16	3.3	3.51	5.06	6.91	10.30	
			1	0.9	1.01	2.67	4.52	7.88	
		All peripherals disabled, External clock, PLL ON(2), Flash deep power down	100	3.5	4.17	5.56	7.54	11.23	
			84	2.9	3.48	4.94	6.76	10.40	
			64	2.2	2.73	3.94	5.80	8.98	
			50	1.8	2.38	3.57	5.42	8.60	
			25	1.3	1.86	3.11	4.82	8.12	
			20	1.3	1.90	3.13	4.85	8.15	
		All peripherals disabled, HSI, PLL OFF(2), Flash deep power down	16	0.6	0.68	2.33	4.16	7.47	
			1	0.5	0.59	2.24	4.07	7.38	
		All peripherals disabled, External clock, PLL ON(2), Flash ON	100	4.0	4.54	5.97	8.09	11.74	
			84	3.3	3.87	5.32	7.19	10.84	
			64	2.5	3.04	4.33	6.15	9.47	
			50	2.2	2.69	3.93	5.82	9.04	
			25	1.6	2.13	3.37	5.20	8.46	
			20	1.6	2.16	3.39	5.22	8.48	
		All peripherals disabled, HSI, PLL OFF(2), Flash ON	16	0.9	0.96	2.62	4.47	7.82	
			1	0.7	0.85	2.50	4.36	7.71	

1. Guaranteed by characterization results.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 67. SPI dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{a(SO)}$	Data output access time	Slave mode	7	-	21	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	5	-	12	ns
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge), 2.7 V < V_{DD} < 3.6 V	-	7	12.5	ns
		Slave mode (after enable edge), 1.71 V < V_{DD} < 3.6 V	-	7	19	
$t_{v(MO)}$		Master mode	-	2	3	
$t_{h(SO)}$	Data output hold time	Slave mode 1.71 V < V_{DD} < 3.6 V	6	-	-	ns
$t_{h(MO)}$		Master mode	1.5	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%

Figure 40. SPI timing diagram - slave mode and CPHA = 0

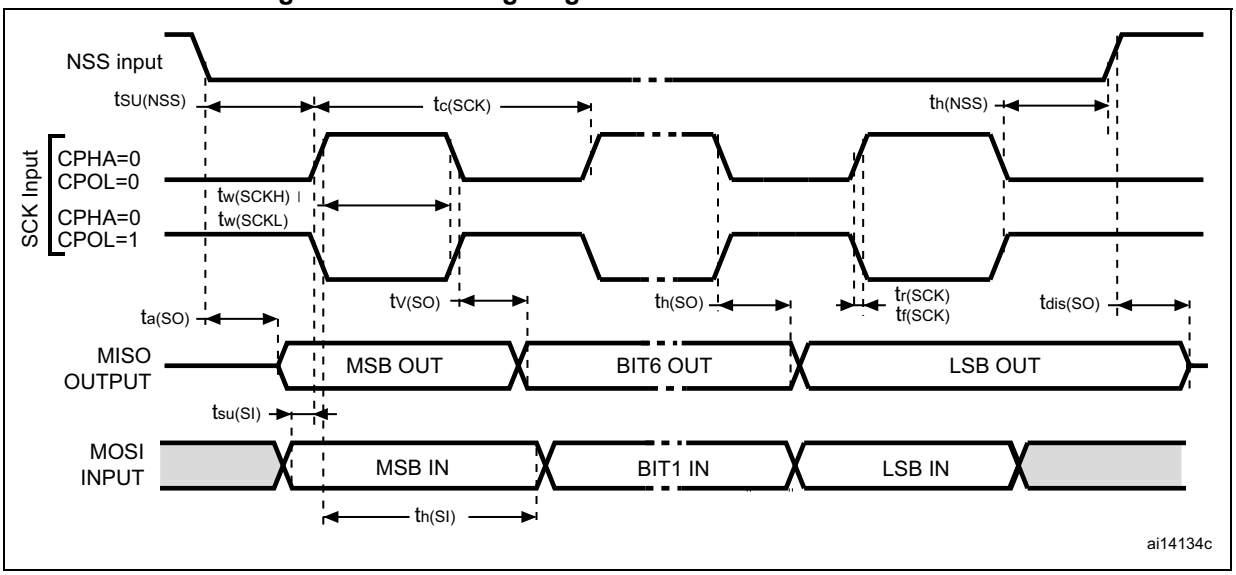


Figure 45. SAI master timing waveforms

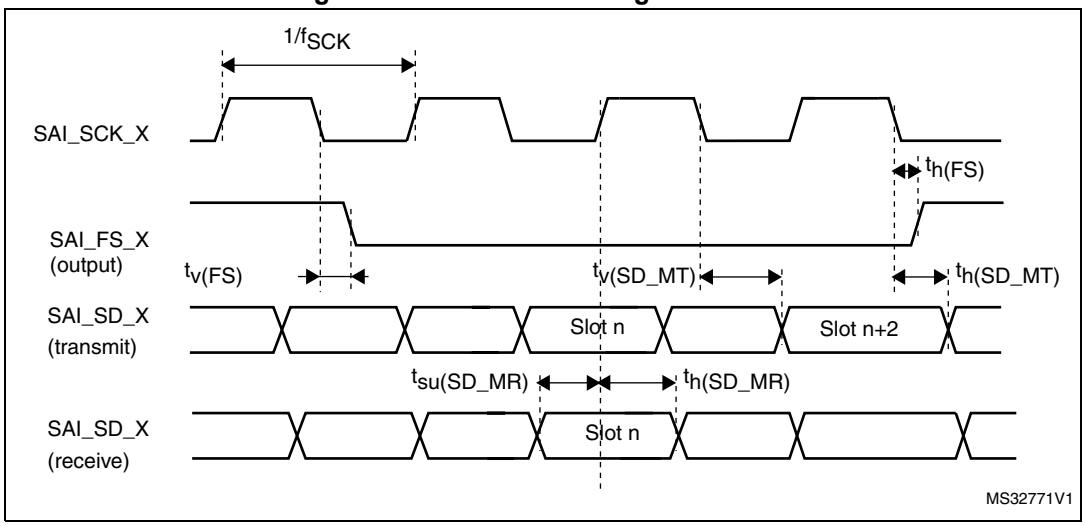
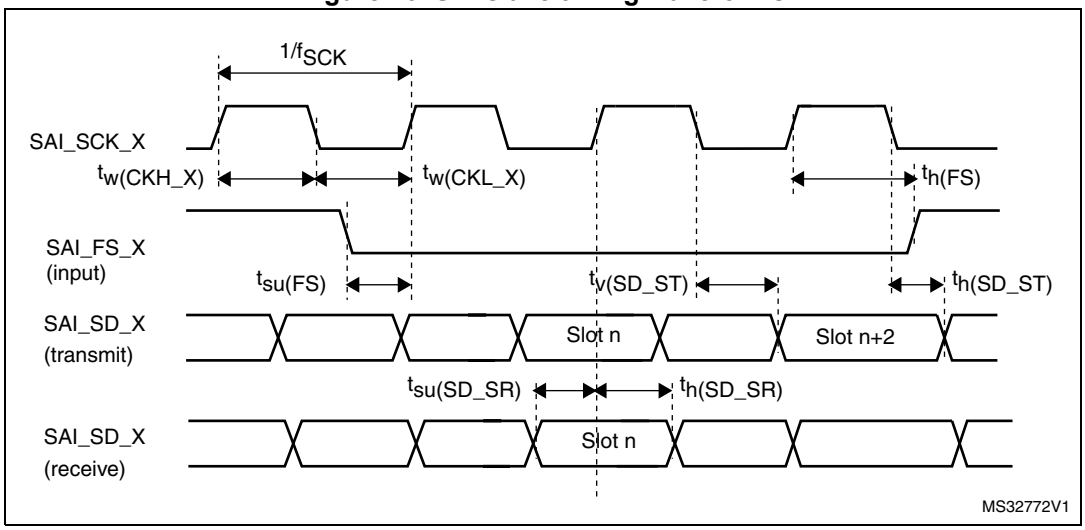


Figure 46. SAI slave timing waveforms



6.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 75* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 17*.

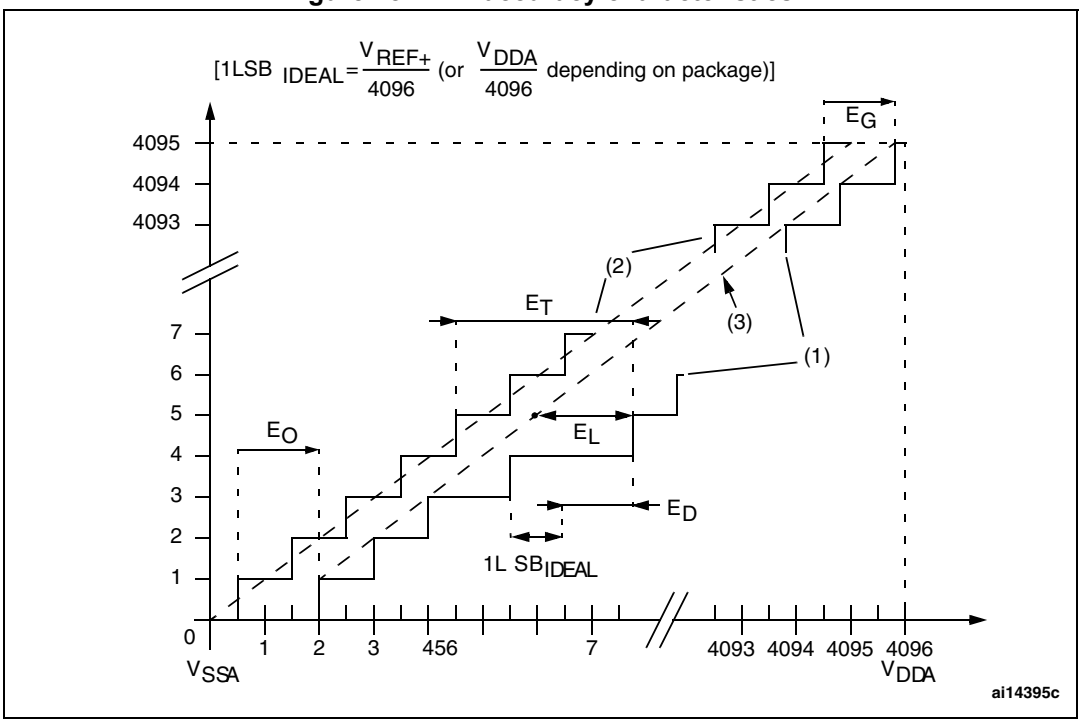
Table 75. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	V_{DDA} –V_{REF+} < 1.2 V	1.7(1)	-	3.6	V
V_{REF+}	Positive reference voltage		1.7(1)	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	-	0	-	
f_{ADC}	ADC clock frequency	V_{DDA} = 1.7(1) to 2.4 V	0.6	15	18	MHz
		V_{DDA} = 2.4 to 3.6 V	0.6	30	36	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 30 MHz, 12-bit resolution	-	-	1764	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* for details	-	-	50	kΩ
R_{ADC}(2)(4)	Sampling switch resistance	-	-	-	6	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	4	7	pF
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
		-	-	-	3(5)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
		-	-	-	2(5)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
		-	3	-	480	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	-	2	3	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.50	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
		f_{ADC} = 30 MHz 6-bit resolution	0.30	-	16.20	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.16* does not affect the ADC accuracy.

Figure 48. ADC accuracy characteristics

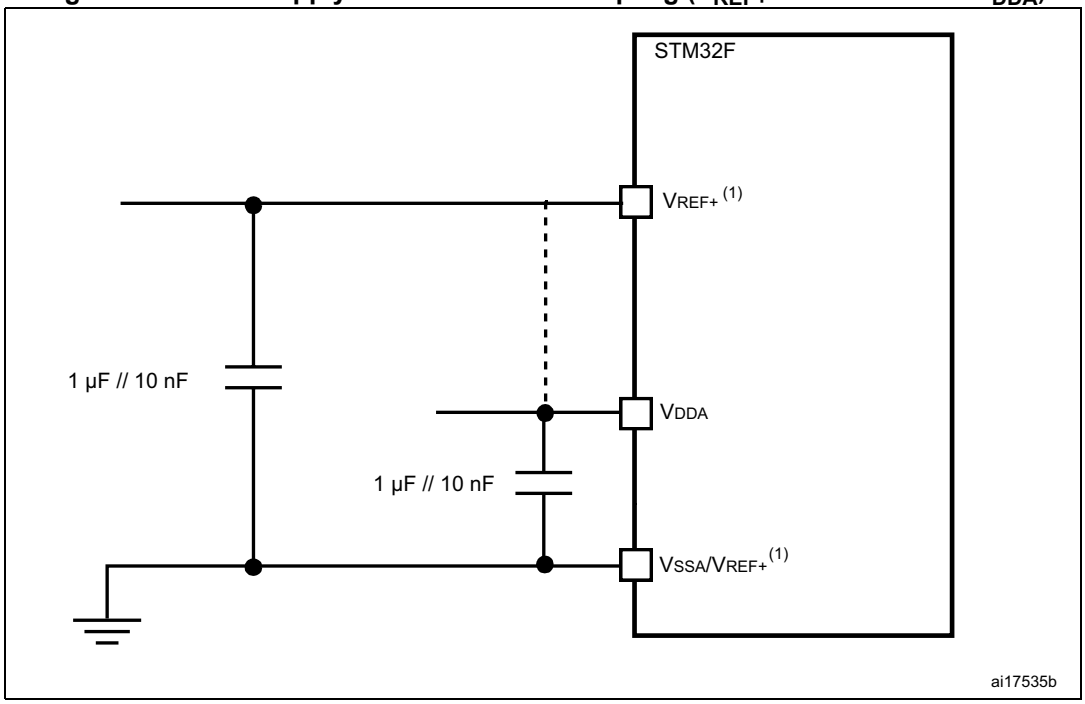


1. See also *Table 77*.
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 50* or *Figure 51*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 50. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA100. V_{REF+} is also available on LQFP100. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

Table 88. Asynchronous non-multiplexed SRAM/PSRAM/NOR - read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$2 * t_{HCLK} - 1$	$2 * t_{HCLK} + 1$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	0	0.5	
$t_{w(NOE)}$	FSMC_NOE low time	$2 * t_{HCLK} - 1$	$2 * t_{HCLK} + 1$	
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0.5	
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$t_{HCLK} - 2$	-	
$t_{su(Data\_NOE)}$	Data to FSMC_NOEx high setup time	$t_{HCLK} - 2$	-	
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	0	
$t_{w(NADV)}$	FSMC_NADV low time	-	$t_{HCLK} + 1$	

1. C_L = 30 pF.
2. Based on characterization.

Table 89. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$7 * t_{HCLK} + 1$	$7 * t_{HCLK} + 1$	ns
$t_{w(NOE)}$	FSMC_NWE low time	$5 * t_{HCLK} - 1$	$5 * t_{HCLK} + 1$	
$t_{w(NWAIT)}$	FSMC_NWAIT low time	$t_{HCLK} - 0.5$	-	
$t_{su(NWAIT\_NE)}$	FSMC_NWAIT valid before FSMC_NEx high	$5 * t_{HCLK} + 1.5$	-	
$t_{h(NE\_NWAIT)}$	FSMC_NEx hold time after FSMC_NWAIT invalid	$4 * t_{HCLK} + 1$	-	

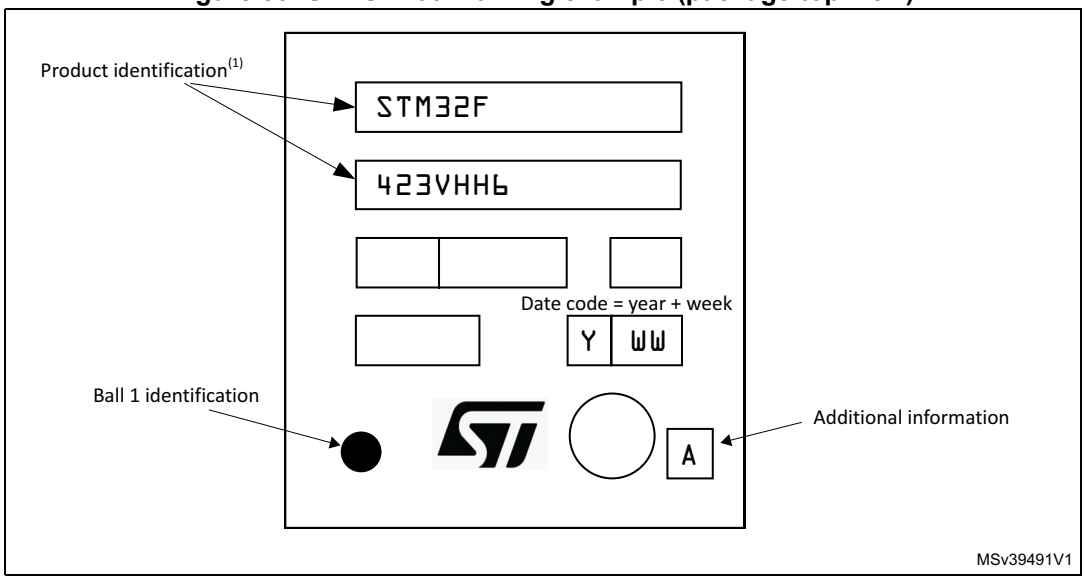
1. C_L = 30 pF.
2. Based on characterization.

Device marking for UFBGA100

The following figure gives an example of topside marking and ball 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 80. UFBGA100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.