Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA
Supplier Device Package	144-UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f423zhj6

Table 10. STM32F423xH pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	B8	-	H3	E5	143	PDR_ON	I	FT	-	-	-
48	64	A9	100	C4	F5	144	VDD	S	-	-	-	-

1. Function availability depends on the chosen device.
2. NC (Not Connected) pins are not bonded. They must be configured by software to output push-pull and forced to 0 in the output data register to avoid extra power consumption in low power mode.
3. Compatibility issue on alternate function pin PE4 SAI1_SD_A and PE6 SAI1_FS_A: Pins have been swapped versus other MCUs supporting those alternate SAI functions on those pins
4. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
5. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F423xHreference manual.
6. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
7. Incompatibility issue on alternate function with other MCUs supporting UART4: UART4_TX wrongly mapped to PD10 instead of PC10

Table 11. FSMC pin definition

Pins	FSMC		64 pins	81 pins	100 pins	144 pins
	LCD/NOR/ PSRAM/SRAM	NOR/PSRAM Mux				
PE2	A23	A23	-	-	Yes	Yes
PE3	A19	A19	-	-	Yes	Yes
PE4	A20	A20	-	-	Yes	Yes
PE5	A21	A21	-	-	Yes	Yes
PE6	A22	A22	-	-	Yes	Yes
PF0	A0	-	-	-	-	Yes
PF1	A1	-	-	-	-	Yes
PF2	A2	-	-	-	-	Yes
PF3	A3	-	-	-	-	Yes
PF4	A4	-	-	-	-	Yes
PF5	A5	-	-	-	-	Yes
PC2	NWE	NWE	Yes	Yes	Yes	Yes
PC3	A0	-	Yes	Yes	Yes	Yes
PA2	D4	DA4	Yes	Yes	Yes	Yes

3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.

Table 24. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A= 25 °C	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	T_A= 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)	100	33.3	35.32(3)	35.65	37.65	41.26(3)	mA
			84	26.8	28.45(3)	28.97	30.82	34.39(3)	
			64	18.6	19.74(3)	20.35	22.11	25.35(3)	
			50	14.6	15.57	16.41	18.21	21.46	
			25	7.8	8.37	9.64	11.32	14.68	
			20	6.7	7.25	8.40	10.25	13.45	
		HSI, PLL OFF(4), all peripherals enabled(2)	16	4.6	4.96	6.39	8.20	11.54	
			1	0.8	0.86	2.51	4.34	7.65	
		External clock, PLL ON, all peripherals disabled(2)	100	15.7	16.74(3)	17.62	19.50	23.16(3)	
			84	12.7	13.57(3)	14.60	16.38	19.98(3)	
			64	9.0	9.62(3)	10.60	12.37	15.58(3)	
			50	7.1	7.69	8.79	10.63	13.79	
			25	4.0	4.52	5.68	7.44	10.68	
			20	3.4	4.03	5.23	6.90	10.27	
		HSI, PLL OFF, all peripherals disabled(2)	16	2.3	2.44	4.00	5.81	9.13	
			1	0.6	0.70	2.35	4.18	7.49	

1. Guaranteed by characterization results.
2. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.
3. Tested in production
4. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered

Table 25. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory- V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)(3)	100	30.2	32.03	32.71	34.69	38.46	mA
			84	24.3	25.77	26.58	28.47	32.16	
			64	16.8	17.80	18.66	20.53	23.85	
			50	13.2	14.05	15.12	16.85	20.27	
			25	7.1	7.62	8.92	10.81	14.11	
			20	6.1	6.69	7.95	9.72	13.09	
		HSI, PLL OFF, all peripherals enabled(2)	16	4.4	4.99	6.28	8.18	11.45	
			1	0.9	1.50	2.88	4.58	8.00	
		External clock, PLL ON(4) all peripherals disabled(2)	100	12.6	13.46	14.75	16.68	20.54	
			84	10.2	10.90	12.25	14.10	17.84	
			64	7.2	7.70	8.95	10.81	14.14	
			50	5.7	6.26	7.56	9.26	12.72	
			25	3.2	3.77	5.11	6.82	10.26	
			20	2.9	3.41	4.79	6.49	9.92	
		HSI, PLL OFF, all peripherals disabled(2)	16	2.1	2.63	3.91	5.80	9.06	
			1	0.8	1.34	2.72	4.42	7.86	

1. Guaranteed by characterization results..
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.
4. Refer to *Table 47* and RM0383 for the possible PLL VCO setting

Table 28. Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)(3)	100	36.1	38.48	39.08	40.91	44.59	mA
			84	30.6	32.60	33.14	35.10	38.56	
			64	23.9	25.67	26.27	27.94	31.19	
			50	18.9	20.32	21.04	22.85	26.10	
			25	10.8	11.63	12.75	14.56	17.87	
			20	9.2	9.84	11.06	12.98	16.23	
		HSI, PLL OFF, all peripherals enabled(2)(3)	16	7.1	7.69	9.02	10.87	14.25	
			1	1.2	1.84	3.10	4.84	8.20	
		External clock, PLL ON(3) all peripherals disabled	100	18.6	20.33	21.23	23.15	26.71	
			84	16.5	18.09	19.01	20.81	24.29	
			64	14.3	15.76	16.67	18.28	21.50	
			50	11.5	12.57	13.53	15.33	18.49	
			25	7.0	7.67	8.90	10.76	14.05	
			20	6.0	6.68	7.87	9.65	12.96	
		HSI, PLL OFF, all peripherals disabled(3)	16	4.8	5.33	6.66	8.49	11.86	
			1	1.0	1.62	2.95	4.66	8.06	

1. Guaranteed by characterization results.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.

Table 29. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)	100	42.3	45.08	45.76	47.88	51.71	mA
			84	34.6	36.87	37.58	39.64	43.32	
			64	25.5	27.18	27.93	29.90	33.23	
			50	20.2	21.55	22.50	24.34	27.73	
			25	10.9	11.61	12.87	14.72	18.08	
			20	9.3	9.86	11.20	13.13	16.41	
		HSI, PLL OFF, all peripherals enabled	16	6.9	7.37	8.81	10.72	14.04	
			1	1.2	1.83	3.09	4.83	8.19	
		External clock, PLL ON(2) all peripherals disabled	100	24.7	26.76	27.84	29.93	33.66	
			84	20.5	22.18	23.25	25.33	28.98	
			64	15.9	17.13	18.23	20.18	23.46	
			50	12.7	13.68	14.95	16.71	20.13	
			25	7.1	7.57	9.01	10.88	14.25	
			20	6.1	6.61	7.98	9.80	13.11	
		HSI, PLL OFF, all peripherals disabled	16	4.5	5.00	6.44	8.33	11.63	
			1	1.0	1.61	2.94	4.65	8.06	

1. Guaranteed by characterization results.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 30. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)	100	42.9	45.86	45.76	47.88	51.71	mA
			84	35.4	37.90	38.16	40.01	43.26	
			64	26.2	28.19	28.74	30.37	33.54	
			50	20.7	22.32	22.50	24.34	27.73	
			25	11.1	11.87	12.87	14.72	18.08	
			20	9.4	10.05	11.26	13.16	16.46	
		HSI, PLL OFF, all peripherals enabled	16	7.1	7.72	9.06	10.90	14.29	
			1	1.2	1.84	3.10	4.84	8.20	
		External clock, PLL ON(2) all peripherals disabled	100	25.4	27.83	27.84	29.93	33.66	
			84	21.4	23.44	24.10	25.77	29.04	
			64	16.6	18.31	19.17	20.72	23.86	
			50	13.2	15.10	14.95	16.71	20.13	
			25	7.2	7.90	9.01	10.88	14.25	
			20	6.2	6.83	8.05	9.88	13.15	
		HSI, PLL OFF, all peripherals disabled	16	4.8	5.37	6.70	8.52	11.89	
			1	1.0	1.62	2.96	4.67	8.07	

1. Guaranteed by characterization results.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 56. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD STM5.3.1, UFBGA144, UFBGA100, LQFP144, LQFP100, WLCSP81, LQFP64	3	250	
		T_A = +25 °C conforming to ANSI/ESD STM5.3.1, UFQFPN48	4	500	

1. Guaranteed by characterization results.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 57. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +125 °C conforming to JESD78A	II level A

6.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in *Table 58*.

6.3.19 Communications interfaces

I^2C interface characteristics

The I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I^2C characteristics are described in *Table 64*. Refer also to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

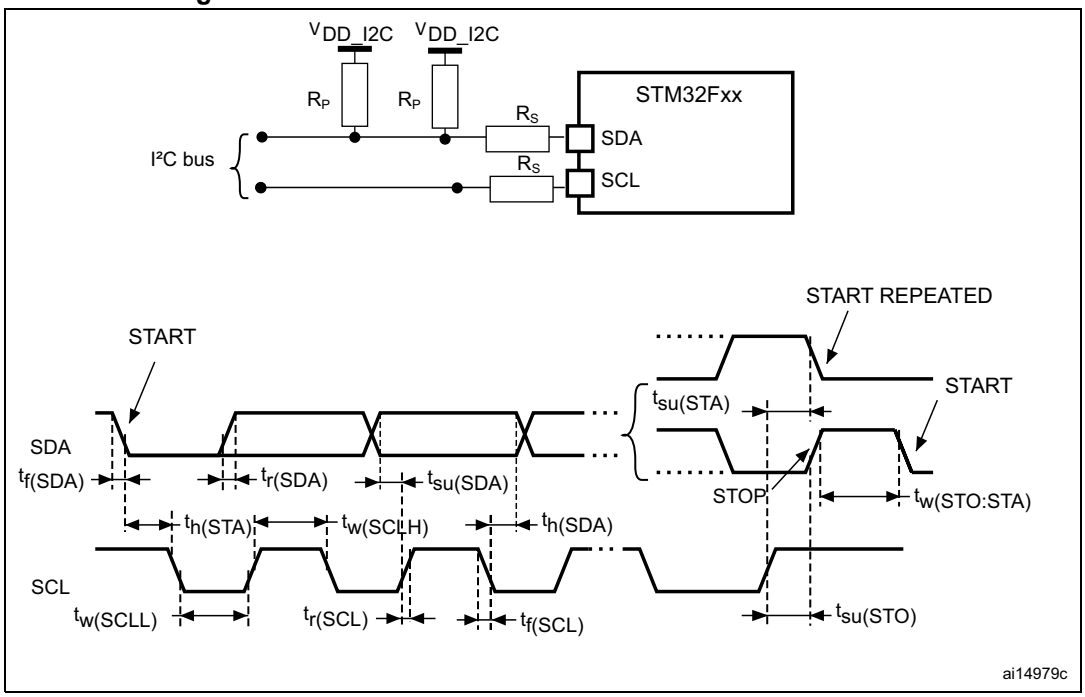
The I^2C bus interface supports standard mode (up to 100 kHz) and fast mode (up to 400 kHz). The I^2C bus frequency can be increased up to 1 MHz. For more details about the complete solution, contact your local ST sales representative.

Table 64. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)(2)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.70	-	1.30	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.60	-	
$t_{su(SDA)}$	SDA setup time	0.25	-	0.10	-	
$t_{h(SDA)}$	SDA data hold time	0	-	0	-	
$t_{v(SDA,ACK)}$	SDA data hold time	-	3.45(3)	-	0.90(4)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	0.100	-	0.30	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	0.30	-	0.30	
$t_{h(STA)}$	Start condition hold time	4	-	0.6	-	
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4	-	0.60	-	
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.70	-	1.3	-	
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard fast mode	-	-	0.05	0.10(5)	
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve fast mode I^2C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I^2C fast mode clock.
3. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
4. The maximum data hold time has only to be met if the interface does not stretch the low period of SCL signal.
5. The minimum width of the spikes filtered by the analog filter is above t_{SP} (max)

Figure 38. I²C bus AC waveforms and measurement circuit



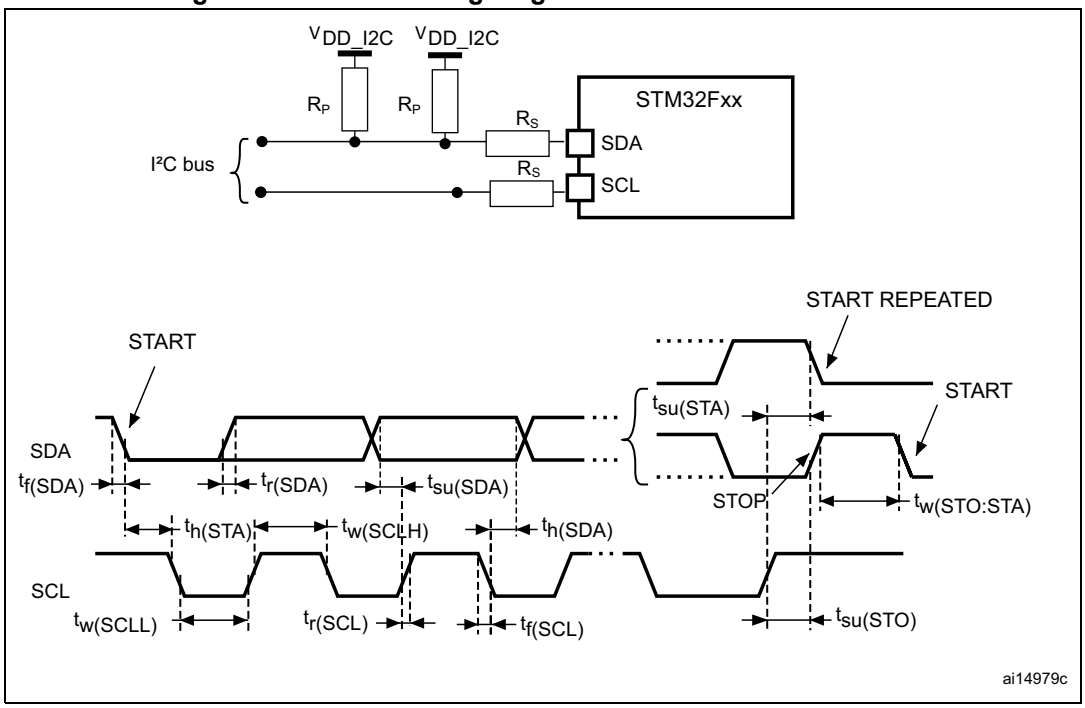
1. R_S = series protection resistor.
2. R_P = external pull-up resistor.
3. V_{DD_I2C} is the I2C bus power supply.

Table 65. SCL frequency (f_{PCLK1}= 50 MHz, V_{DD} = V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x8019
300	0x8021
200	0x8032
100	0x0096
50	0x012C
20	0x02EE

1. R_P = External pull-up resistance, f_{SCL} = I²C speed
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

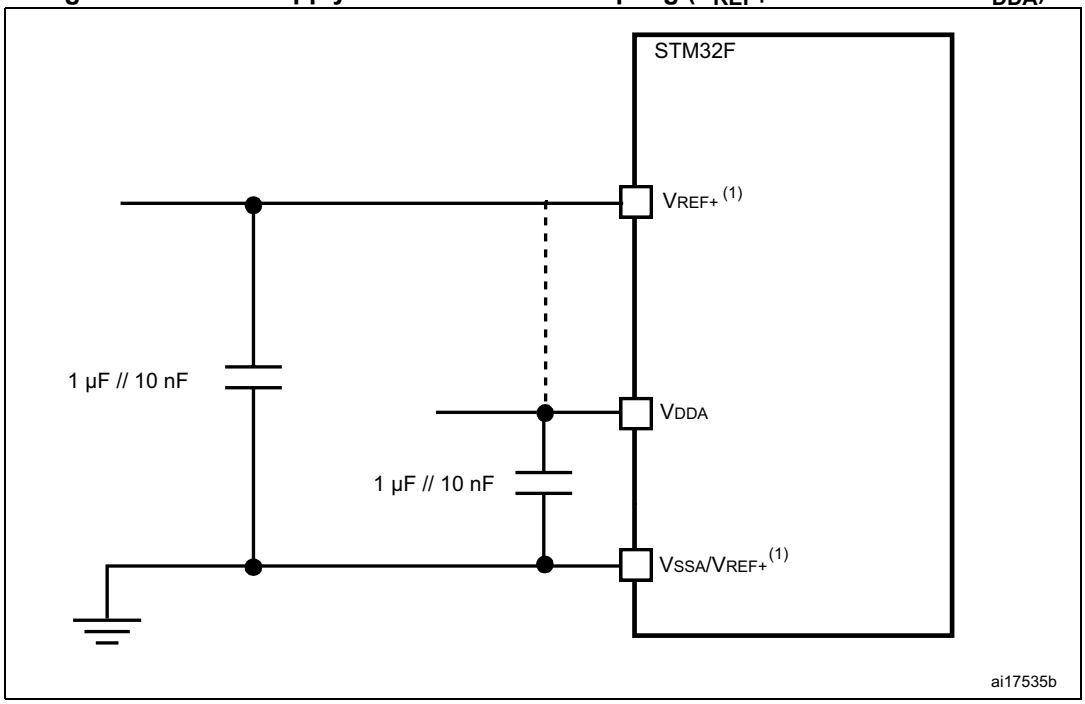
Figure 39. FMPI^{2}C timing diagram and measurement circuit



General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 50* or *Figure 51*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 50. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA100. V_{REF+} is also available on LQFP100. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

6.3.22 V_{BAT} monitoring characteristics

Table 83. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat}(2)(2)	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.23 Embedded reference voltage

The parameters given in *Table 84* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 84. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +125 °C	1.18	1.21	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	10	-	-	µs
V_{RERINT_s}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3V ± 10mV	-	3	5	mV
T_{Coeff}(2)	Temperature coefficient	-	-	30	50	ppm/°C
t_{START}(2)	Startup time	-	-	6	10	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design

Table 85. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C V_{DDA} = 3.3 V	0x1FFF 7A2A - 0x1FFF 7A2B

6.3.27 SD/SDIO MMC/eMMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in *Table 100* for the SDIO are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output characteristics.

Figure 61. SDIO high-speed mode

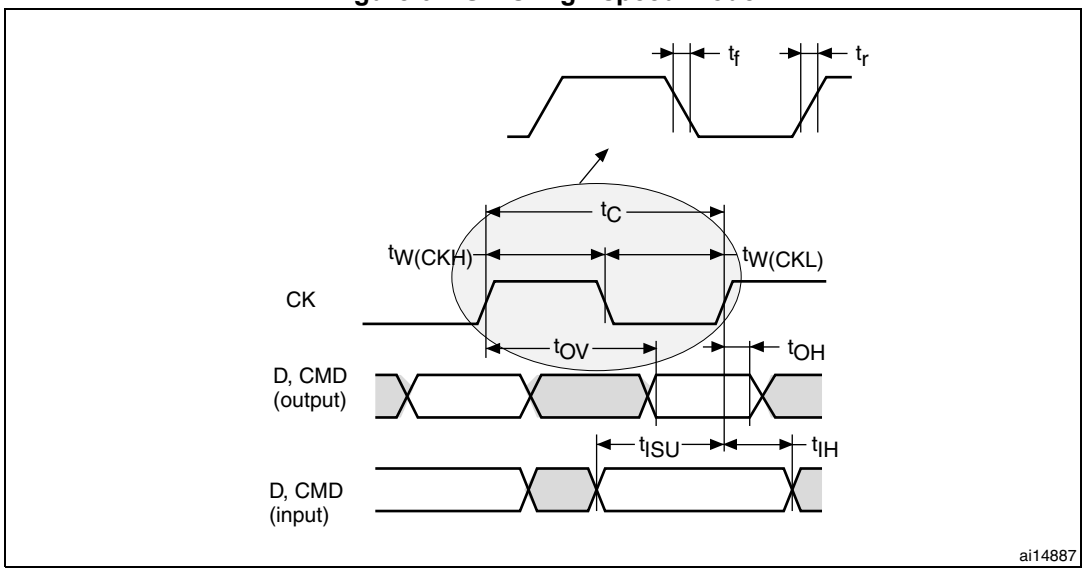
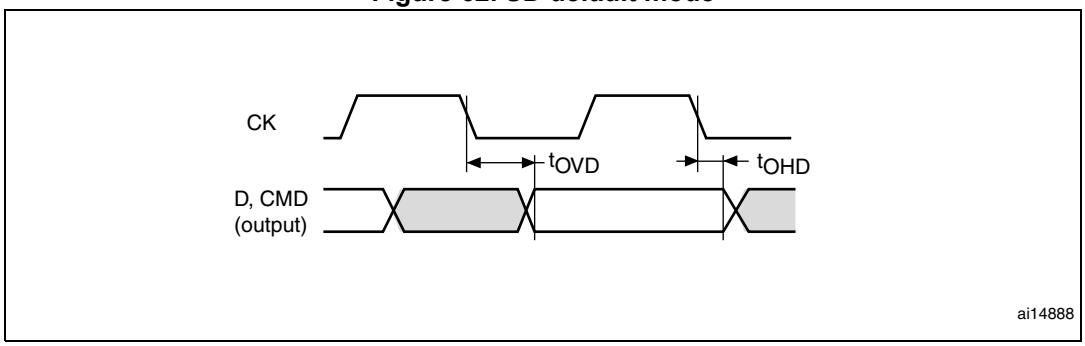


Figure 62. SD default mode

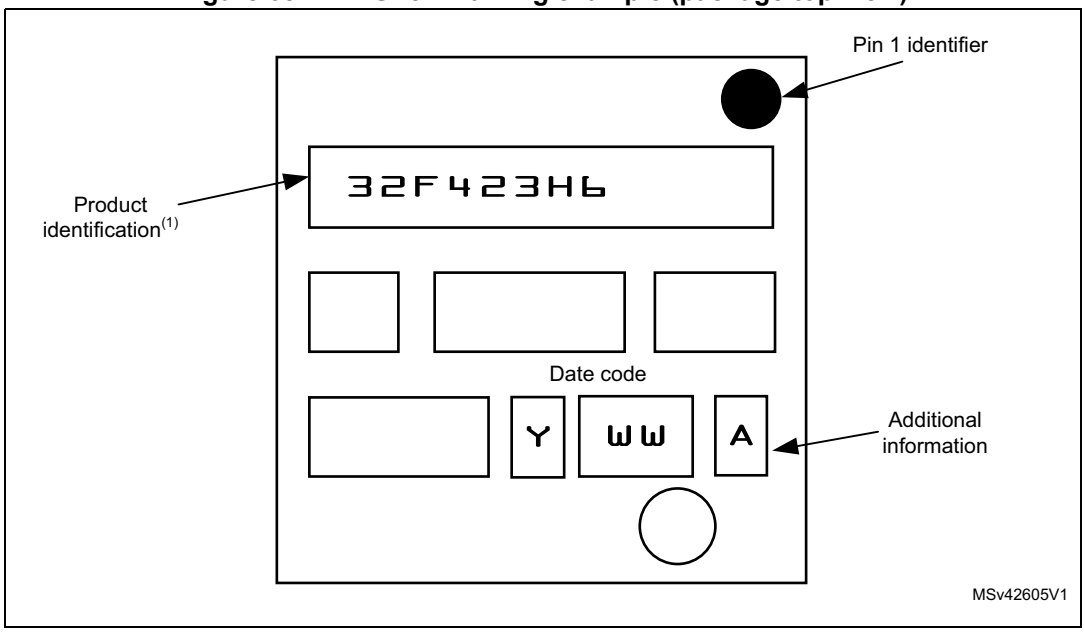


Device marking for WLCSP81

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

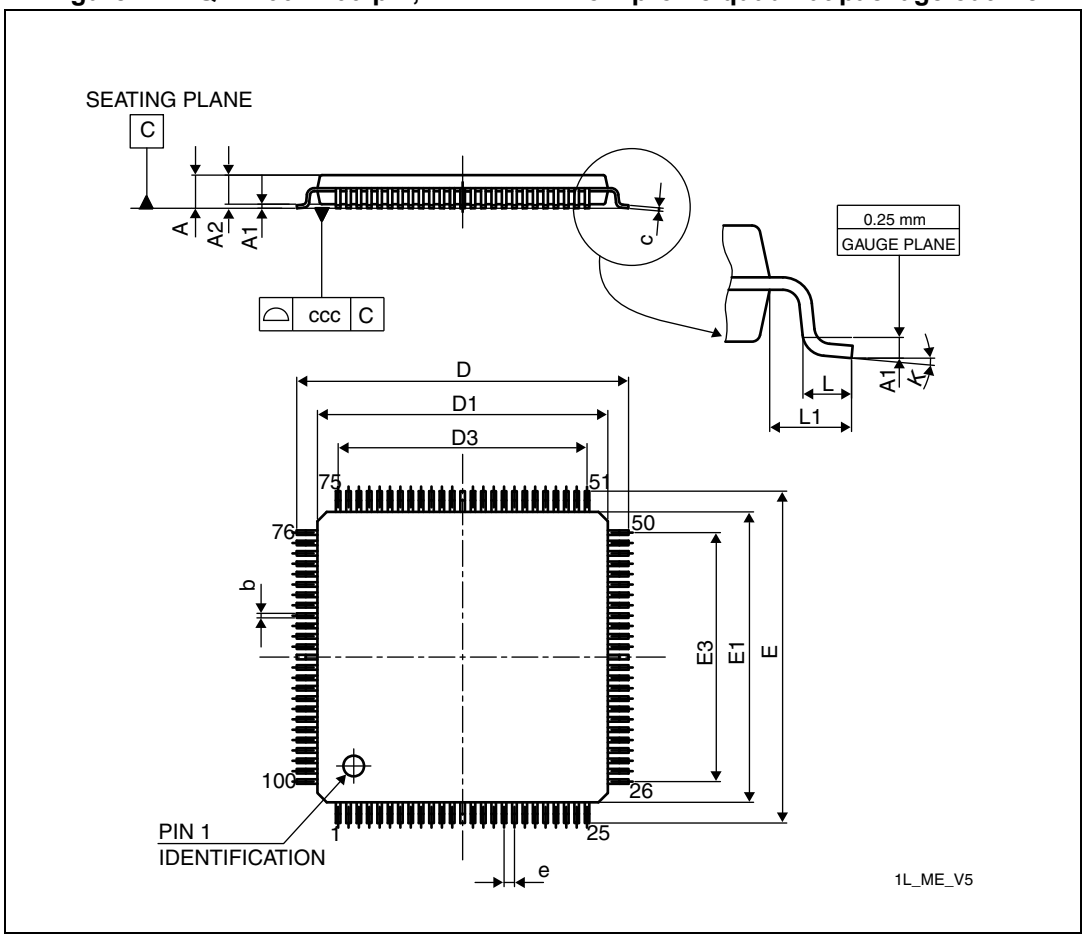
Figure 65. WLCSP81 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.4 LQFP100 package information

Figure 72. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale. Dimensions are in millimeters.

Table 107. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

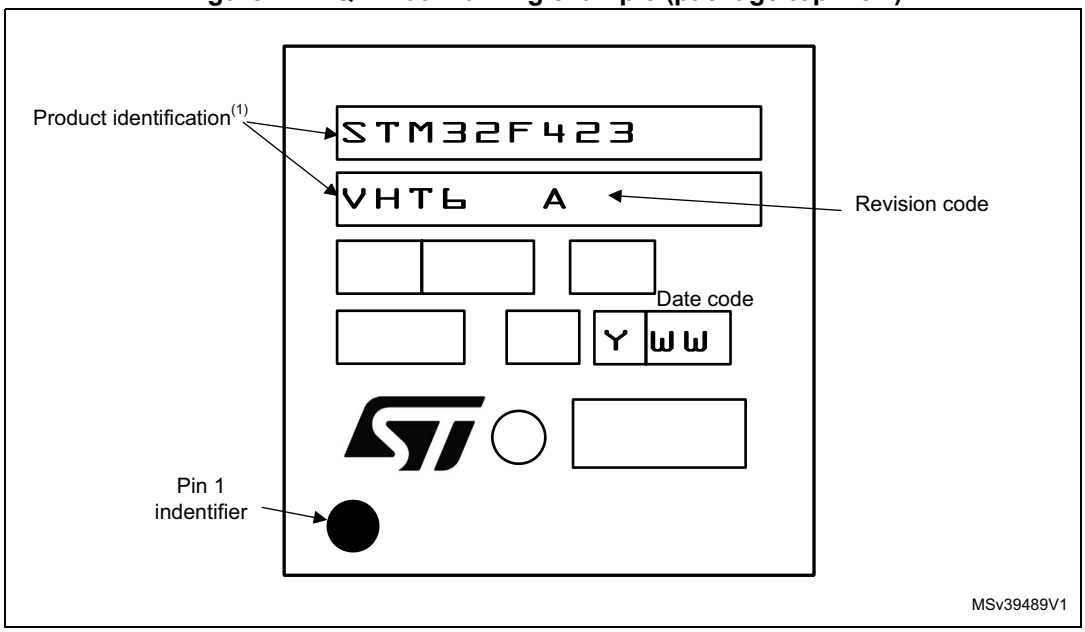
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

Device marking for LQFP100

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 74. LQFP100 marking example (package top view)



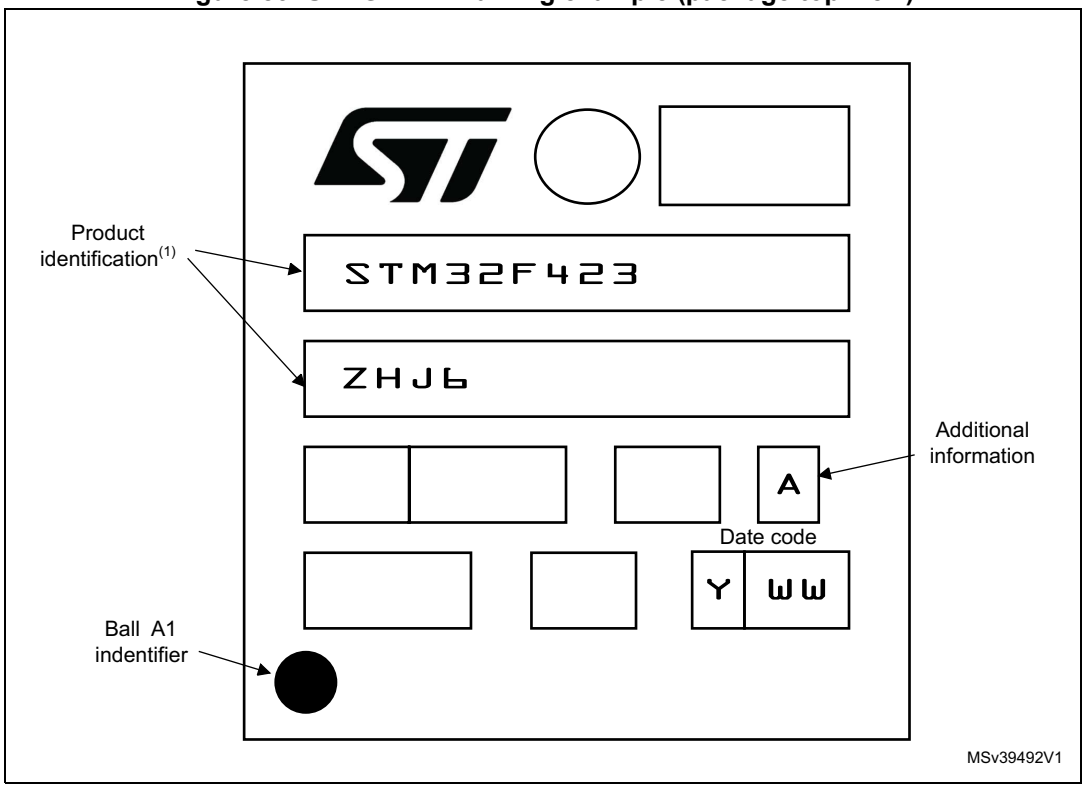
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device marking for UFBGA144

The following figure gives an example of topside marking and ball A1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 83. UFBGA144 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Revision history

Table 115. Document revision history

Date	Revision	Changes
02-Sep-2016	1	Initial release.
24-Oct-2016	2	Updated *Figure 65: WLCSP81 marking example (package top view)*
13-Dec-2016	3	Updated: – *Table 55: EMI characteristics for LQFP144* – *Table 56: ESD absolute maximum ratings* – *Table 70: QSPI dynamic characteristics in SDR mode* – *Table 111: UFBGA144 - 144-ball, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data* – *Figure 81: UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package outline*
12-Jan-2017	4	Added: – *Table 1: Device summary*
07-Mar-2017	5	Updated: – *Table 2: STM32F423xH features and peripheral counts* – *Table 12: STM32F423xH alternate functions* Added: – *Table 11: FSMC pin definition*