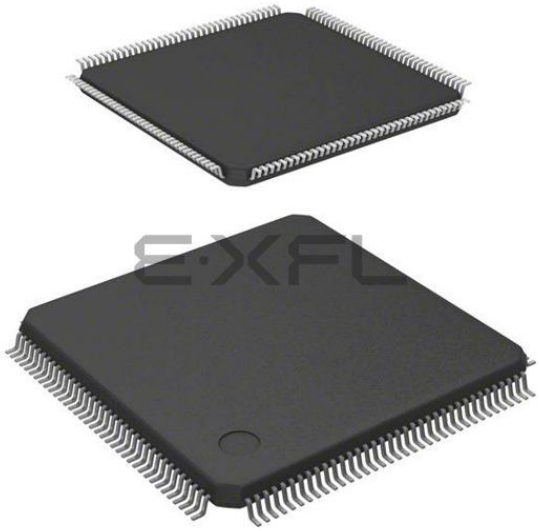

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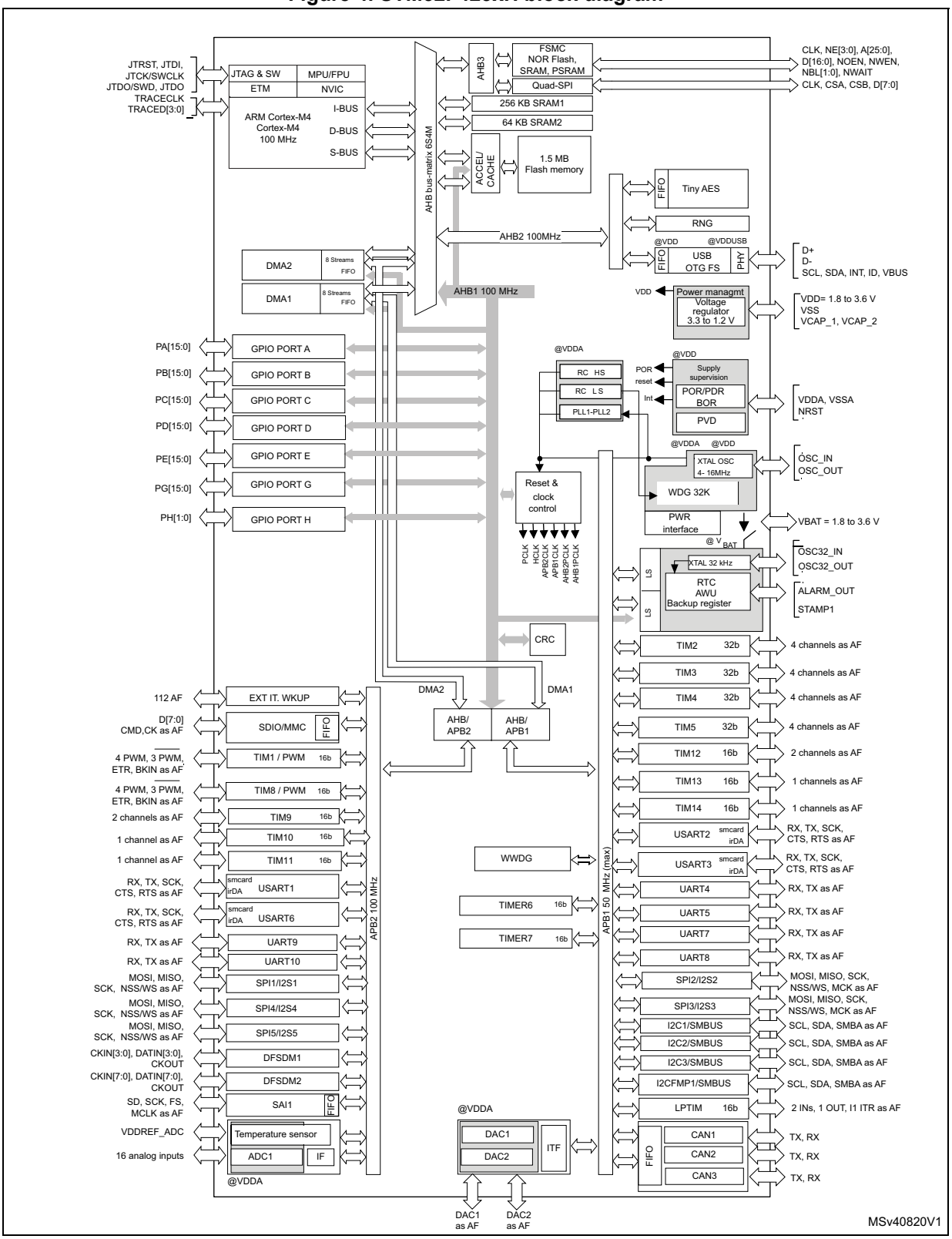
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f423zht3

Figure 4. STM32F423xH block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 100 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 50 MHz.

Table 5. Timer feature comparison (continued)

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complemen-tary output	Max. interface clock (MHz)	Max. timer clock (MHz)
Basic timers	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	50	100
Low-power timer	LPTIM1	16-bit	Up	Between 1 and 128	No	2	No	50	100

3.22.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1/8) can be seen as three-phase PWM generator multiplexed on 4 independent channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as a 16-bit PWM generator, they have full modulation capability (0-100%).

The advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

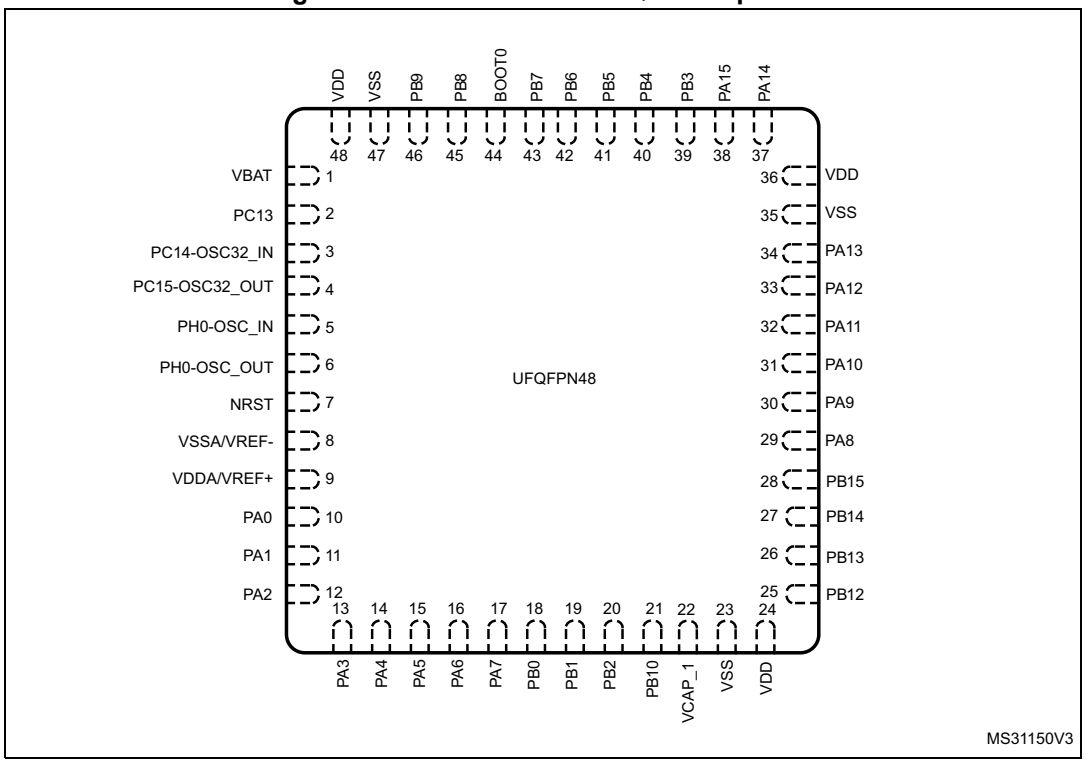
3.22.2 General-purpose timers (TIMx)

There are elven synchronizable general-purpose timers embedded in the STM32F423xH (see *Table 5* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The STM32F423xH devices include 4 full-featured general-purpose timers: TIM2. TIM3, TIM4 and TIM5. TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler while TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter plus a 16-bit prescaler. They all features four

Figure 12. STM32F423xH UFQFPN48 pinout



1. The above figure shows the package top view.

Table 10. STM32F423xH pin definition

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	NC	1	B2	A3	1	PE2	I/O	FT	(2)	TRACECLK, SPI4_SCK/I2S4_CK, SPI5_SCK/I2S5_CK, SAI1_MCLK_A, QUADSPI_BK1_IO2, UART10_RX, FSMC_A23, EVENTOUT	-
-	-	NC	2	A1	A2	2	PE3	I/O	FT	(2)	TRACED0, SAI1_SD_B, UART10_TX, FSMC_A19, EVENTOUT	-
-	-	NC	3	B1	B2	3	PE4	I/O	FT	(2)(3)	TRACED1, SPI4_NSS/I2S4_WS, SPI5_NSS/I2S5_WS, SAI1_SD_A, DFSDM1_DATIN3, FSMC_A20, EVENTOUT	-
-	-	NC	4	C2	B3	4	PE5	I/O	FT	(2)	TRACED2, TIM9_CH1, SPI4_MISO, SPI5_MISO, SAI1_SCK_A, DFSDM1_CKIN3, FSMC_A21, EVENTOUT	-
-	-	NC	5	D2	B4	5	PE6	I/O	FT	(2)(3)	TRACED3, TIM9_CH2, SPI4_MOSI/I2S4_SD, SPI5_MOSI/I2S5_SD, SAI1_FS_A, FSMC_A22, EVENTOUT	-
1	1	B9	6	E2	C2	6	VBAT	S	-	-	-	VBAT
2	2	C8	7	C1	A1	7	PC13-ANTI_TAMP	I/O	FT	(4)(5)	EVENTOUT	TAMP_1
3	3	C9	8	D1	B1	8	PC14-OSC32_IN	I/O	FT	(4)(5)(6)	EVENTOUT	OSC32_IN
4	4	D9	9	E1	C1	9	PC15-OSC32_OUT	I/O	FT	(4)(6)	EVENTOUT	OSC32_OUT
-	-	-	-	-	C3	10	PF0	I/O	FT	-	I2C2_SDA, FSMC_A0, EVENTOUT	-
-	-	-	-	-	C4	11	PF1	I/O	FT	-	I2C2_SCL, FSMC_A1, EVENTOUT	-

Table 10. STM32F423xH pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	39	E1	65	E10	F11	98	PC8	I/O	FT	-	TIM3_CH3, TIM8_CH3, DFSDM2_CKIN3, USART6_CK, QUADSPI_BK1_IO2, SDIO_D0, EVENTOUT	-
-	40	E2	66	D12	E11	99	PC9	I/O	FT	-	MCO_2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S2_CKIN, DFSDM2_DATIN3, QUADSPI_BK1_IO0, SDIO_D1, EVENTOUT	-
29	41	D3	67	D11	E12	100	PA8	I/O	FT	-	MCO_1, TIM1_CH1, I2C3_SCL, DFSDM1_CKOUT, USART1_CK, UART7_RX, USB_FS_SOF, CAN3_RX, SDIO_D1, EVENTOUT	-
30	42	D2	68	D10	D12	101	PA9	I/O	FT	-	TIM1_CH2, DFSDM2_CKIN3, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, USB_FS_VBUS, SDIO_D2, EVENTOUT	-
31	43	D1	69	C12	D11	102	PA10	I/O	FT	-	TIM1_CH3, DFSDM2_DATIN3, SPI2_MOSI/I2S2_SD, SPI5_MOSI/I2S5_SD, USART1_RX, USB_FS_ID, EVENTOUT	-
32	44	C3	70	B12	C12	103	PA11	I/O	FT	-	TIM1_CH4, DFSDM2_CKIN5, SPI2_NSS/I2S2_WS, SPI4_MISO, USART1_CTS, USART6_TX, CAN1_RX, USB_FS_DM, UART4_RX, EVENTOUT	-

Table 10. STM32F423xH pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
33	45	B3	71	A12	B12	104	PA12	I/O	FT	-	TIM1_ETR, DFSDM2_DATIN5, SPI2_MISO, SPI5_MISO, USART1_RTS, USART6_RX, CAN1_TX, USB_FS_DP, UART4_TX, EVENTOUT	-
34	46	C2	72	A11	A12	105	PA13	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
-	-	C1	73	C11	G9	106	VCAP_2	S	-	-	-	-
35	47	B1	74	F11	G10	107	VSS	S	-	-	-	-
-	48	-	75	G11	-	-	VDD	S	-	-	-	-
36	-	A1	-	-	F9	108	VDD	S	-	-	-	-
37	49	B2	76	A10	A11	109	PA14	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
38	50	A3	77	A9	A10	110	PA15	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART1_TX, UART7_TX, SAI1_MCLK_A, CAN3_TX, EVENTOUT	-
-	51	A2	78	B11	B11	111	PC10	I/O	FT	-	DFSDM2_CKIN5, SPI3_SCK/I2S3_CK, USART3_TX, QUADSPI_BK1_IO1, SDIO_D2, EVENTOUT	-
-	52	C4	79	C10	B10	112	PC11	I/O	FT	-	DFSDM2_DATIN5, I2S3ext_SD, SPI3_MISO, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, FSMC_D2/FSMC_DA2, SDIO_D3, EVENTOUT	-
-	53	B4	80	B10	C10	113	PC12	I/O	FT	-	SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, FSMC_D3/FSMC_DA3, SDIO_CK, EVENTOUT	-

Table 12. STM32F423xH alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/2/ LPTIM1	TIM3/4/5	DFSDM2/ TIM8/9/10/11	I2C1/2/3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2	SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3	DFSDM1/ USART3/4/ 5/6/7/8/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI	SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS	UART4/ UART5/ UART9/ UART10 /CAN3	FSMC /SDIO	-	RNG	SYS_AF
Port C	PC0	-	LPTIM1_IN1	-	DFSDM2_CKIN4	-	-	-	SAI1_MCLK_B	-	-	-	-	-	-	-	EVENTOUT
	PC1	-	LPTIM1_OUT	-	DFSDM2_DATIN4	-	-	-	SAI1_SD_B	-	-	-	-	-	-	-	EVENTOUT
	PC2	-	LPTIM1_IN2	-	DFSDM2_DATIN7	-	SPI2_MISO	I2S2ext_SD	SAI1_SCK_B	DFSDM1_CKOUT	-	-	-	FSMC_NWE	-	-	EVENTOUT
	PC3	-	LPTIM1_ETR	-	DFSDM2_CKIN7	-	SPI2_MOSI/ I2S2_SD	-	SAI1_FS_B	-	-	-	-	FSMC_A0	-	-	EVENTOUT
	PC4	-	-	-	DFSDM2_CKIN2	-	I2S1_MCK	-	-	-	-	QUADSPI_BK2_IO2	-	FSMC_NE4	-	-	EVENTOUT
	PC5	-	-	-	DFSDM2_DATIN2	I2CFMP1_SMBA	-	-	USART3_RX	-	-	QUADSPI_BK2_IO3	-	FSMC_NOE	-	-	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	I2CFMP1_SCL	I2S2_MCK	DFSDM1_CKIN3	DFSDM2_DATIN6	USART6_TX	-	FSMC_D1/ FSMC_DA1	-	SDIO_D6	-	-	EVENTOUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	I2CFMP1_SDA	SPI2_SCK/ I2S2_CK	I2S3_MCK	DFSDM2_CKIN6	USART6_RX	-	DFSDM1_DATIN3	-	SDIO_D7	-	-	EVENTOUT
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	DFSDM2_CKIN3	USART6_CK	QUADSPI_BK1_IO2	-	-	SDIO_D0	-	-	EVENTOUT
	PC9	MCO_2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S2_CKIN	-	DFSDM2_DATIN3	-	QUADSPI_BK1_IO0	-	-	SDIO_D1	-	-	EVENTOUT
	PC10	-	-	-	DFSDM2_CKIN5	-	-	SPI3_SCK/ I2S3_CK	USART3_TX	-	QUADSPI_BK1_IO1	-	-	SDIO_D2	-	-	EVENTOUT
	PC11	-	-	-	DFSDM2_DATIN5	-	I2S3ext_SD	SPI3_MISO	USART3_RX	UART4_RX	QUADSPI_BK2_NCS	FSMC_D2/ FSMC_DA2	-	SDIO_D3	-	-	EVENTOUT
	PC12	-	-	-	-	-	-	SPI3_MOSI/ I2S3_SD	USART3_CK	UART5_TX	-	FSMC_D3/ FSMC_DA3	-	SDIO_CK	-	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 32. Typical and maximum current consumption in Sleep mode - V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Sleep mode**	External clock, PLL ON, Flash deep power down, all peripherals enabled(2)	100	21.2	22.64	23.56	25.66	29.30	mA
			84	17.1	18.20	19.27	21.14	24.75	
			64	11.8	12.53	13.59	15.47	18.66	
			50	9.3	9.88	11.06	12.94	16.11	
			25	5.0	5.52	6.83	8.61	11.88	
			20	4.4	4.93	6.16	8.03	11.19	
		HSI, PLL OFF(2), Flash deep power down, all peripherals enabled	16	3.0	3.53	4.91	6.57	9.94	
			1	0.6	1.19	2.55	4.21	7.57	
		External clock, PLL ON(2) all peripherals enabled, Flash ON	100	21.7	23.10	24.09	26.12	29.90	
			84	17.4	18.61	19.72	21.55	25.27	
			64	12.1	12.89	13.98	15.84	19.18	
			50	9.6	10.20	11.43	13.32	16.62	
			25	5.2	5.80	7.19	8.91	12.33	
			20	4.6	5.18	6.47	8.37	11.63	
		HSI, PLL OFF(2), all peripherals enabled, Flash ON	16	3.2	3.79	5.17	6.88	10.32	
			1	0.9	1.43	2.80	4.50	7.92	
		All peripherals disabled, External clock, PLL ON(2), Flash deep power down	100	3.3	3.82	5.34	7.25	10.97	
			84	2.7	3.22	4.70	6.54	10.13	
			64	1.9	2.48	3.70	5.55	8.71	
			50	1.6	2.13	3.35	5.15	8.35	
			25	1.0	1.61	2.90	4.57	7.91	
			20	1.1	1.66	2.93	4.59	7.93	
		All peripherals disabled, HSI, PLL OFF(2), Flash deep power down	16	0.6	1.12	2.49	4.14	7.49	
			1	0.5	1.04	2.40	4.06	7.40	
		All peripherals disabled, External clock, PLL ON(2), Flash ON	100	3.7	4.28	5.76	7.83	11.49	
			84	3.1	3.60	5.11	6.96	10.64	
			64	2.3	2.80	4.09	5.96	9.23	
			50	1.9	2.44	3.70	5.59	8.82	
			25	1.3	1.89	3.18	4.94	8.27	
			20	1.4	1.92	3.20	4.97	8.29	
		All peripherals disabled, HSI, PLL OFF(2), Flash ON	16	0.8	1.38	2.75	4.44	7.87	
			1	0.7	1.25	2.65	4.34	7.77	

1. Guaranteed by characterization results.

Figure 27. High-speed external clock source AC timing diagram

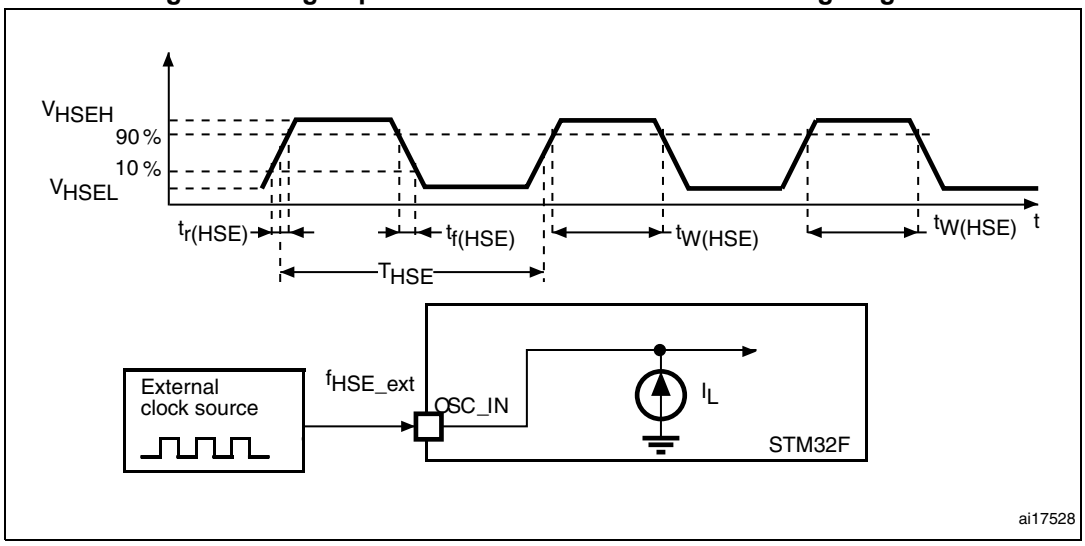
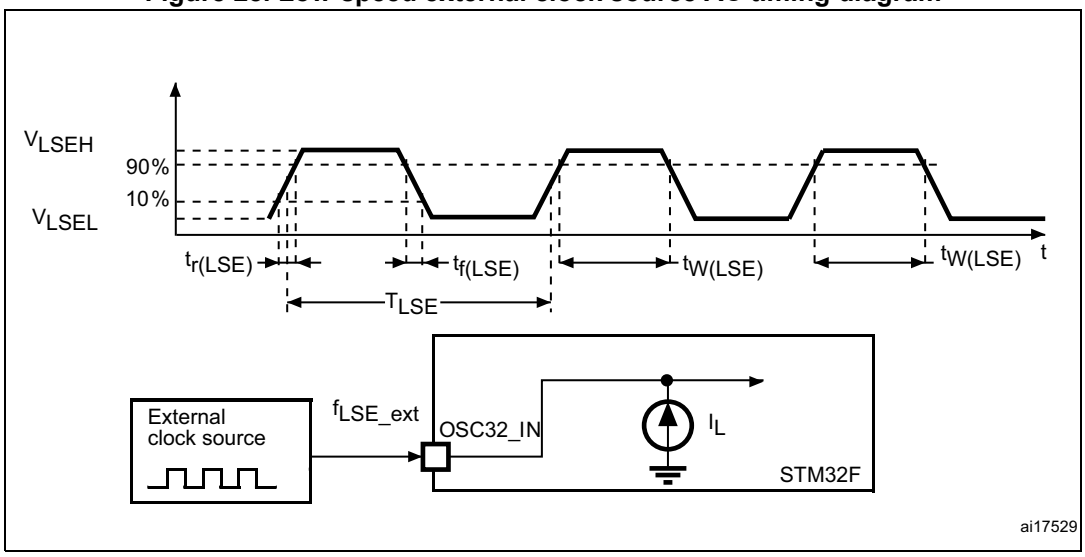


Figure 28. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 43*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

6.3.9 Internal clock source characteristics

The parameters given in *Table 45* and *Table 46* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

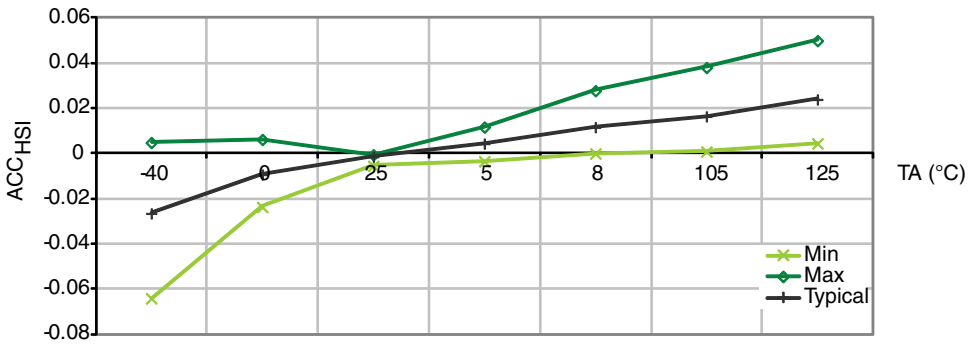
High-speed internal (HSI) RC oscillator

Table 45. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user trimming step(2)	-	-	-	1	%
	Accuracy of the HSI oscillator	T_A = – 40 to 125 °C(3)	–8	-	6.75	%
		T_A = – 40 to 105 °C(3)	–8	-	4.5	%
		T_A = –10 to 85 °C(3)	–4	-	4	%
		T_A = 25 °C(4)	–1	-	1	%
$t_{su(HSI)}$(2)	HSI oscillator startup time	-	-	2.2	4	µs
$I_{DD(HSI)}$(2)	HSI oscillator power consumption	-	-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 125 °C unless otherwise specified.
2. Guaranteed by design
3. Based on characterization
4. Factory calibrated, parts not soldered.

Figure 31. ACC_{HSI} versus temperature



1. Guaranteed by characterization results.

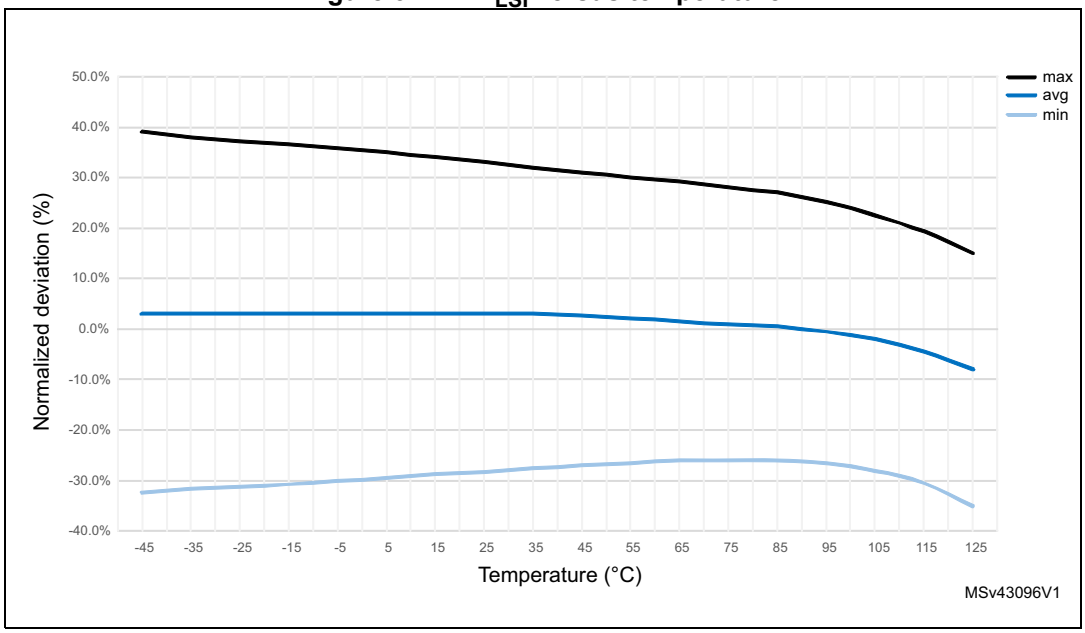
Low-speed internal (LSI) RC oscillator

Table 46. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI} (2)	Frequency	16.1	32.0	47.0	kHz
$t_{su(LSI)}$ (3)	LSI oscillator startup time	-	15.0	40.0	µs
$I_{DD(LSI)}$ (3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 125 °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design.

Figure 32. ACC_{LSI} versus temperature



Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with IEC61967-2 standard which specifies the test board and the pin loading.

Table 55. EMI characteristics for LQFP144

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				8/100 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP144 package, conforming to IEC 61967-2, EEMBC, ART ON, all peripheral clocks enabled, clock dithering disabled.	0.1 to 30 MHz	13	dBµV
			30 to 130 MHz	21	
			130 MHz to 1 GHz	25	
			1 GHz to 2 GHz	19	
			EMI Level	4	-

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

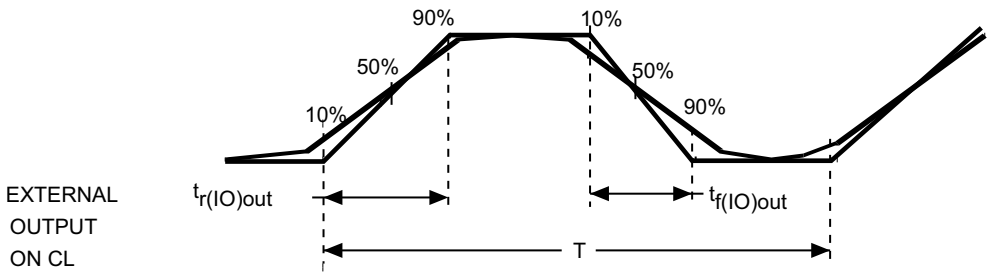
Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 61. I/O AC characteristics(1)(2)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} ≥ 2.70 V	-	-	4	MHz
			C_L = 50 pF, V_{DD}≥ 1.7 V	-	-	2	
			C_L = 10 pF, V_{DD} ≥ 2.70 V	-	-	8	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	4	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.7 V to 3.6 V	-	-	100	ns
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} ≥ 2.70 V	-	-	25	MHz
			C_L = 50 pF, V_{DD} ≥ 1.7 V	-	-	12.5	
			C_L = 10 pF, V_{DD} ≥ 2.70 V	-	-	50	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	20	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} ≥2.7 V	-	-	10	ns
			C_L = 50 pF, V_{DD} ≥ 1.7 V	-	-	20	
			C_L = 10 pF, V_{DD} ≥ 2.70 V	-	-	6	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 40 pF, V_{DD} ≥ 2.70 V	-	-	50(4)	MHz
			C_L = 40 pF, V_{DD} ≥ 1.7 V	-	-	25	
			C_L = 10 pF, V_{DD} ≥ 2.70 V	-	-	100(4)	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	50(4)	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, V_{DD}≥ 2.70 V	-	-	6	ns
			C_L = 40 pF, V_{DD}≥ 1.7 V	-	-	10	
			C_L = 10 pF, V_{DD}≥ 2.70 V	-	-	4	
			C_L = 10 pF, V_{DD}≥ 1.7 V	-	-	6	
11	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, V_{DD} ≥ 2.70 V	-	-	100(4)	MHz
			C_L = 30 pF, V_{DD} ≥ 1.7 V	-	-	50(4)	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 30 pF, V_{DD} ≥ 2.70 V	-	-	4	ns
			C_L = 30 pF, V_{DD} ≥ 1.7 V	-	-	6	
			C_L = 10 pF, V_{DD}≥ 2.70 V	-	-	2.5	
			C_L = 10 pF, V_{DD}≥ 1.7 V	-	-	4	
FM+	Fmax	Maximum frequency	C_L = 50 pF, 1.6 ≤ V_{DD} ≤ 3.6 V	-	-	1	MHz
	Tf	Output high to low level fall time		-	-	5	ns
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	-	ns

1. Guaranteed by characterization results.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in *Figure 36*.
4. For maximum frequencies above 50 MHz and V_{DD} > 2.4 V, the compensation cell should be used.

Figure 36. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

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6.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 59*).

Unless otherwise specified, the parameters given in *Table 62* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*. Refer to *Table 59: I/O static characteristics* for the values of VIH and VIL for NRST pin.

Table 62. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	V_{DD} > 2.7 V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	µs

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

FMPI^{2}C characteristics

The following table presents FMPI^{2}C characteristics.

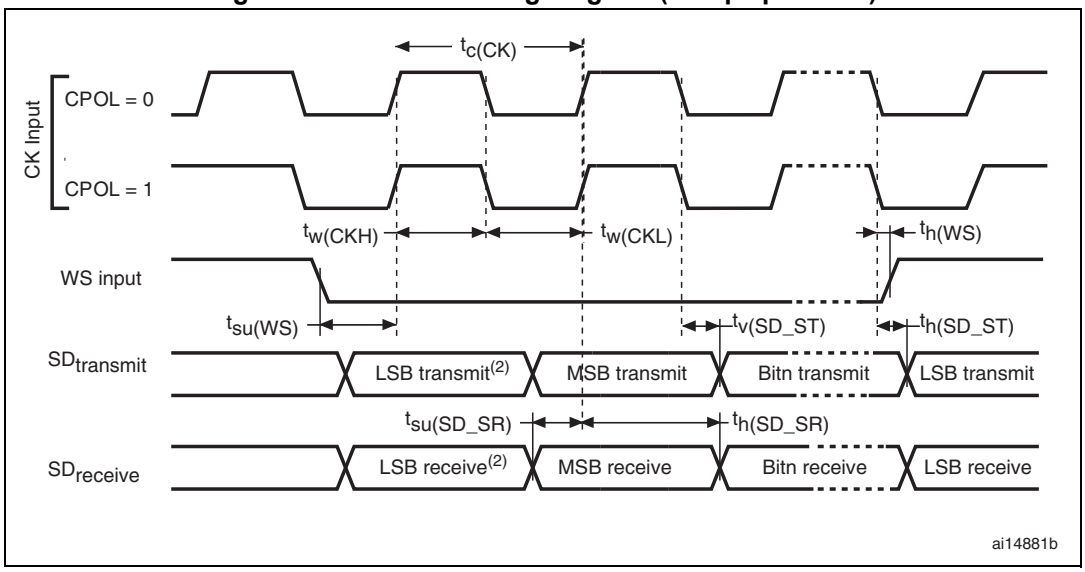
Refer also to *Section 6.3.16: I/O port characteristics* for more details on the input/output function characteristics (SDA and SCL).

Table 66. FMPI^{2}C characteristics(1)

	Parameter	Standard mode		Fast mode		Fast+ mode		Unit
		Min	Max	Min	Max	Min	Max	
$f_{FMPI2CC}$	$F_{MPI2CCLK}$ frequency	2	-	8	-	18	-	µs
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.5	-	
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	
$t_{su(SDA)}$	SDA setup time	0.25	-	0.10	-	0.05	-	
$t_{H(SDA)}$	SDA data hold time	0	-	0	-	0	-	
$t_{v(SDA,ACK)}$	Data, ACK valid time	-	3.45	-	0.9	-	0.45	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1.0	-	0.30	-	0.12	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	0.30	-	0.30	-0	0.12	
$t_{h(STA)}$	Start condition hold time	4	-	0.6	-	0.26	-	
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	0.26	-	
$t_{su(STO)}$	Stop condition setup time	4	-	0.6	-	0.26	-	
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	0.5	-	
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode	-	-	0.05	0.1	0.05	0.1	
C_b	Capacitive load for each bus Line	-	400	-	400	-	550(2)	pF

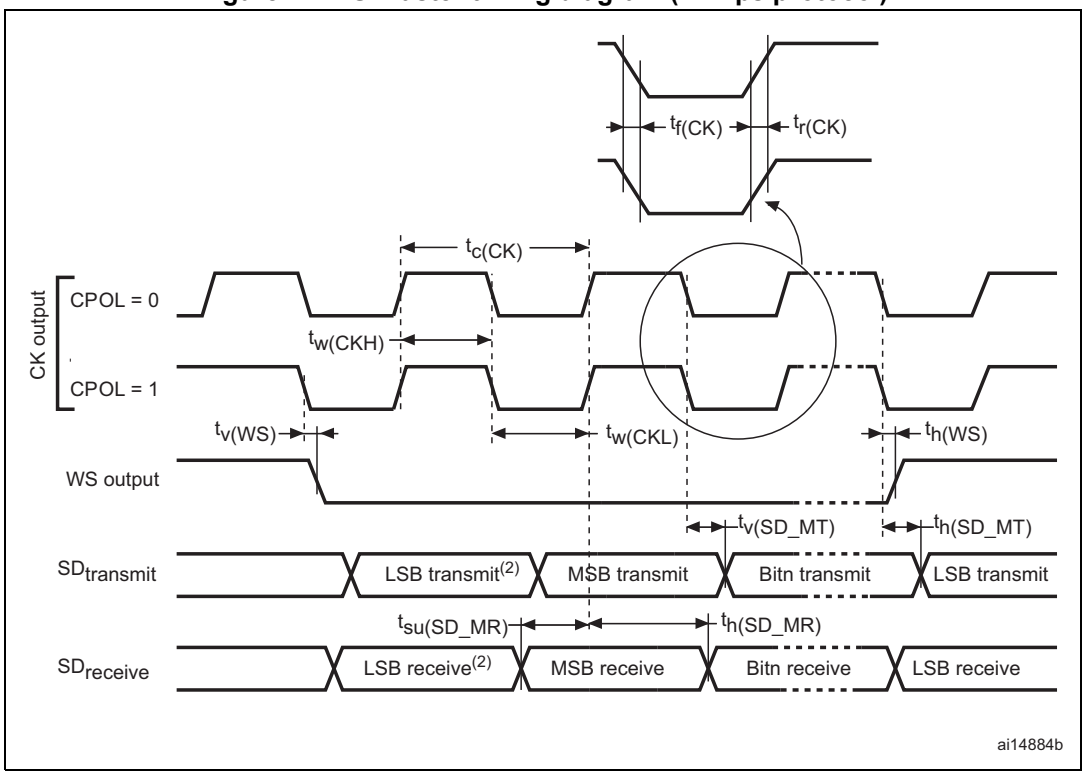
1. Based on characterization results.
2. Can be limited. Maximum supported value can be retrieved by referring to the following formulas:
   $t_{r(SDA/SCL)} = 0.8473 \times R_p \times C_{load}$
   $R_{p(min)} = (V_{DD} - V_{OL(max)}) / I_{OL(max)}$

Figure 43. I²S slave timing diagram (Philips protocol)



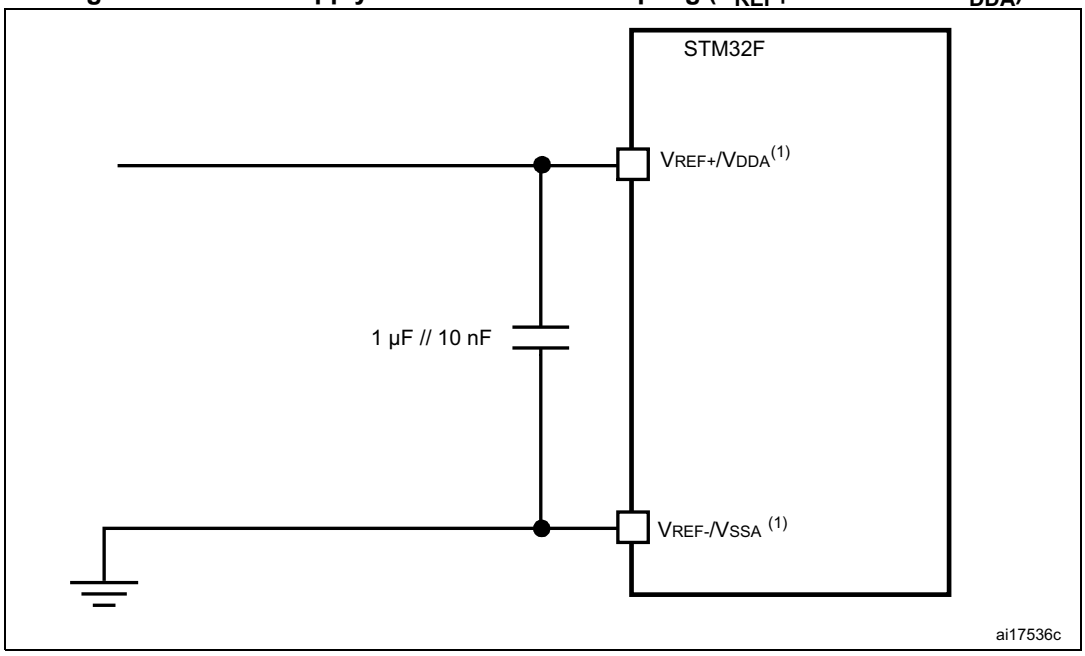
1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 44. I²S master timing diagram (Philips protocol)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 51. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA100. V_{REF+} is also available on LQFP100. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

6.3.21 Temperature sensor characteristics

Table 81. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5	-	mV/°C
V_{25}(1)	Voltage at 25 °C	-	0.76	-	V
t_{START}(2)	Startup time	-	6	10	µs
T_{S_temp}(2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	µs

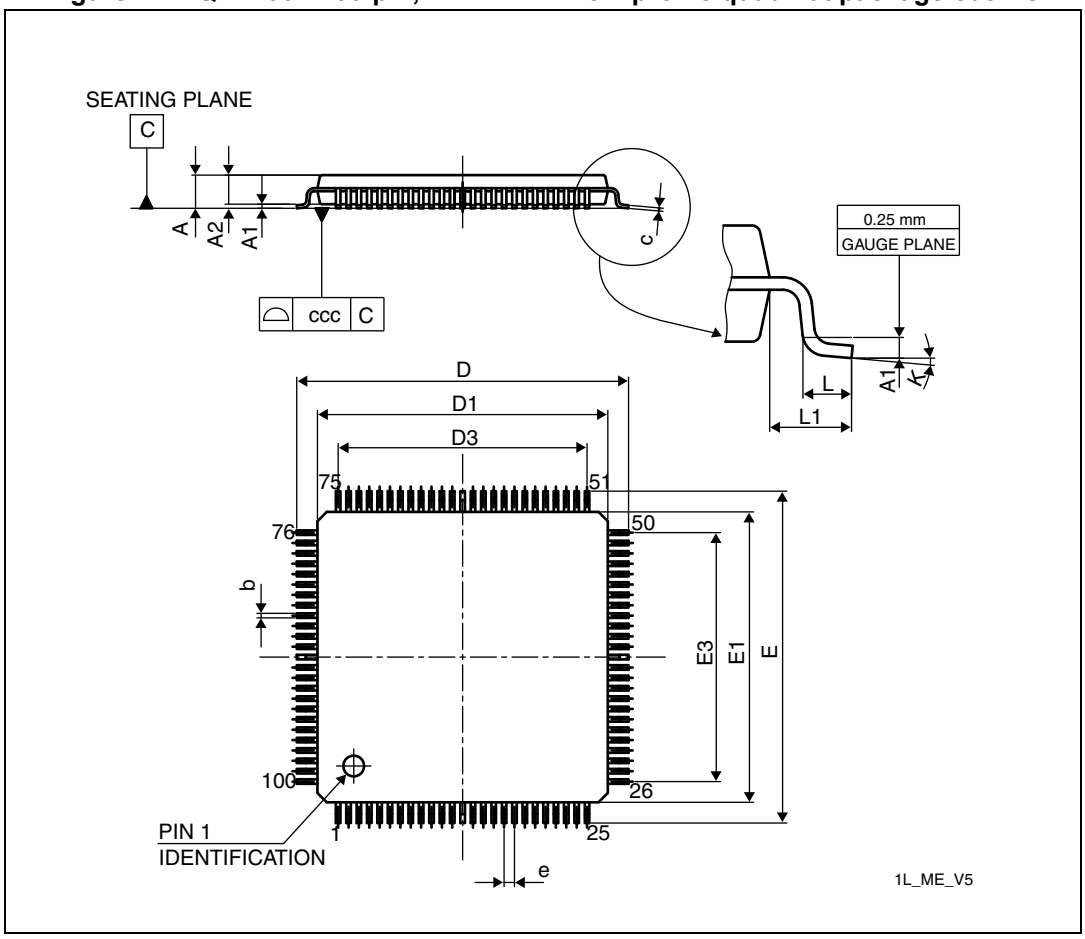
1. Guaranteed by characterization results.
2. Guaranteed by design.

Table 82. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF 7A2C - 0x1FFF 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C, V_{DDA}= 3.3 V	0x1FFF 7A2E - 0x1FFF 7A2F

7.4 LQFP100 package information

Figure 72. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale. Dimensions are in millimeters.

Table 107. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

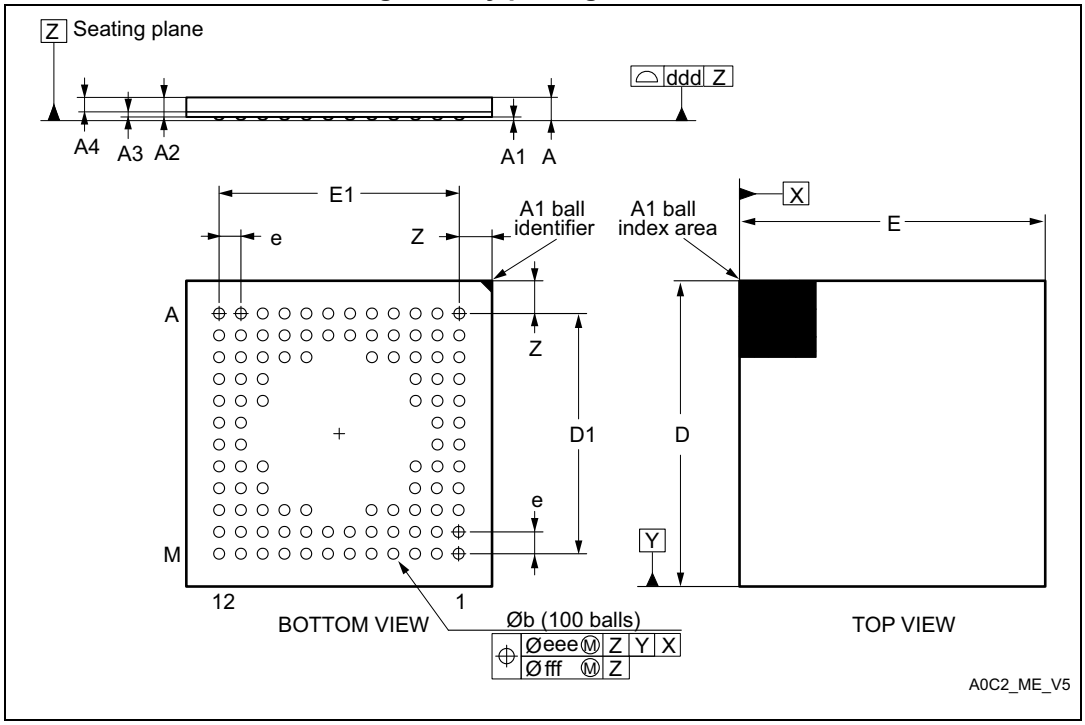
Table 108. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.6 UFBGA100 package information

Figure 78. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 109. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-