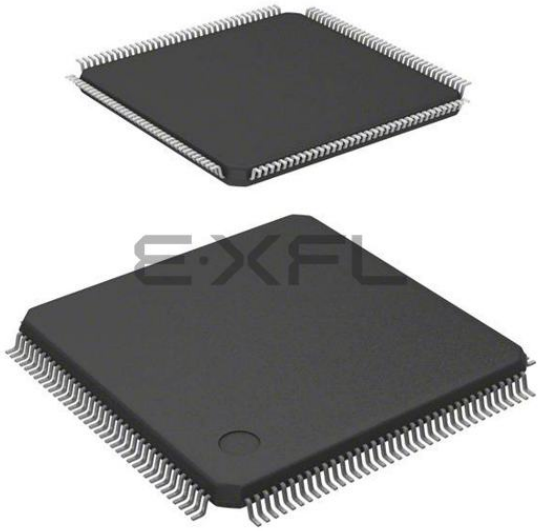

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f423zht6

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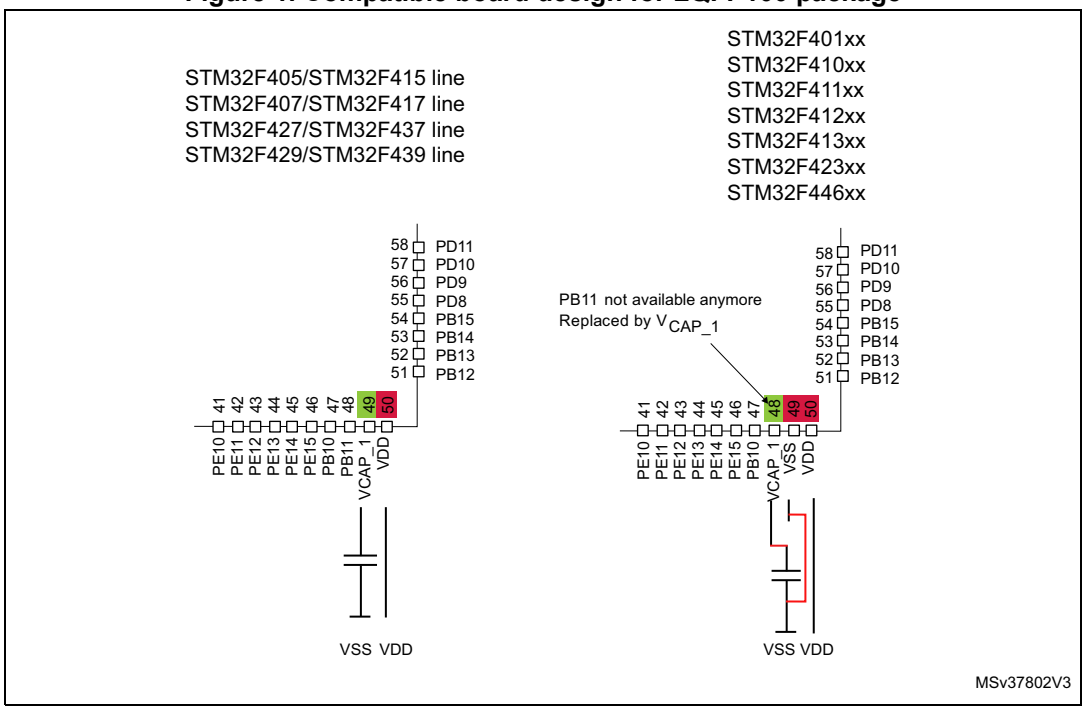
3. 81 pins packages: TIM4: ETR pin not available.
4. 48 pins packages: TIM8:CH1, CH2, CH3 and CH4 pins not available.

2.1 Compatibility with STM32F4 series

The STM32F423xH are fully software and feature compatible with the STM32F4 series (STM32F42x, STM32F401, STM32F43x, STM32F41x, STM32F405 and STM32F407)

The STM32F423xH can be used as drop-in replacement of the other STM32F4 products but some slight changes have to be done on the PCB board.

Figure 1. Compatible board design for LQFP100 package



3.18.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal power supply supervisor availability

Package	Regulator ON	Regulator OFF	Power supply supervisor ON	Power supply supervisor OFF
UFQFPN48	Yes	No	Yes	No
LQFP64	Yes	No	Yes	No
WLCSP81	Yes BYPASS_REG set to V_{SS}	Yes BYPASS_REG set to V_{DD}	Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
LQFP100	Yes	No	Yes	No
LQFP144	Yes	No	Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
UFBGA100	Yes BYPASS_REG set to V_{SS}	Yes BYPASS_REG set to V_{DD}		
UFBGA144	Yes BYPASS_REG set to V_{SS}	Yes BYPASS_REG set to V_{DD}		

3.19 Real-time clock (RTC) and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC features a reference clock detection, a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The backup registers are 32-bit registers used to store 80 byte of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see *Section 3.20: Low-power modes*).

3.22.6 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.22.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.23 Inter-integrated circuit interface (I^2C)

The devices feature up to four I^2C bus interfaces which can operate in multimaster and slave modes:

- One I^2C interface supports the Standard mode (up to 100 kHz), Fast-mode (up to 400 kHz) modes and Fast-mode plus (up to 1 MHz).
- Three I^2C interfaces support the Standard mode (up to 100 KHz) and the Fast mode (up to 400 KHz). Their frequency can be increased up to 1 MHz. For more details on the complete solution, refer to the nearest STMicroelectronics sales office.

All I^2C interfaces features 7/10-bit addressing mode and 7-bit addressing mode (as slave) and embed a hardware CRC generation/verification.

They can be served by DMA and they support SMBus 2.0/PMBus.

The devices also include programmable analog and digital noise filters (see *Table 6*).

Table 6. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks

3.24 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) as well as six universal asynchronous receiver transmitters (UART4, UART5, UART7, UART8, UART9 and UART10).

These ten interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. USART1, USART6, UART9 and UART10 can communicate at speeds up to 12.5 Mbit/s. The other interfaces communicate at up to 6.25 bit/s.

Table 10. STM32F423xH pin definition (continued)

Pin Number							Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP81	LQFP100	UFBGA100	UFBGA144	LQFP144						
-	-	-	-	-	D8	125	PG10	I/O	FT	-	FSMC_NE3, EVENTOUT	-
-	-	-	-	-	C8	126	PG11	I/O	FT	-	CAN2_RX, UART10_RX, EVENTOUT	-
-	-	-	-	-	B8	127	PG12	I/O	FT	-	USART6_RTS, CAN2_TX, UART10_TX, FSMC_NE4, EVENTOUT	-
-	-	-	-	-	D7	128	PG13	I/O	FT	-	TRACED2, USART6_CTS, FSMC_A24, EVENTOUT	-
-	-	-	-	-	C7	129	PG14	I/O	FT	-	TRACED3, USART6_TX, QUADSPI_BK2_IO3, FSMC_A25, EVENTOUT	-
-	-	-	-	-	-	130	VSS	S	-	-	-	-
-	-	-	-	-	F6	131	VDD	S	-	-	-	-
-	-	-	-	-	B7	132	PG15	I/O	FT	-	USART6_CTS, EVENTOUT	-
39	55	A5	89	A8	A7	133	PB3	I/O	FTf	-	JTDO-SWO, TIM2_CH2, I2CFMP1_SDA, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, USART1_RX, UART7_RX, I2C2_SDA, SAI1_SD_A, CAN3_RX, EVENTOUT	-
40	56	B5	90	A7	A6	134	PB4	I/O	FT	-	JTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, I2S3ext_SD, UART7_TX, I2C3_SDA, SAI1_SCK_A, CAN3_TX, SDIO_D0, EVENTOUT	-

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3 σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.7 V ≤ V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2 σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 19*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 20*.

Figure 19. Pin loading conditions

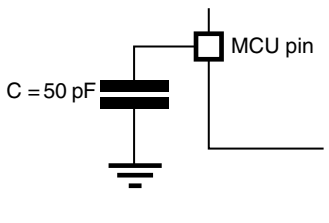


Figure 20. Input voltage measurement

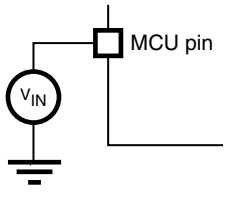


Table 25. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory- V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)(3)	100	30.2	32.03	32.71	34.69	38.46	mA
			84	24.3	25.77	26.58	28.47	32.16	
			64	16.8	17.80	18.66	20.53	23.85	
			50	13.2	14.05	15.12	16.85	20.27	
			25	7.1	7.62	8.92	10.81	14.11	
			20	6.1	6.69	7.95	9.72	13.09	
		HSI, PLL OFF, all peripherals enabled(2)	16	4.4	4.99	6.28	8.18	11.45	
			1	0.9	1.50	2.88	4.58	8.00	
		External clock, PLL ON(4) all peripherals disabled(2)	100	12.6	13.46	14.75	16.68	20.54	
			84	10.2	10.90	12.25	14.10	17.84	
			64	7.2	7.70	8.95	10.81	14.14	
			50	5.7	6.26	7.56	9.26	12.72	
			25	3.2	3.77	5.11	6.82	10.26	
			20	2.9	3.41	4.79	6.49	9.92	
		HSI, PLL OFF, all peripherals disabled(2)	16	2.1	2.63	3.91	5.80	9.06	
			1	0.8	1.34	2.72	4.42	7.86	

1. Guaranteed by characterization results..
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.
4. Refer to *Table 47* and RM0383 for the possible PLL VCO setting

Table 26. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON(2), all peripherals enabled(3)	100	30.7	32.85(4)	33.30	35.37	39.08	mA
			84	24.7	26.48	27.15	28.94	32.65	
			64	17.2	18.36	19.14	20.88	24.29	
			50	13.6	14.54	15.45	17.27	20.58	
			25	7.4	7.97	9.23	11.05	14.42	
			20	6.4	6.99	8.18	10.03	13.32	
		HSI, PLL OFF, all peripherals enabled(3)	16	4.5	5.04	6.32	8.23	11.50	
			1	1.0	1.50	2.89	4.59	8.01	
		External clock, PLL ON(2) all peripherals disabled(3)	100	13.1	14.36	15.33	17.25	20.98	
			84	10.7	11.67	12.73	14.56	18.21	
			64	7.5	8.23	9.40	11.13	14.52	
			50	6.1	6.74	7.89	9.61	12.98	
			25	3.5	4.19	5.37	7.08	10.48	
			20	3.2	3.71	5.02	6.72	10.15	
		HSI, PLL OFF, all peripherals disabled(3)	16	2.1	2.67	3.95	5.84	9.10	
			1	0.8	1.35	2.72	4.43	7.87	

1. Guaranteed by characterization results.
2. Refer to *Table 47* and RM0383 for the possible PLL VCO setting
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
4. Tested in production.

Table 30. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)				Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, PLL ON, all peripherals enabled(2)	100	42.9	45.86	45.76	47.88	51.71	mA
			84	35.4	37.90	38.16	40.01	43.26	
			64	26.2	28.19	28.74	30.37	33.54	
			50	20.7	22.32	22.50	24.34	27.73	
			25	11.1	11.87	12.87	14.72	18.08	
			20	9.4	10.05	11.26	13.16	16.46	
		HSI, PLL OFF, all peripherals enabled	16	7.1	7.72	9.06	10.90	14.29	
			1	1.2	1.84	3.10	4.84	8.20	
		External clock, PLL ON(2) all peripherals disabled	100	25.4	27.83	27.84	29.93	33.66	
			84	21.4	23.44	24.10	25.77	29.04	
			64	16.6	18.31	19.17	20.72	23.86	
			50	13.2	15.10	14.95	16.71	20.13	
			25	7.2	7.90	9.01	10.88	14.25	
			20	6.2	6.83	8.05	9.88	13.15	
		HSI, PLL OFF, all peripherals disabled	16	4.8	5.37	6.70	8.52	11.89	
			1	1.0	1.62	2.96	4.67	8.07	

1. Guaranteed by characterization results.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.
4. Tested in production.

Table 39. Peripheral current consumption (continued)

Peripheral		I_{DD} (Typ)			Unit
		Scale 1	Scale 2	Scale 3	
APB2	AHB-APB2 bridge	0.10	0.11	0.09	µA/MHz
	TIM1	6.78	6.46	5.80	
	TIM8	6.94	6.62	5.94	
	USART1	3.14	3.00	2.69	
	USART6	3.12	2.98	2.67	
	UART9	2.89	1.98	1.75	
	UART10	2.91	2.00	1.77	
	ADC1	3.45	3.29	2.95	
	SDIO	3.54	3.37	3.03	
	SPI1	1.52	1.46	1.31	
	SPI4	1.50	1.43	1.28	
	SYSCFG	0.58	0.55	0.50	
	EXT1	0.91	0.86	0.78	
	TIM9	2.95	2.81	2.53	
	TIM10	1.88	1.79	1.61	
	TIM11	1.86	1.77	1.59	
	SPI5	1.50	1.43	1.30	
	SAI	2.89	2.75	2.47	
	DFSDM1	4.43	4.21	3.80	
	DFSDM2	7.08	6.76	6.05	
Bus Matrix		4.06	3.87	3.45	

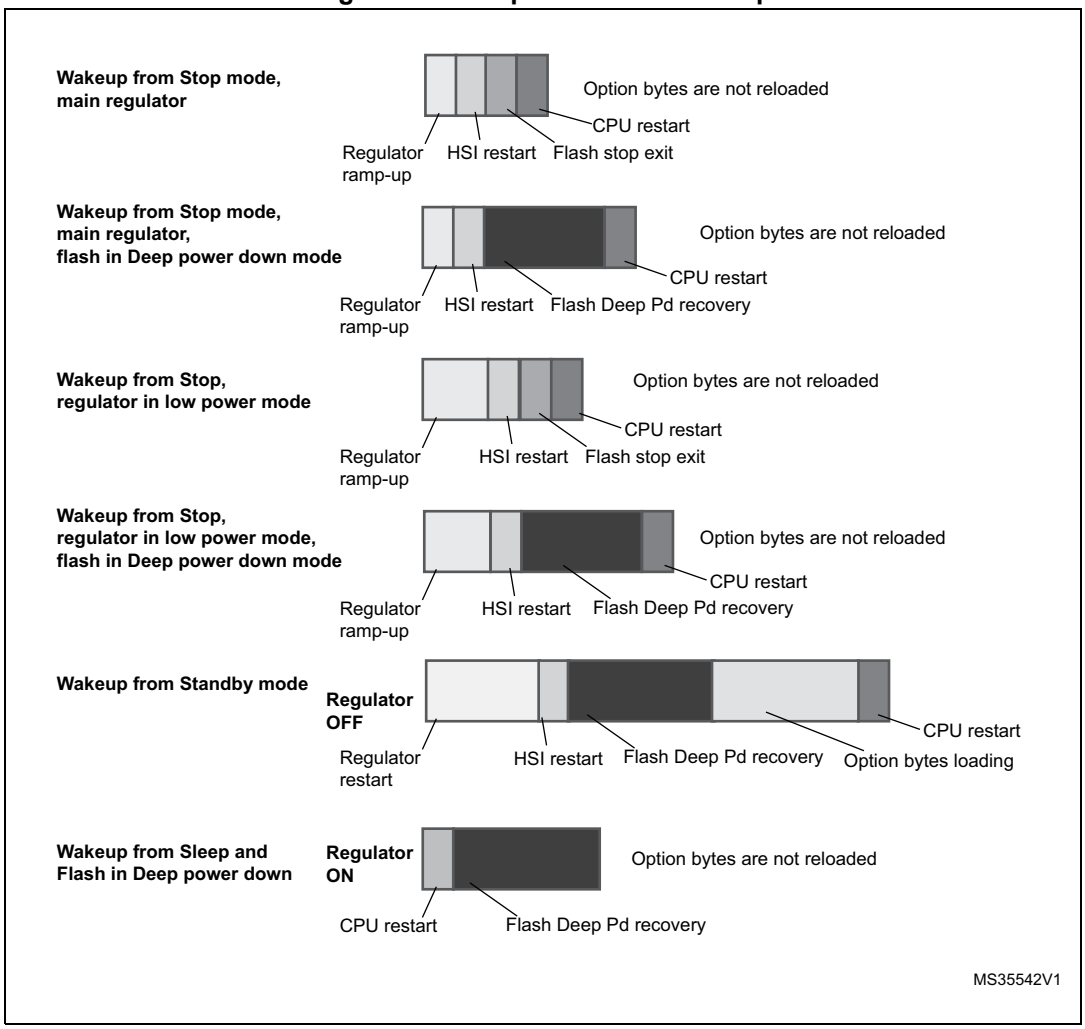
1. N is the number of stream enable (1...8).

6.3.7 Wakeup time from low-power modes

The wakeup times given in *Table 40* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0/PC0/PC1) pins are used to wakeup from Standby, Stop and Sleep modes.

Figure 26. Low-power mode wakeup



All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Figure 27. High-speed external clock source AC timing diagram

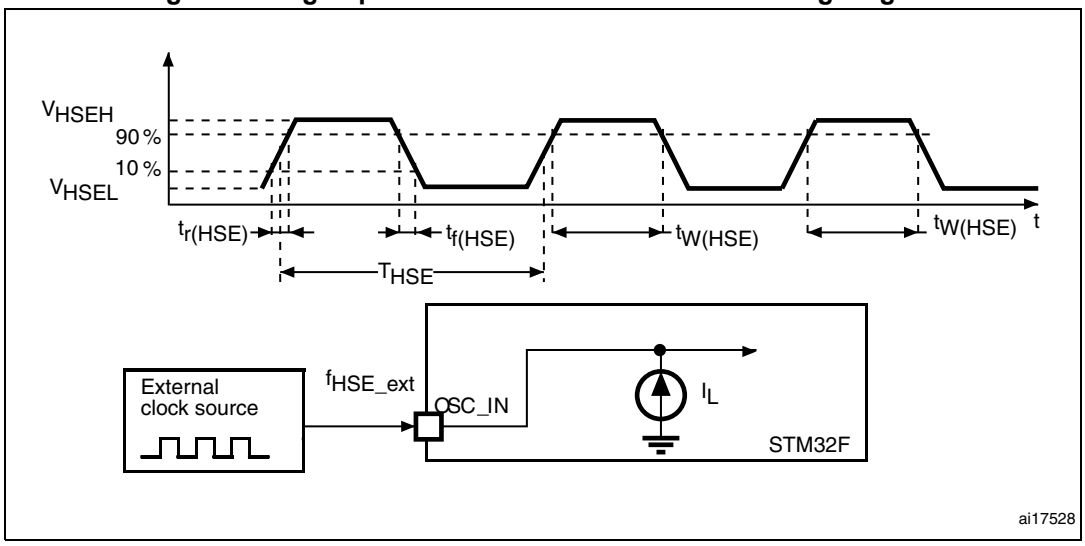
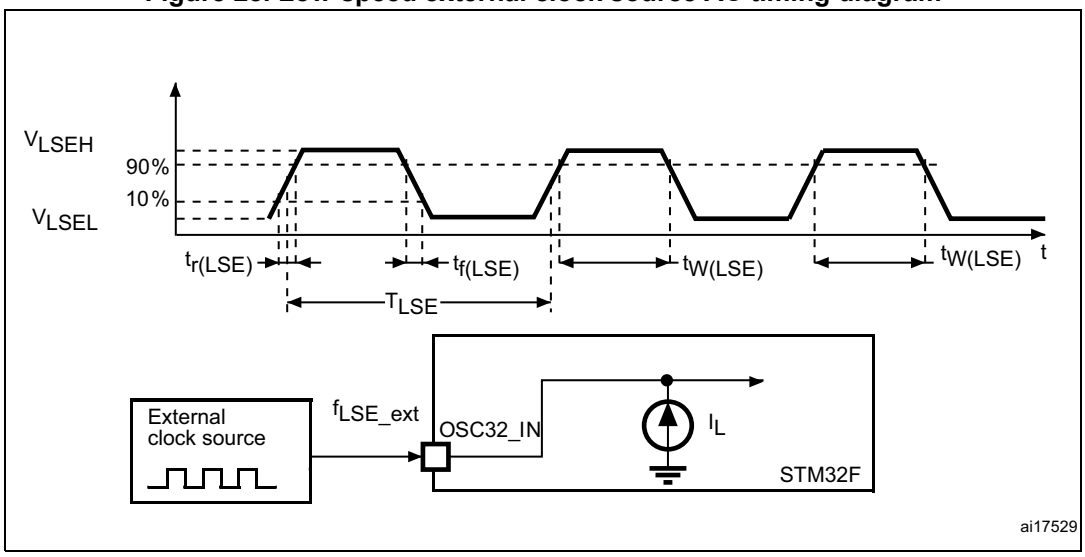


Figure 28. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 43*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 55*. They are based on the EMS levels and classes defined in application note AN1709.

Table 54. EMS characteristics for LQFP144 package

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144 T_A = +25 °C, f_{HCLK} = 100 MHz, conforms to IEC 61000-4-2	1B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144 T_A = +25 °C, f_{HCLK} = 100 MHz, conforms to IEC 61000-4-4	3B

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, on LQFP144 packages and PDR_ON on WLCSP81.

As a consequence, it is recommended to add a serial resistor (1 kΩ maximum) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

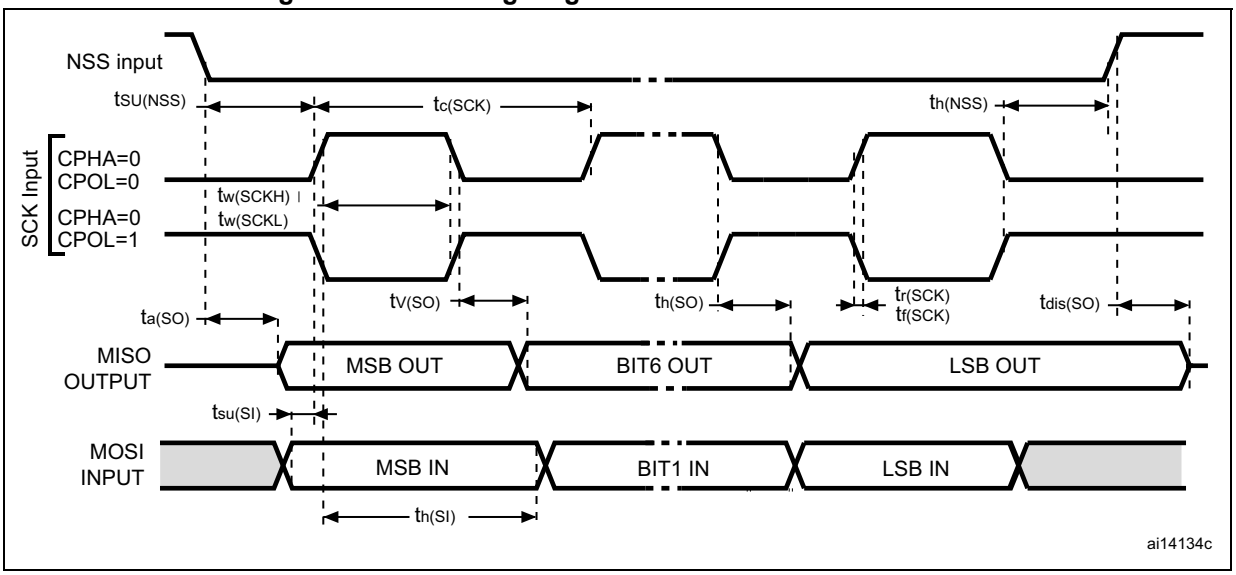
- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Table 67. SPI dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{a(SO)}$	Data output access time	Slave mode	7	-	21	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	5	-	12	ns
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge), 2.7 V < V_{DD} < 3.6 V	-	7	12.5	ns
		Slave mode (after enable edge), 1.71 V < V_{DD} < 3.6 V	-	7	19	
$t_{v(MO)}$		Master mode	-	2	3	
$t_{h(SO)}$	Data output hold time	Slave mode 1.71 V < V_{DD} < 3.6 V	6	-	-	ns
$t_{h(MO)}$		Master mode	1.5	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%

Figure 40. SPI timing diagram - slave mode and CPHA = 0



6.3.25 DFSDM characteristics

Unless otherwise specified, the parameters given in *Table 87* for DFSDM are derived from tests performed under the ambient temperature, f_{APB2} frequency and V_{DD} supply voltage conditions summarized in *Table 17: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 * V_{DD}

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDM_CKINy, DFSDM_DATINy, DFSDM_CKOUT for DFSDM).

Table 87. DFSDM characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	1.71 < V_{DD} < 3.6 V	-	-	f_{SYSCLK}	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0] = 0,1), External clock mode (SPICKSEL[1:0] = 0, 1.71 < V_{DD} < 3.6 V	-	-	20 ($f_{DFBDMCLK}$ / 4	
		SPI mode (SITP[1:0] = 0,1), External clock mode (SPICKSEL[1:0] = 0, 2.7 < V_{DD} < 3.6 V	-	-	20 ($f_{DFBDMCLK}$ / 4	
		SPI mode (SITP[1:0] = 0,1), Internal clock mode (SPICKSEL[1:0] ≠ 0, 1.71 < V_{DD} < 3.6 V	-	-	20 ($f_{DFBDMCLK}$ / 4	
		SPI mode (SITP[1:0] = 0,1), Internal clock mode (SPICKSEL[1:0] ≠ 0, 2.7 < V_{DD} < 3.6 V	-	-	20 ($f_{DFBDMCLK}$ / 4	
f_{CKOUT}	Output clock frequency	1.71 < V_{DD} < 3.6 V	-	-	20	
$DuCy_{CKOUT}$	Output clock frequency duty cycle	1.71 < V_{DD} < 3.6 V	45	50	55	%

1. C_L = 30 pF.
2. Based on characterization.

Table 91. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	8 * t_{HCLK} - 1	8 * t_{HCLK} + 1	ns
$t_{w(NWE)}$	FSMC_NWE low time	6 * t_{HCLK} - 1.5	6 * t_{HCLK} + 0.5	
$t_{su(NWAIT\_NE)}$	FSMC_NWAIT valid before FSMC_NEx high	6 * t_{HCLK} - 1	-	
$t_{h(NE\_NWAIT)}$	FSMC_NEx hold time after FSMC_NWAIT invalid	4 * t_{HCLK} + 2	-	

1. C_L = 30 pF.
2. Based on characterization.

Figure 55. Asynchronous multiplexed PSRAM/NOR read waveforms

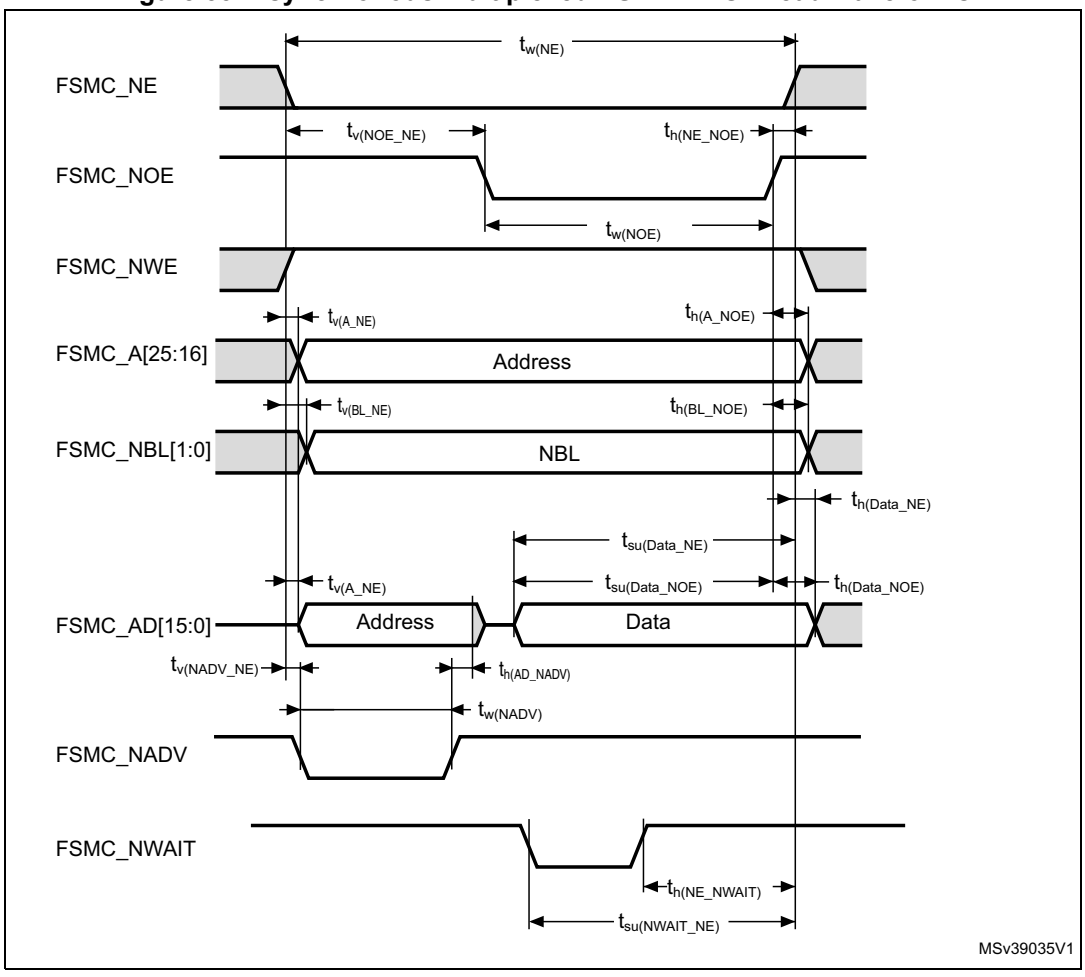


Figure 56. Asynchronous multiplexed PSRAM/NOR write waveforms

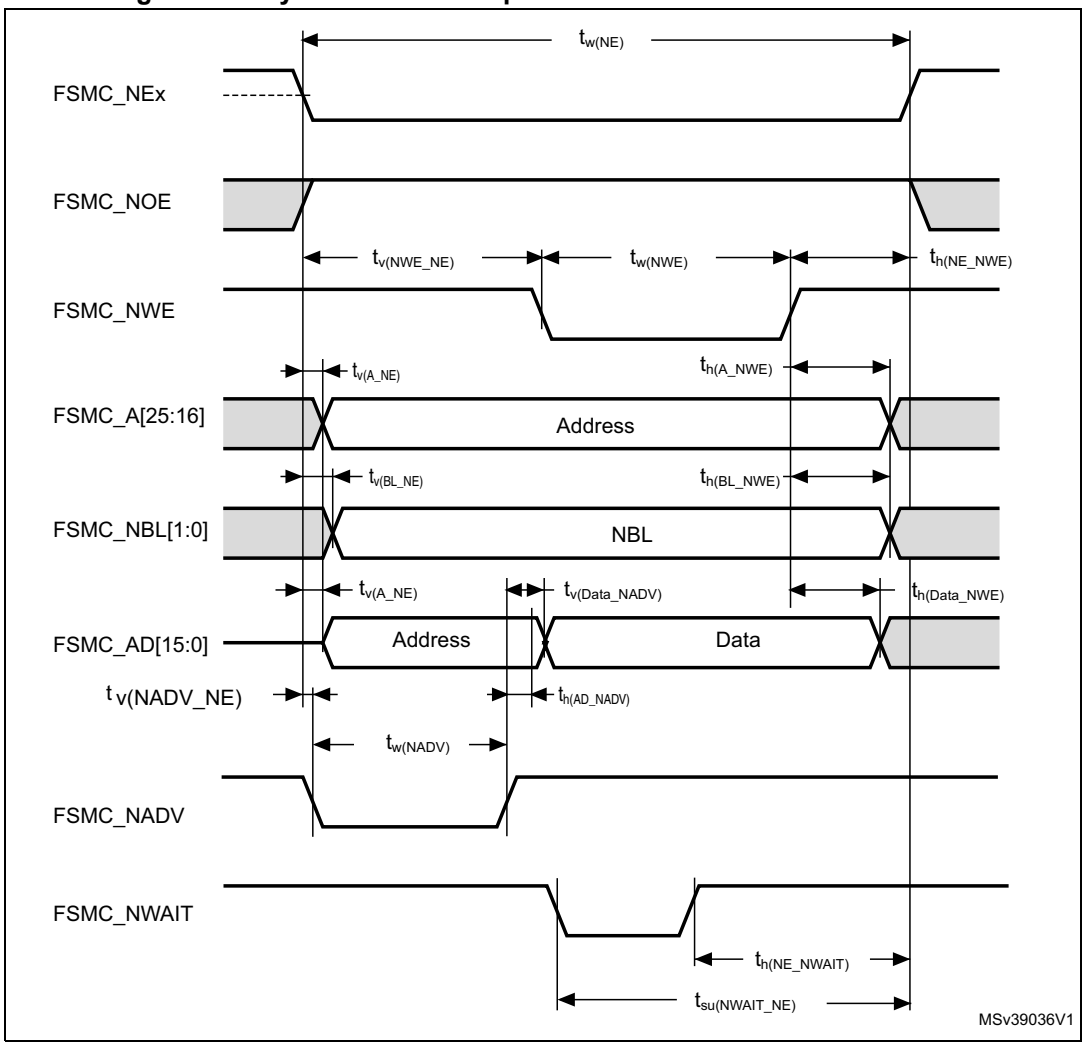
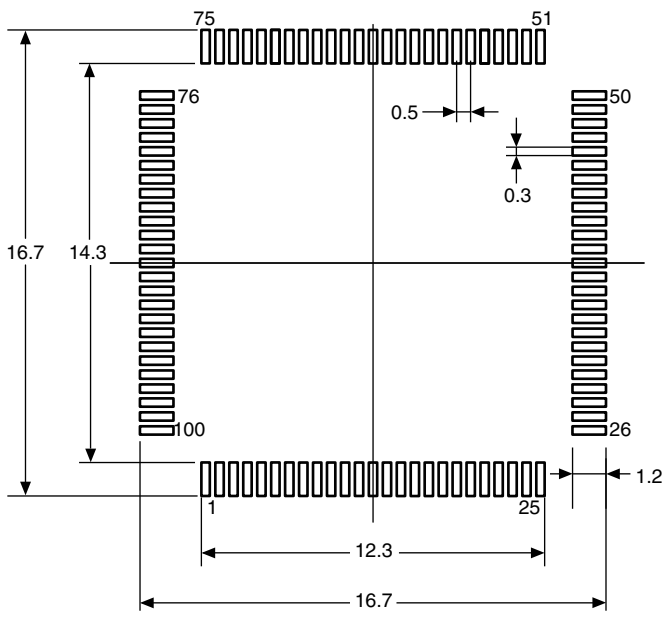


Table 107. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 73. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



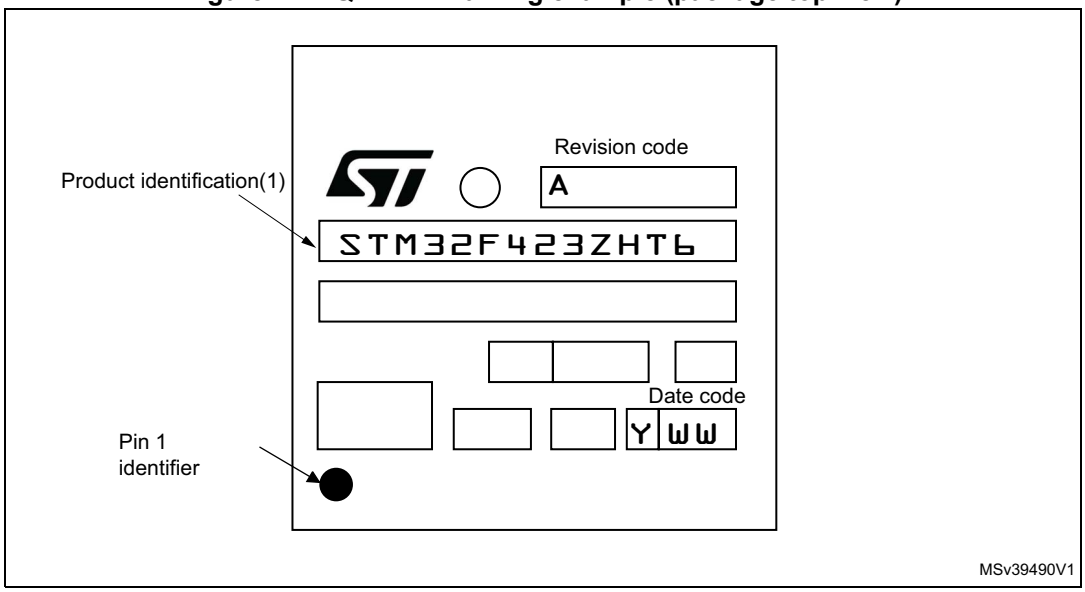
1. Dimensions are in millimeters.

Device marking for LQFP144

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 77. LQFP144 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.