Microchip Technology - AT32UC3L0128-AUT Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	36
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at32uc3l0128-aut

10.6 Module Configuration

The specific configuration for each HMATRIX instance is listed in the following tables.The module bus clocks listed here are connected to the system bus clocks. Please refer to the Power Manager chapter for details.

Table 10-3. HMATRIX Clocks

Clock Name	Description
CLK_HMATRIX	Clock for the HMATRIX bus interface

10.6.1 Bus Matrix Connections

The bus matrix has the several masters and slaves. Each master has its own bus and its own decoder, thus allowing a different memory mapping per master. The master number in the table below can be used to index the HMATRIX control registers. For example, HMATRIX MCFG0 register is associated with the CPU Data master interface.

Table 10-4. High Speed Bus Masters

Master 0	CPU Data
Master 1	CPU Instruction
Master 2	CPU SAB
Master 3	SAU
Master 4	PDCA

Each slave has its own arbiter, thus allowing a different arbitration per slave. The slave number in the table below can be used to index the HMATRIX control registers. For example, SCFG3 is associated with the Internal SRAM Slave Interface.

Accesses to unused areas returns an error result to the master requesting such an access.

Table 10-5. High Speed Bus Slaves

Slave 0	Internal Flash
Slave 1	HSB-PB Bridge A
Slave 2	HSB-PB Bridge B
Slave 3	Internal SRAM
Slave 4	SAU

12.7 User Interface

Table 12-7. PM Register Memory Map

Offset	Register	Register Name	Access	Reset
0x000	Main Clock Control	MCCTRL	Read/Write	0x00000000
0x004	CPU Clock Select	CPUSEL	Read/Write	0x00000000
0x008	HSB Clock Select	HSBSEL	Read-only	0x00000000
0x00C	PBA Clock Select	PBASEL	Read/Write	0x00000000
0x010	PBB Clock Select	PBBSEL	Read/Write	0x00000000
0x014 - 0x01C	Reserved			
0x020	CPU Mask	CPUMASK	Read/Write	0x00010001
0x024	HSB Mask	HSBMASK	Read/Write	0x0000007F
0x028	PBA Mask	PBAMASK	Read/Write	0x0FFFFFFF
0x02C	PBB Mask	PBBMASK	Read/Write	0x0000000F
0x030- 0x03C	Reserved			
0x040	PBA Divided Mask	PBADIVMASK	Read/Write	0x0000007F
0x044 - 0x050	Reserved			
0x054	Clock Failure Detector Control	CFDCTRL	Read/Write	0x00000000
0x058	Unlock Register	UNLOCK	Write-only	0x00000000
0x05C - 0x0BC	Reserved			
0x0C0	Interrupt Enable Register	IER	Write-only	0x00000000
0x0C4	Interrupt Disable Register	IDR	Write-only	0x00000000
0x0C8	Interrupt Mask Register	IMR	Read-only	0x00000000
0x0CC	Interrupt Status Register	ISR	Read-only	0x00000000
0x0D0	Interrupt Clear Register	ICR	Write-only	0x00000000
0x0D4	Status Register	SR	Read-only	0x00000020
0x0D8 - 0x15C	Reserved			
0x160	Peripheral Power Control Register	PPCR	Read/Write	0x000001FA
0x164 - 0x17C	Reserved			
0x180	Reset Cause Register	RCAUSE	Read-only	-[2]
0x184	Wake Cause Register	WCAUSE	Read-only	-[3]
0x188	Asynchronous Wake Up Enable Register	AWEN	Read/Write	0x00000000
0x18C - 0x3F4	Reserved			
0x3F8	Configuration Register	CONFIG	Read-only	0x00000043
0x3FC	Version Register	VERSION	Read-only	-[1]

Note: 1. The reset value is device specific. Please refer to the Module Configuration section at the end of this chapter.

2. Latest Reset Source.

3. Latest Wake Source.

12.7.6 PBA Divided Mask

Name: PBADIVMASK

Access Type: Read/Write

Offset: 0x040

Reset Value: 0x0000007F

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-		-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	MASK[6:0]						

- **MASK: Clock Mask**

  If bit n is written to zero, the clock divided by $2^{(n+1)}$ is stopped. If bit n is written to one, the clock divided by $2^{(n+1)}$ is enabled according to the current power mode. Table 12-10 shows what clocks are affected by the different MASK bits.

Table 12-10. Divided Clock Mask

Bit	USART0	USART1	USART2	USART3	TC0	TC1
0	-	-	-	-	TIMER_CLOCK2	TIMER_CLOCK2
1	-	-	-	-	-	-
2	CLK_USART/ DIV	CLK_USART/ DIV	CLK_USART/ DIV	CLK_USART/ DIV	TIMER_CLOCK3	TIMER_CLOCK3
3	-	-	-	-	-	-
4	-	-	-	-	TIMER_CLOCK4	TIMER_CLOCK4
5	-	-	-	-	-	-
6	-	-	-	-	TIMER_CLOCK5	TIMER_CLOCK5

Note that this register is protected by a lock. To write to this register the UNLOCK register has to be written first. Please refer to the UNLOCK register description for details.

12.7.17 Wake Cause Register

Name: WCAUSE

Access Type: Read-only

Offset: 0x184

Reset Value: Latest Wake Source

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">WCAUSE[31:24]</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">WCAUSE[23:16]</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">WCAUSE[15:8]</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">WCAUSE[7:0]</td></tr>
</table>

A bit in this register is set on wake up caused by the peripheral referred to in Table 12-12 on page 181.

Table 12-12. Wake Cause

Bit	Wake Cause
0	CAT
1	ACIFB
2	ADCIFB
3	TWI Slave 0
4	TWI Slave 1
5	WAKE_N
6	ADCIFB Pen Detect
15:7	-
16	EIC
17	AST
31:18	-

13.6.17 Voltage Regulator Calibration Register

Name: VREGCR

Access Type: Read/Write

Reset Value: -

31	30	29	28	27	26	25	24
SFV	INTPD	-	-	-	DBG-	POR18VALUE	POR33VALUE

23	22	21	20	19	18	17	16
POR18MASK	POR18STATUS	POR18EN	POR33MASK	POR33STATUS	POR33EN	DEEPDIS	FCD

15	14	13	12	11	10	9	8
-	-	-	-	CALIB			

7	6	5	4	3	2	1	0
ON	VREGOK	EN	-	-	SELVDD		

- **SFV: Store Final Value**

  0: The register is read/write.

  1: The register is read-only, to protect against further accidental writes.

  This bit is cleared by a Power-on Reset.

- **INTPD: Internal Pull-down**

  This bit is used for test purposes only.

  0: The voltage regulator output is not pulled to ground.

  1: The voltage regulator output has a pull-down to ground.

- **POR18VALUE: Power-on Reset 1.8V Output Value**

  0: VDDCORE voltage is below the POR18 power-on threshold level.

  1: VDDCORE voltage is above the POR18 power-on threshold level.

  This bit is read-only. Writing to this bit has no effect.

- **POR33VALUE: Power-on Reset 3.3V Output Value**

  0: Internal regulator supply voltage is below the POR33 power-on threshold level.

  1: Internal regulator supply voltage is above the POR33 power-on threshold level.

  This bit is read-only. Writing to this bit has no effect.

- **POR18MASK: Power-on Reset 1.8V Output Mask**

  0: Power-on Reset is not masked.

  1: Power-on Reset is masked.

- **POR18STATUS: Power-on Reset 1.8V Status**

  0: Power-on Reset is disabled.

  1: Power-on Reset is enabled.

  This bit is read-only. Writing to this bit has no effect.

- **POR18EN: Power-on Reset 1.8V Enable**

  Writing a zero to this bit disables the POR18 detector.

  Writing a one to this bit enables the POR18 detector.

- **POR33MASK: Power-on Reset 3.3V Output Mask**

  0: Power-on Reset 3.3V is not masked.

13.6.27 Fractional Prescaler Control Register

Name: FPCR

Access Type: Read/Write

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	-	CKSEL			FPEN

- **CKSEL: Clock input selection**
  This field selects the Clock input for the prescaler. See the “FP clock sources” table in the SCIF Module Configuration section for details. It must not be changed if the FPEN is one.
- **FPEN: High Resolution Prescaler Enable**
  0: The Fractional Prescaler is disabled.
  1: The Fractional Prescaler is enabled.

18.7.18 Lock Register

Name: LOCK

Access: Read/Write, Set, Clear, Toggle

Offset: 0x1A0, 0x1A4, 0x1A8, 0x1AC

Reset Value: -

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-31: Lock State**

0: Pin is unlocked. The corresponding bit can be changed in any GPIO register for this port.

1: Pin is locked. The corresponding bit can not be changed in any GPIO register for this port.

The value of LOCK determines which bits are locked in the lockable registers.

The LOCK, LOCKC, and LOCKT registers are protected, which means they can only be written immediately after a write to the UNLOCK register with the proper KEY and OFFSET.

LOCKS is not protected, and can be written at any time.

- DLM=1: the response data length is defined by the Identifier bits according to the table below.

Table 19-8. Response Data Length if DLM = 1

IDCHR[5]	IDCHR[4]	Response Data Length [bytes]
0	0	2
0	1	2
1	0	4
1	1	8

19.6.5.11 Checksum

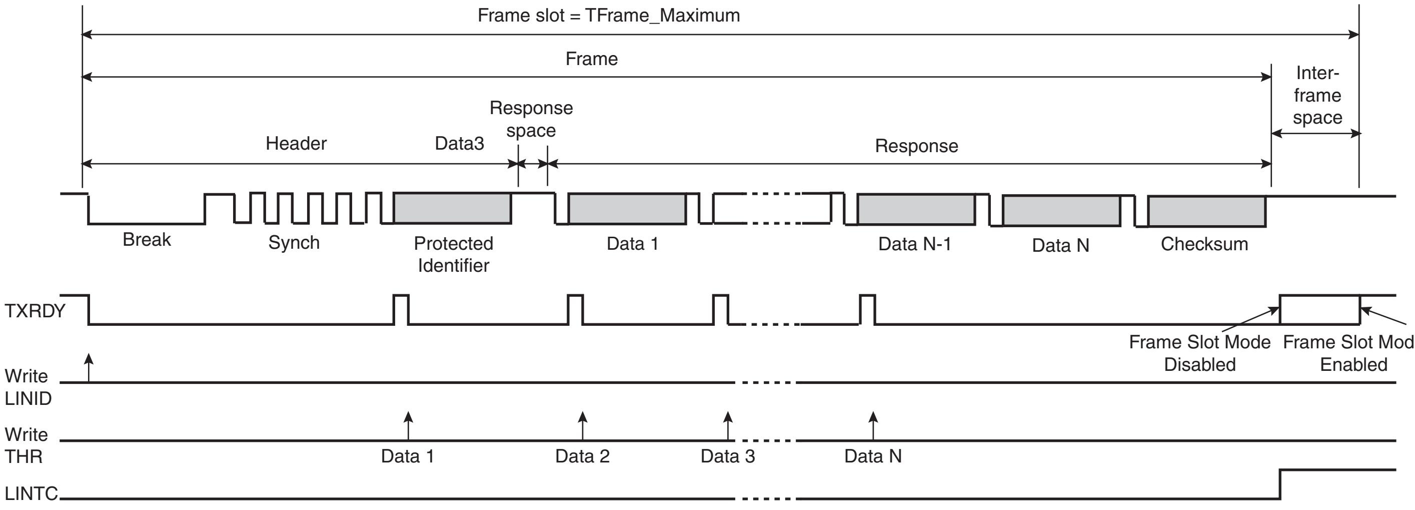
The last frame field is the checksum. It is configured by the Checksum Type (LINMR.CHKTYP), and the Checksum Disable (LINMR.CHKDIS) bits. TXRDY will not be set after the last THR data write if enabled. Writing a one to CHKDIS will disable the automatic checksum generation/checking, and the user may send/check this last byte manually, disguised as a normal data. The checksum is an inverted 8-bit sum with carry, either:

- over all data bytes, called a classic checksum. This is used for LIN 1.3 compliant slaves, and automatically managed when CHKDIS=0, and CHKTYP=1.
- over all data bytes and the protected identifier, called an enhanced checksum. This is used for LIN 2.0 compliant slaves, and automatically managed when CHKDIS=0, and CHKTYP=0.

19.6.5.12 Frame Slot Mode

A LIN master can be configured to use frame slots with a pre-defined minimum length. Writing a one to the Frame Slot Mode Disable bit (LINMR.FSDIS) disables this mode. This mode will not allow TXRDY to be set after a frame transfer until the entire frame slot duration has elapsed, in effect preventing the master from sending a new header. The LIN Transfer Complete bit (CSR.LINTC) will still be set after the checksum has been sent. Writing a one to CR.RSTST clears LINTC.

Figure 19-26. Frame Slot Mode with Automatic Checksum



The minimum frame slot size is determined by TFrame_Maximum, and calculated below (all values in bit periods):

- THeader_Nominal = 34

19.7.14 Write Protect Mode Register

Register Name: WPMR

Access Type: Read-write

Offset: 0xE4

Reset Value: See Table 19-10

31	30	29	28	27	26	25	24
WPKEY[23:16]							
23	22	21	20	19	18	17	16
WPKEY[15:8]							
15	14	13	12	11	10	9	8
WPKEY[7:0]							
7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	WPEN

- **WPKEY: Write Protect KEY**

  Has to be written to 0x555341 (“USA” in ASCII) in order to successfully write WPEN. Always reads as zero.

- **WPEN: Write Protect Enable**

  0 = Write protection disabled.

  1 = Write protection enabled.

Protects the registers:

- ”Mode Register” on page 408
- ”Baud Rate Generator Register” on page 418
- ”Receiver Time-out Register” on page 419
- ”Transmitter Timeguard Register” on page 420

Figure 22-8. Slave Transmitter with Multiple Data Bytes

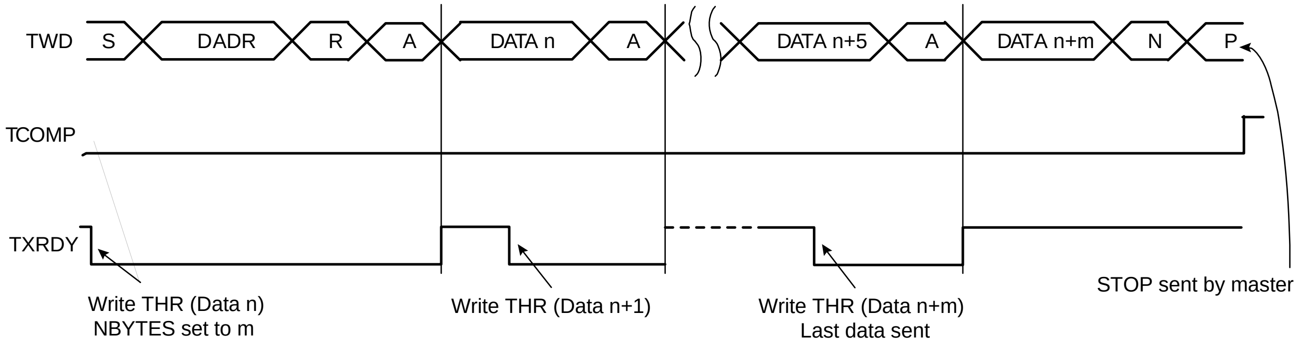
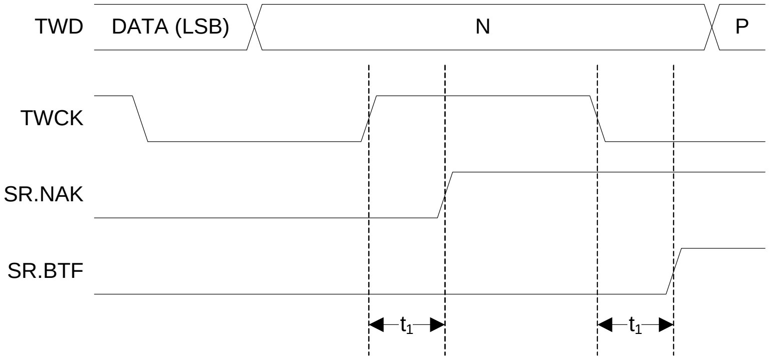


Figure 22-9. Timing Relationship between TWCK, SR.NAK, and SR.BTF



t_1: (CLK_TWIS period) x 2

22.8.4 Slave Receiver Mode

If the TWIS matches an address in which the R/$\overline{W}$ bit in the TWI address phase transfer is cleared, it will enter slave receiver mode and clear SR.TRA (note that SR.TRA is cleared one CLK_TWIS cycle after the relevant address match bit in the same register is set).

After the address phase, the following is repeated:

1. If SMBus mode and PEC is used, NBYTES must be set up with the number of bytes to receive. This is necessary in order to know which of the received bytes is the PEC byte. NBYTES can also be used to count the number of bytes received if using DMA.
2. Receive a byte. Set SR.BTF when done.
3. Update NBYTES. If CR.CUP is written to one, NBYTES is incremented, otherwise NBYTES is decremented. NBYTES is usually configured to count downwards if PEC is used.
4. After a data byte has been received, the slave transmits an ACK or NAK bit. For ordinary data bytes, the CR.ACK field controls if an ACK or NAK should be returned. If PEC is enabled and the last byte received was a PEC byte (indicated by NBYTES equal to zero), The TWIS will automatically return an ACK if the PEC value was correct, otherwise a NAK will be returned.
5. If STOP is received, SR.TCOMP will be set.
6. If REPEATED START is received, SR.REP will be set.

The TWI transfers require the receiver to acknowledge each received data byte. During the acknowledge clock pulse (9th pulse), the master releases the data line (HIGH), enabling the

22.10 Module Configuration

The specific configuration for each TWIS instance is listed in the following tables.The module bus clocks listed here are connected to the system bus clocks. Please refer to the Power Manager chapter for details.

Table 22-7. Module Clock Name

Module Name	Clock Name	Description
TWIS0	CLK_TWIS0	Clock for the TWIS0 bus interface
TWIS1	CLK_TWIS1	Clock for the TWIS1 bus interface

Table 22-8. Register Reset Values

Register	Reset Value
VERSION	0x00000120
PARAMETER	0x00000000

23.7.13 Interlinked Single Value Channel Set

Name: ISCHSETm

Access Type: Write-only

Offset: 0x30+m*0x10

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
SET							

23	22	21	20	19	18	17	16
SET							

15	14	13	12	11	10	9	8
SET							

7	6	5	4	3	2	1	0
SET							

- **SET: Single Value Channel Set**

  If the bit *n* in SET is one, the duty cycle of PWMA channel *n* will be updated with the value written to ISDUTY.

  If more than one ISCHSET register is present, ISCHSET0 controls channels 31 to 0 and ISCHSET1 controls channels 63 to 32.

Note: The duty registers will be updated with the value stored in the ISDUTY register when any ISCHSETm register is written. Synchronization takes place immediately when an ISCHSET register is written. The duty cycle registers will, however, not be updated until the synchronization is completed and the timebase counter reaches its top value in order to avoid glitches.

23.7.16 Composite Waveform Generation

Name: CWG

Access Type: Read/Write

Offset: 0x3C+k*0x10

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
XOR							

23	22	21	20	19	18	17	16
XOR							

15	14	13	12	11	10	9	8
XOR							

7	6	5	4	3	2	1	0
XOR							

- **XOR: Pair Waveform XOR'ed**

  If the bit *n* in XOR field is one, the pair of PWMA output waveforms will be XORed before output. The even number output will be the XOR'ed output and the odd number output will be reverse of it. For example, if bit 0 in XOR is one, the pair of PWMA output waveforms for channel 0 and 1 will be XORed together.

  If bit *n* in XOR is zero, normal waveforms are output for that pair. Note that

  If more than one CWG register is present, CWG0 controls the first 32 pairs, corresponding to channels 63 downto 0, and CWG1 controls the second 32 pairs, corresponding to channels 127 downto 64.

- **BCPC: RC Compare Effect on TIOB**

BCPC	Effect
0	none
1	set
2	clear
3	toggle

- **BCPB: RB Compare Effect on TIOB**

BCPB	Effect
0	none
1	set
2	clear
3	toggle

- **ASWTRG: Software Trigger Effect on TIOA**

ASWTRG	Effect
0	none
1	set
2	clear
3	toggle

- **AEEVT: External Event Effect on TIOA**

AEEVT	Effect
0	none
1	set
2	clear
3	toggle

- **ACPC: RC Compare Effect on TIOA**

ACPC	Effect
0	none
1	set
2	clear
3	toggle

24.7.13 Block Mode Register

Name: BMR

Access Type: Read/Write

Offset: 0xC4

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	TC2XC2S		TC1XC1S		TC0XC0S	

- **TC2XC2S: External Clock Signal 2 Selection**

TC2XC2S	Signal Connected to XC2
0	TCLK2
1	none
2	TIOA0
3	TIOA1

- **TC1XC1S: External Clock Signal 1 Selection**

TC1XC1S	Signal Connected to XC1
0	TCLK1
1	none
2	TIOA0
3	TIOA2

26.9.16 Channel Disable Register

Name: CHDR

Access Type: Write-only

Offset: 0x44

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24

23	22	21	20	19	18	17	16
CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16

15	14	13	12	11	10	9	8
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8

7	6	5	4	3	2	1	0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- **CHn: Channel N Disable**

Writing a zero to a bit in this register has no effect.

Writing a one to a bit in this register disables the corresponding channel.

Warning: If the corresponding channel is disabled during a conversion, or if it is disabled and then re-enabled during a conversion, its associated data and its corresponding DRDY and OVRE bits in SR are unpredictable.

The number of available channels is device dependent. Please refer to the Module Configuration section at the end of this chapter for information regarding how many channels are implemented.

28.7.15 Interrupt Enable Register

Name: IER

Access Type: Write-only

Offset: 0x44

Reset Value: -

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
DMATSC	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	ACQDONE	ACREADY

7	6	5	4	3	2	1	0
-	-	-	-	-	ATSC	ATCAL	-

Writing a zero to a bit in this register has no effect.

Writing a one to a bit in this register will set the corresponding bit in IMR.

28.7.18 Acquisition Initiation and Selection Register

Name:	AISR
Access Type:	Read/Write
Offset:	0x50
Reset Value:	0x00000000

31	30	29	28	27	26	25	24
-							

23	22	21	20	19	18	17	16
-							

15	14	13	12	11	10	9	8
-							

7	6	5	4	3	2	1	0
-						ACQSEL	

- **ACQSEL: Acquisition Type Selection**

  A write to this register initiates an acquisition of the following type:

  00: QTouch Group A.

  01: QTouch Group B.

  10: QMatrix Group.

  11: Undefined behavior.

  A read of this register will return the value that was previously written.

30.7.7 Receive Holding Register

Name:	RHR
Access Type:	Read-only
Offset:	0x18
Reset Value:	0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
RXDATA							

- **RXDATA: Received Data**
  The last byte received.

31.6.7 aWire Command Summary

The implemented aWire commands are shown in the table below. The responses from the AW are listed in Section 31.6.8.

Table 31-32. aWire Command Summary

COMMAND	Instruction	Description
0x01	AYA	“Are you alive”.
0x02	JTAG_ID	Asks AW to return the JTAG IDCODE.
0x03	STATUS_REQUEST	Request a status message from the AW.
0x04	TUNE	Tell the AW to report the current baud rate.
0x05	MEMORY_SPEED_REQUEST	Reports the speed difference between the aWire control and the SAB clock domains.
0x06	CHIP_ERASE	Erases the flash and all volatile memories.
0x07	DISABLE	Disables the AW.
0x08	2_PIN_MODE	Enables the DATAOUT pin and puts the aWire in 2-pin mode, where all responses are sent on the DATAOUT pin.
0x80	MEMORY_WRITE	Writes words, halfwords, or bytes to the SAB.
0x81	MEMORY_READ	Reads words, halfwords, or bytes from the SAB.
0x82	HALT	Issues a halt command to the device.
0x83	RESET	Issues a reset to the Reset Controller.
0x84	SET_GUARD_TIME	Sets the guard time for the AW.

All aWire commands are described below, with a summary in table form.

Table 31-33. Command/Response Description Notation

Command/Response	Description
Command/Response value	Shows the command/response value to put into the command/response field of the packet.
Additional data	Shows the format of the optional data field if applicable.
Possible responses	Shows the possible responses for this command.

31.6.7.1 AYA

This command asks the AW: “Are you alive”, where the AW should respond with an acknowledge.

Table 31-34. AYA Details

Command	Details
Command value	0x01
Additional data	N/A
Possible responses	0x40: ACK (Section 31.6.8.1) 0x41: NACK (Section 31.6.8.2)