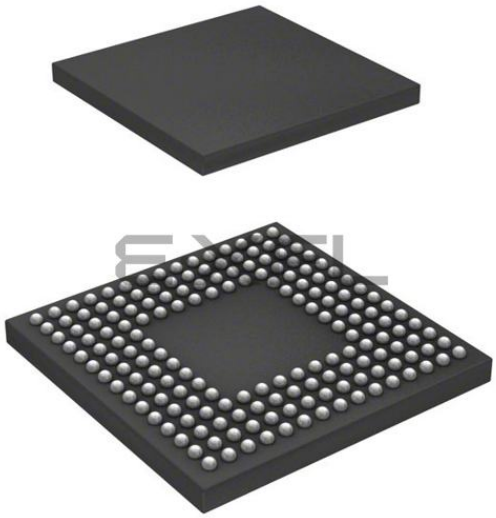
Renesas Electronics America Inc - R5F72145ADBG#U1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, I²C, SCI, SPI, USB
Peripherals	DMA, PWM, WDT
Number of I/O	112
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f72145adbg-u1

- Setting for Area 3

  Burst read/single write (burst length 1):

Data Bus Width	CAS Latency	Access Address	External Address Pin
16 bits	2	H'FFFC5440	H'0000440
	3	H'FFFC5460	H'0000460
32 bits	2	H'FFFC5880	H'0000880
	3	H'FFFC58C0	H'00008C0

  Burst read/burst write (burst length 1):

Data Bus Width	CAS Latency	Access Address	External Address Pin
16 bits	2	H'FFFC5040	H'0000040
	3	H'FFFC5060	H'0000060
32 bits	2	H'FFFC5080	H'0000080
	3	H'FFFC50C0	H'00000C0

  When a mode register write command is issued, the outputs of the external address pins are as follows.

When the data bus width of the area connected to SDRAM is 32 bits	A15 to A9	00000000 (burst read/burst write) 00000100 (burst read/single write)
	A8 to A6	010 (CAS latency 2), 011 (CAS latency 3)
	A5	0 (lap time = sequential)
	A4 to A2	000 (burst length 1)
When the data bus width of the area connected to SDRAM is 16 bits	A14 to A8	00000000 (burst read/burst write) 00000100 (burst read/single write)
	A7 to A5	010 (CAS latency 2), 011 (CAS latency 3)
	A4	0 (lap time = sequential)
	A3 to A1	000 (burst length 1)

Mode register setting timing is shown in figure 9.33. A PALL command (all bank pre-charge command) is firstly issued. A REF command (auto refresh command) is then issued 8 times. An MRS command (mode register write command) is finally issued. Idle cycles, of which number is specified by the WTRP1 and WTRP0 bits in CS3WCR, are inserted between the PALL and the first REF. Idle cycles, of which number is specified by the WTRC1 and WTRC0 bits in CS3WCR,

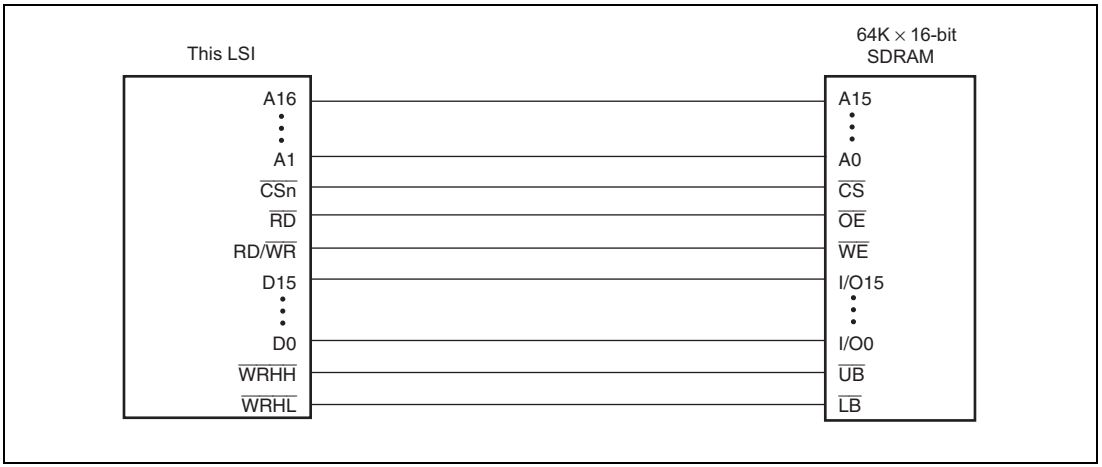

Figure 9.41 Example of Connection with 16-Bit Data-Width SRAM with Byte Selection

9.5.9 Burst ROM (Clock Synchronous) Interface

The burst ROM (clock synchronous) interface is supported to access a ROM with a synchronous burst function at high speed. The burst ROM interface accesses the burst ROM in the same way as a normal space. This interface is valid only for area 0.

In the first access cycle, wait cycles are inserted. In this case, the number of wait cycles to be inserted is specified by the W3 to W0 bits in CS0WCR. In the second and subsequent cycles, the number of wait cycles to be inserted is specified by the BW1 and BW0 bits in CS0WCR.

While the burst ROM (clock synchronous) is accessed, the $\overline{BS}$ signal is asserted only for the first access cycle and an external wait input is also valid for the first access cycle.

If the bus width is 16 bits, the burst length must be specified as 8. The burst ROM interface does not support the 8-bit bus width for the burst ROM.

The burst ROM interface performs burst operations for all read access. For example, in a longword access over a 16-bit bus, valid 16-bit data is read two times and invalid 16-bit data is read six times. These invalid data read cycles increase the memory access time and degrade the program execution speed and DMA transfer speed. To prevent this problem, using 16-byte read by the DMA is recommended. The burst ROM interface performs write access in the same way as normal space access.

10.3.5 DMA Reload Source Address Registers (RSAR)

The DMA reload source address registers (RSAR) are 32-bit readable/writable registers.

When the reload function is enabled, the RSAR value is written to the source address register (SAR) at the end of the current DMA transfer. In this case, a new value for the next DMA transfer can be preset in RSAR during the current DMA transfer. When the reload function is disabled, RSAR is ignored.

To transfer data of 16-bit or 32-bit width, specify the address with 16-bit or 32-bit address boundary respectively. To transfer data in units of 16 bytes, set a value at a 16-byte boundary.

RSAR is initialized to H'00000000 by a reset and retains the value in software standby mode and module standby mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Choose to detect DREQ by either the edge or level of the signal input with the DL and DS bits in CHCR_0 to CHCR_3 as shown in table 10.6. The source of the transfer request does not have to be the data transfer source or destination.

Table 10.6 Selecting External Request Detection with DL and DS Bits

CHCR		
DL bit	**DS bit**	**Detection of External Request**
0	0	Low level detection
	1	Falling edge detection
1	0	High level detection
	1	Rising edge detection

When DREQ is accepted, the DREQ pin enters the request accept disabled state (non-sensitive period). After issuing acknowledge DACK signal for the accepted DREQ, the DREQ pin again enters the request accept enabled state.

When DREQ is used by level detection, there are following two cases by the timing to detect the next DREQ after outputting DACK.

Overrun 0: Transfer is terminated after the same number of transfer has been performed as requests.

Overrun 1: Transfer is terminated after transfers have been performed for (the number of requests plus 1) times.

The DO bit in CHCR selects this overrun 0 or overrun 1.

Table 10.7 Selecting External Request Detection with DO Bit

CHCR	
DO bit	**External Request**
0	Overrun 0
1	Overrun 1

Table 11.31 Output Level Select Function

Bit 0	Function			
			Compare Match Output	
OLSP	Initial Output	Active Level	Up Count	Down Count
0	High level	Low level	Low level	High level
1	Low level	High level	High level	Low level

Figure 11.2 shows an example of complementary PWM mode output (1 phase) when OLSN = 1, OLSP = 1.

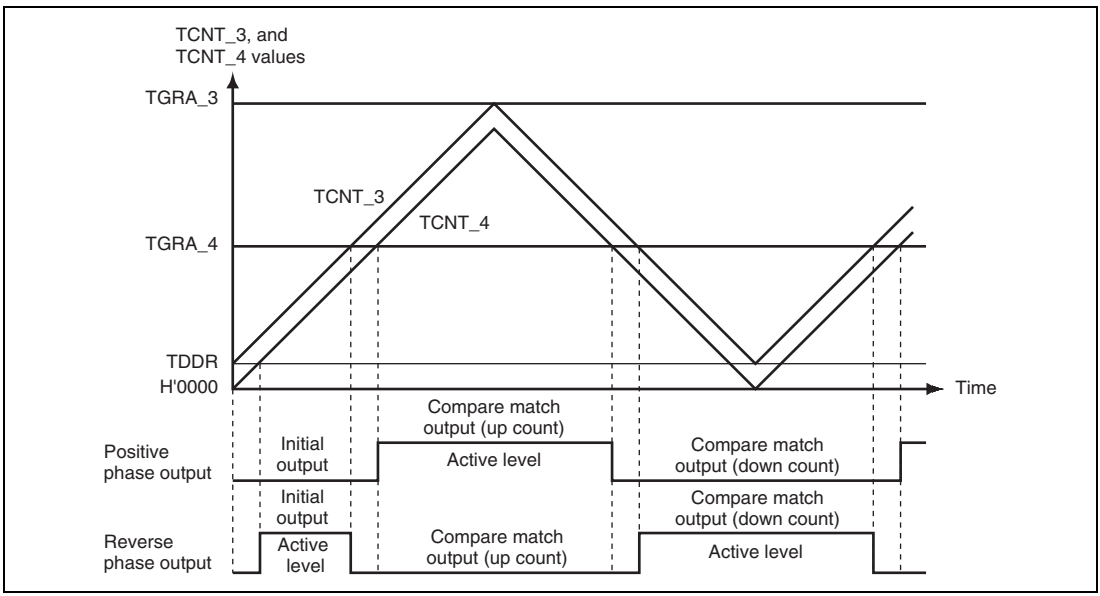

Figure 11.2 Complementary PWM Mode Output Level Example

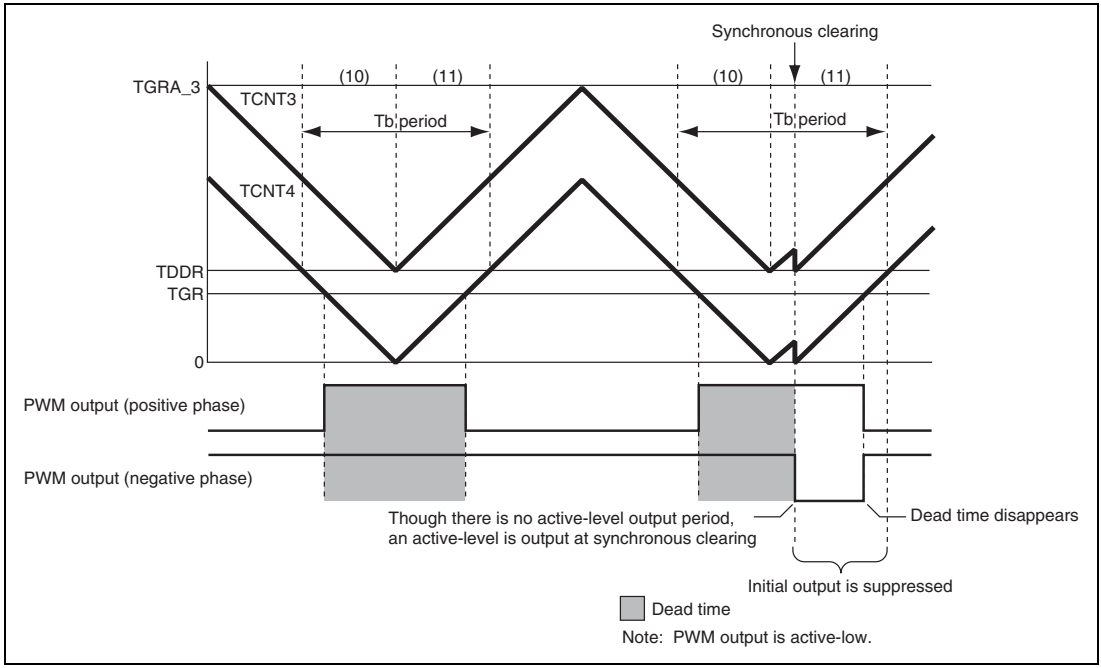

Figure 11.138 Example of Synchronous Clearing under Condition (2)

The above phenomena can be avoided by the following method.

Perform synchronous clearing after compare registers TGRB_3, TGRA_4, and TGRB_4 are all set to be at least twice of the setting of the timer dead time data register (TDDR).

Section 13 Port Output Enable 2 (POE2)

The port output enable 2 (POE2) can be used to place the high-current pins (PE9/TIOC3B, PE11/TIOC3D, PE12/TIOC4A, PE13/TIOC4B, PE14/TIOC4C, PE15/TIOC4D, PE0/TIOC4AS, PE1/TIOC4BS, PE2/TIOC4CS, PE3/TIOC4DS, PE5/TIOC3BS, PE6/TIOC3DS, PD15/TIOC4DS, PD14/TIOC4CS, PD13/TIOC4BS, PD12/TIOC4AS, PD11/TIOC3DS, PD10/TIOC3BS, PD24/TIOC4DS, PD25/TIOC4CS, PD26/TIOC4BS, PD27/TIOC4AS, PD28/TIOC3DS, and PD29/TIOC3BS) and the pins for channel 0 of the MTU2 (PE0/TIOC0A, PE1/TIOC0B, PE2/TIOC0C, PE3/TIOC0D, PB1/TIOC0A, PB2/TIOC0B, PB3/TIOC0C, and PB4/TIOC0D) in high-impedance state, depending on the change on the $\overline{\text{POE0}}$ to $\overline{\text{POE4}}$ and $\overline{\text{POE8}}$ input pins and the output status of the high-current pins, or by modifying register settings. It can also simultaneously generate interrupt requests.

13.1 Features

- Each of the $\overline{\text{POE0}}$ to $\overline{\text{POE4}}$ and $\overline{\text{POE8}}$ input pins can be set for falling edge, Pϕ/8 × 16, Pϕ/16 × 16, or Pϕ/128 × 16 low-level sampling.
- High-current pins and the pins for channel 0 of the MTU2 can be placed in high-impedance state by $\overline{\text{POE0}}$ to $\overline{\text{POE4}}$ and $\overline{\text{POE8}}$ pins falling-edge or low-level sampling.
- High-current pins can be placed in high-impedance state when the high-current pin output levels are compared and simultaneous active-level output continues for one cycle or more.
- High-current pins and the pins for channel 0 of the MTU2 can be placed in high-impedance state by modifying the POE2 register settings.
- Interrupts can be generated by input-level sampling or output-level comparison results.

The POE2 has input level detection circuits, output level comparison circuits, and a high-impedance request/interrupt request generating circuit as shown in the block diagram of figure 13.1.

Bit	Bit Name	Initial Value	R/W	Description
6	MTU2SP4CZE	0	R/W*	MTU2S Port 4 Output Comparison/High-Impedance Enable Specifies whether to compare output levels for the MTU2S high-current PD10/TIOC3BS and PD11/TIOC3DS pins and to place them in high-impedance state when the OSF2 bit is set to 1 while the OCE2 bit is 1 or when one of the POE4F and MTU2SHIZ bits is set to 1. 0: Does not compare output levels or place the pins in high-impedance state. 1: Compares output levels and places the pins in high-impedance state.
5	MTU2SP5CZE	0	R/W*	MTU2S Port 5 Output Comparison/High-Impedance Enable Specifies whether to compare output levels for the MTU2S high-current PD12/TIOC4AS and PD14/TIOC4CS pins and to place them in high-impedance state when the OSF2 bit is set to 1 while the OCE2 bit is 1 or when one of the POE4F and MTU2SHIZ bits is set to 1. 0: Does not compare output levels or place the pins in high-impedance state. 1: Compares output levels and places the pins in high-impedance state.
4	MTU2SP6CZE	0	R/W*	MTU2S Port 6 Output Comparison/High-Impedance Enable Specifies whether to compare output levels for the MTU2S high-current PD13/TIOC4BS and PD15/TIOC4DS pins and to place them in high-impedance state when the OSF2 bit is set to 1 while the OCE2 bit is 1 or when one of the POE4F and MTU2SHIZ bits is set to 1. 0: Does not compare output levels or place the pins in high-impedance state. 1: Compares output levels and places the pins in high-impedance state.

16.4 Operation

16.4.1 Overview

For serial communication, the SCI has an asynchronous mode in which characters are synchronized individually, and a clock synchronous mode in which communication is synchronized with clock pulses.

Asynchronous or clock synchronous mode is selected and the transmit format is specified in the serial mode register (SCSMR) as shown in table 16.14. The SCI clock source is selected by the combination of the C/$\overline{A}$ bit in SCSMR and the CKE1 and CKE0 bits in the serial control register (SCSCR) as shown in table 16.15.

(1) Asynchronous Mode

- Data length is selectable: 7 or 8 bits.
- Parity bit is selectable. So is the stop bit length (1 or 2 bits). The combination of the preceding selections constitutes the communication format and character length.
- In receiving, it is possible to detect framing errors, parity errors, overrun errors, and breaks.
- An internal or external clock can be selected as the SCI clock source.
  - When an internal clock is selected, the SCI operates using the clock supplied by the on-chip baud rate generator and can output a clock with a frequency 16 times the bit rate.
  - When an external clock is selected, the external clock input must have a frequency 16 times the bit rate. (The on-chip baud rate generator is not used.)

(2) Clock Synchronous Mode

- The transmission/reception format has a fixed 8-bit data length.
- In receiving, it is possible to detect overrun errors.
- An internal or external clock can be selected as the SCI clock source.
  - When an internal clock is selected, the SCI operates using the on-chip baud rate generator, and outputs a serial clock signal to external devices.
  - When an external clock is selected, the SCI operates on the input serial clock. The on-chip baud rate generator is not used.

17.3.3 Transmit Shift Register (SCTSR)

SCTSR transmits serial data. The SCIF loads transmit data from the transmit FIFO data register (SCFTDR) into SCTSR, then transmits the data serially from the TXD pin, LSB (bit 0) first. After transmitting one data byte, the SCIF automatically loads the next transmit data from SCFTDR into SCTSR and starts transmitting again.

The CPU cannot read or write to SCTSR directly.

Bit:	7	6	5	4	3	2	1	0
Initial value:	-	-	-	-	-	-	-	-
R/W:	-	-	-	-	-	-	-	-

17.3.4 Transmit FIFO Data Register (SCFTDR)

SCFTDR is a 16-byte FIFO register that stores data for serial transmission. When the SCIF detects that the transmit shift register (SCTSR) is empty, it moves transmit data written in the SCFTDR into SCTSR and starts serial transmission. Continuous serial transmission is performed until there is no transmit data left in SCFTDR. The CPU can write to SCFTDR at all times.

When SCFTDR is full of transmit data (16 bytes), no more data can be written. If writing of new data is attempted, the data is ignored.

SCFTDR is initialized to an undefined value by a power-on reset.

Bit:	7	6	5	4	3	2	1	0
Initial value:	-	-	-	-	-	-	-	-
R/W:	W	W	W	W	W	W	W	W

(5) Multi-Master/Multi-Slave (with This LSI Acting as Master)

Figure 18.7 shows a multi-master/multi-slave RSPI system configuration example when this LSI is used as a master. In the example of figure 18.7, the RSPI system is comprised of these two LSIs (master X, master Y) and two RSPI slaves (RSPI slave 1, RSPI slave 2).

The RSPCK and MOSI outputs of this LSI (master X, master Y) are connected to the RSPCK and MOSI inputs of RSPI slaves 1 and 2. The MISO outputs of RSPI slaves 1 and 2 are connected to the MISO inputs of this LSI (master X, master Y). Any generic port Y output from this LSI (master X) is connected to the SSL0 input of this LSI (master Y). Any generic port X output of this LSI (master Y) is connected to the SSL0 input of this LSI (master X). The SSL1 and SSL2 outputs of this LSI (master X, master Y) are connected to the SSL inputs of the RSPI slaves 1 and 2. In this configuration example, because the system can be comprised solely of SSL0 input, and SSL1 and SSL2 outputs for slave connections, the output SSL3 of this LSI is not required.

This LSI drives the RSPCK, MOSI, SSL1, and SSL2 signals when the SSL0 input level is 1. When the SSL0 input level is 0, this LSI detects a mode fault error, sets RSPCK, MOSI, SSL1, and SSL2 to Hi-Z, and releases the RSPI bus right to the other master. Of the RSPI slaves 1 and 2, the slave that receives 0 into the SSL input drives the MISO signal.

22.1.6 Port B Pull-Up MOS Control Register L (PBPCRL)

PBPCRL controls on/off of the input pull-up MOS of port B in bits.

- Port B Pull-Up MOS Control Register L (PBPCRL)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PB15 PCR	PB14 PCR	PB13 PCR	PB12 PCR	PB11 PCR	PB10 PCR	PB9 PCR	PB8 PCR	PB7 PCR	PB6 PCR	PB5 PCR	PB4 PCR	PB3 PCR	PB2 PCR	PB1 PCR	PB0 PCR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	PB15PCR	0	R/W	The corresponding input pull-up MOS turns on when one of these bits is set to 1.
14	PB14PCR	0	R/W	
13	PB13PCR	0	R/W	Reserved
12	PB12PCR	0	R/W	The corresponding input pull-up MOS turns on regardless of the setting value.
11	PB11PCR	0	R/W	The corresponding input pull-up MOS turns on when one of these bits is set to 1.
10	PB10PCR	0	R/W	
9	PB9PCR	0	R/W	
8	PB8PCR	0	R/W	
7	PB7PCR	0	R/W	
6	PB6PCR	0	R/W	
5	PB5PCR	0	R/W	
4	PB4PCR	0	R/W	
3	PB3PCR	0	R/W	
2	PB2PCR	0	R/W	
1	PB1PCR	0	R/W	
0	PB0PCR	0	R/W	

23.3.3 Port C Port Register L (PCPRL)

PCPRL is a 16-bit read-only register, which always returns the states of the pins regardless of the PFC setting. In this LSI, bits PC15PR to PC0PR correspond to pins PC15 to PC0, respectively (description of multiplexed functions are abbreviated here).

- Port C port register L (PCPRL)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PC15PR	PC14PR	PC13PR	PC12PR	PC11PR	PC10PR	PC9PR	PC8PR	PC7PR	PC6PR	PC5PR	PC4PR	PC3PR	PC2PR	PC1PR	PC0PR
Initial value:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	PC15PR	Pin state	R	The pin state is returned regardless of the PFC setting. These bits cannot be modified.
14	PC14PR	Pin state	R	
13	PC13PR	Pin state	R	
12	PC12PR	Pin state	R	
11	PC11PR	Pin state	R	
10	PC10PR	Pin state	R	
9	PC9PR	Pin state	R	
8	PC8PR	Pin state	R	
7	PC7PR	Pin state	R	
6	PC6PR	Pin state	R	
5	PC5PR	Pin state	R	
4	PC4PR	Pin state	R	
3	PC3PR	Pin state	R	
2	PC2PR	Pin state	R	
1	PC1PR	Pin state	R	
0	PC0PR	Pin state	R	

24.3.36 USB Trigger Register 0 (USBTRG0)

USBTRG0 is a write-only register that generates one-shot triggers to control the transmit/receive sequence for endpoint 0. The read value of this register is undefined. Do not write a value to this register using the read value, such as a bit manipulation instruction.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	EP0s RDFN	EP0o RDFN	EP0i PKTE
Initial value:	0	0	0	0	0	0	0	0
R/W:	-	-	-	-	-	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	—	Reserved The write value should always be 0.
2	EP0sRDFN	0	W	EP0s Read Complete Write 1 to this bit after EP0s command FIFO data has been read. Writing 1 to this bit enables transmission/reception of data in the following data stage. A NACK handshake is returned in response to transmit/receive requests from the host in the data stage until 1 is written to this bit.
1	EP0oRDFN	0	W	EP0o Read Complete Writing 1 to this bit after one packet of data has been read from the endpoint 0 receive FIFO buffer initializes the FIFO buffer, enabling the next packet to be received.
0	EP0iPKTE	0	W	EP0i Packet Enable After one packet of data has been written to the endpoint 0 transmit FIFO buffer, the transmit data is fixed by writing 1 to this bit.

Bit	Bit Name	Initial Value	R/W	Description
0	PRM	0	R/W	Promiscuous Mode Setting this bit to 1 enables all Ethernet frames to be received, that is, all receivable frames regardless of differences or enabled/disabled status (destination address, broadcast address, multicast bit, etc.). 0: The EtherC performs normal operation 1: The EtherC performs promiscuous mode operation

- The user boot MAT can be programmed or erased only in boot mode, USB boot mode, and programmer mode.
- In boot mode or USB boot mode, the user MAT, user boot MAT, and FLD data MAT are all erased immediately after the LSI is started. The user MAT, user boot MAT, and data MAT can then be programmed from the host via the SCI. The ROM can also be read after this entire area erasure.
- In user boot mode, a boot operation with a desired interface can be implemented through mode pin settings different from those in user program mode.

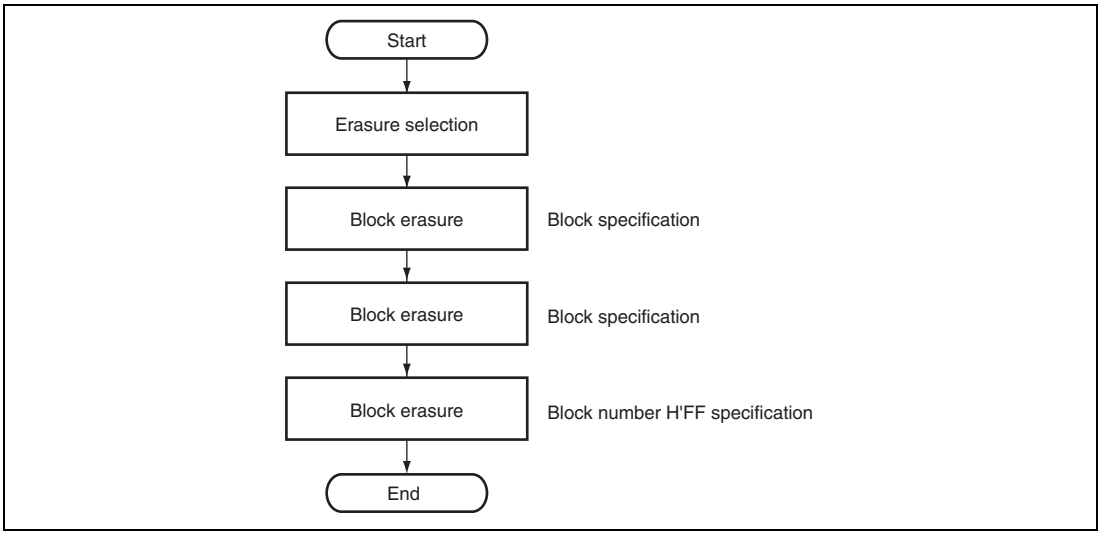

Figure 27.14 Procedure for ROM Erasure in Boot Mode

When H'71 is sent in the first cycle of an FCU command while the FRDMD bit is 0 (memory area read mode), the FCU accepts the lock bit read mode transition command (lock bit read 1). When a ROM program/erase address is read through the P bus after transition to the lock bit read mode, the FCU copies the lock bit of the erasure block corresponding to the accessed address into all bits in the read data. When H'71 is sent in the first cycle of the FCU command while the FRDMD bit is 1 (register read mode), the FCU waits for the second-cycle data (H'D0) of the lock bit read 2 command. When a ROM program/erase address is written to through the P bus in this state, the FCU copies the lock bit of the erasure block corresponding to the accessed address into the FLOCKST bit in FSTATR1.

There are two suspending modes to be initiated by the P/E suspend command; the suspension-priority mode and erasure-priority mode. For details of each mode, refer to section 27.6.4, Suspending Operation.

27.9.2 Software Protection

The software protection function disables ROM programming and erasure according to the control register settings or the lock bit settings in the user MAT. If an attempt is made to issue a programming or erasing command to the ROM against software protection, the FCU detects an error and enters command-locked state.

(1) Protection through FENTRYR

When the FENTRY0 bit is 0, the 1-Mbyte ROM (read addresses: H'00000000 to H'000FFFFF; program/erase addresses: H'80800000 to H'808FFFFF) is set to ROM read mode. In ROM read mode In ROM read mode, the FCU does not accept commands, so ROM programming and erasure are disabled. If an attempt is made to issue an FCU command in ROM read mode, the FCU detects an illegal command error and enters command-locked state (see section 27.9.3, Error Protection).

(2) Protection through Lock Bits

Each erasure block in the user MAT has a lock bit. When the FPROTCN bit in FPROTR is 0, the erasure block whose lock bit is set to 0 cannot be programmed or erased. To program or erase the erasure block whose lock bit is 0, set the FPROTCN bit to 1. If an attempt is made to issue a programming or erasing command against protection by lock bits, the FCU detects an programming/erasure error and enters command-locked state (see section 27.9.3, Error Protection).

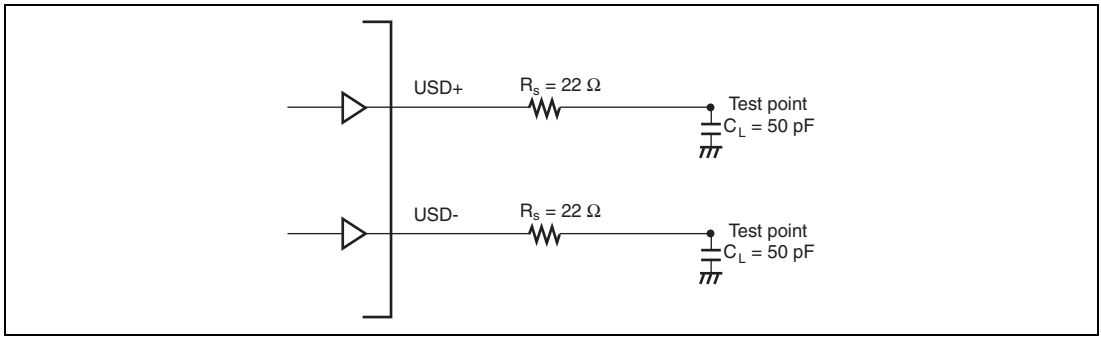

Figure 33.70 Test Load Circuit