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Details

Product Status	Not For New Designs
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, I ² C, SCI, SPI, USB
Peripherals	DMA, PWM, WDT
Number of I/O	112
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f72145bdbg-u1

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2.5.3 Arithmetic Operation Instructions

Table 2.13 Arithmetic Operation Instructions

Instruction		Instruction Code	Operation	Execution Cycles	T Bit	Compatibility		
						SH2E	SH4	SH-2A/ SH2A- FPU
ADD	Rm, Rn	0011nnnnnnmmn1100	$Rn + Rm \rightarrow Rn$	1	—	Yes	Yes	
ADD	#imm, Rn	0111nnnnnniiiiiii	$Rn + imm \rightarrow Rn$	1	—	Yes	Yes	
ADDC	Rm, Rn	0011nnnnnnmmn1110	$Rn + Rm + T \rightarrow Rn$, carry $\rightarrow T$	1	Carry	Yes	Yes	
ADDV	Rm, Rn	0011nnnnnnmmn1111	$Rn + Rm \rightarrow Rn$, overflow $\rightarrow T$	1	Over- flow	Yes	Yes	
CMP/EQ	#imm, R0	10001000iiiiiii	When $R0 = imm$, $1 \rightarrow T$ Otherwise, $0 \rightarrow T$	1	Com- parison result	Yes	Yes	
CMP/EQ	Rm, Rn	0011nnnnnnmm0000	When $Rn = Rm$, $1 \rightarrow T$ Otherwise, $0 \rightarrow T$	1	Com- parison result	Yes	Yes	
CMP/HS	Rm,Rn	0011nnnnnnmm0010	When $Rn \geq Rm$ (unsigned), $1 \rightarrow T$ Otherwise, $0 \rightarrow T$	1	Com- parison result	Yes	Yes	
CMP/GE	Rm, Rn	0011nnnnnnmm0011	When $Rn \geq Rm$ (signed), $1 \rightarrow T$ Otherwise, $0 \rightarrow T$	1	Com- parison result	Yes	Yes	
CMP/HI	Rm, Rn	0011nnnnnnmm0110	When $Rn > Rm$ (unsigned), $1 \rightarrow T$ Otherwise, $0 \rightarrow T$	1	Com- parison result	Yes	Yes	
CMP/GT	Rm,Rn	0011nnnnnnmm0111	When $Rn > Rm$ (signed), $1 \rightarrow T$ Otherwise, $0 \rightarrow T$	1	Com- parison result	Yes	Yes	
CMP/PL	Rn	0100nnnn00010101	When $Rn > 0$, $1 \rightarrow T$ Otherwise, $0 \rightarrow T$	1	Com- parison result	Yes	Yes	
CMP/PZ	Rn	0100nnnn00010001	When $Rn \geq 0$, $1 \rightarrow T$ Otherwise, $0 \rightarrow T$	1	Com- parison result	Yes	Yes	

- CS2WCR, CS3WCR

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	BAS	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	WR[3:0]				WM	-	-	-	-	-	-
Initial value:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	BAS	0	R/W	SRAM with Byte Selection Byte Access Select Specifies the \overline{WR}_{xx} and RD/\overline{WR} signal timing when the SRAM interface with byte selection is used. 0: Asserts the \overline{WR}_{xx} signal at the read timing and asserts the RD/\overline{WR} signal during the write access cycle. 1: Asserts the \overline{WR}_{xx} signal during the read access cycle and asserts the RD/\overline{WR} signal at the write timing.
19 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

- Setting for Area 3

Burst read/single write (burst length 1):

Data Bus Width	CAS Latency	Access Address	External Address Pin
16 bits	2	H'FFFC5440	H'0000440
	3	H'FFFC5460	H'0000460
32 bits	2	H'FFFC5880	H'0000880
	3	H'FFFC58C0	H'00008C0

Burst read/burst write (burst length 1):

Data Bus Width	CAS Latency	Access Address	External Address Pin
16 bits	2	H'FFFC5040	H'0000040
	3	H'FFFC5060	H'0000060
32 bits	2	H'FFFC5080	H'0000080
	3	H'FFFC50C0	H'00000C0

When a mode register write command is issued, the outputs of the external address pins are as follows.

When the data bus width of the area connected to SDRAM is 32 bits	A15 to A9	00000000 (burst read/burst write) 00000100 (burst read/single write)
	A8 to A6	010 (CAS latency 2), 011 (CAS latency 3)
	A5	0 (lap time = sequential)
	A4 to A2	000 (burst length 1)
When the data bus width of the area connected to SDRAM is 16 bits	A14 to A8	00000000 (burst read/burst write) 00000100 (burst read/single write)
	A7 to A5	010 (CAS latency 2), 011 (CAS latency 3)
	A4	0 (lap time = sequential)
	A3 to A1	000 (burst length 1)

Mode register setting timing is shown in figure 9.33. A PALL command (all bank pre-charge command) is firstly issued. A REF command (auto refresh command) is then issued 8 times. An MRS command (mode register write command) is finally issued. Idle cycles, of which number is specified by the WTRP1 and WTRP0 bits in CS3WCR, are inserted between the PALL and the first REF. Idle cycles, of which number is specified by the WTRC1 and WTRC0 bits in CS3WCR,

Table 11.10 TPSC1 and TPSC0 (Channel 5)

Channel	Bit 1 TPSC1	Bit 0 TPSC0	Description
5	0	0	Internal clock: counts on P ϕ /1
		1	Internal clock: counts on P ϕ /4
	1	0	Internal clock: counts on P ϕ /16
		1	Internal clock: counts on P ϕ /64

Note: Bits 7 to 2 are reserved in channel 5. These bits are always read as 0. The write value should always be 0.

11.3.2 Timer Mode Register (TMDR)

The TMDR registers are 8-bit readable/writable registers that are used to set the operating mode of each channel. The MTU2 has five TMDR registers, one each for channels 0 to 4. TMDR register settings should be changed only when TCNT operation is stopped.

Bit:	7	6	5	4	3	2	1	0
	-	BFE	BFB	BFA	MD[3:0]			
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	BFE	0	R/W	Buffer Operation E Specifies whether TGRE_0 and TGRF_0 are to operate in the normal way or to be used together for buffer operation. TGRF compare match is generated when TGRF is used as the buffer register. In channels 1 to 4, this bit is reserved. It is always read as 0 and the write value should always be 0. 0: TGRE_0 and TGRF_0 operate normally 1: TGRE_0 and TGRF_0 used together for buffer operation

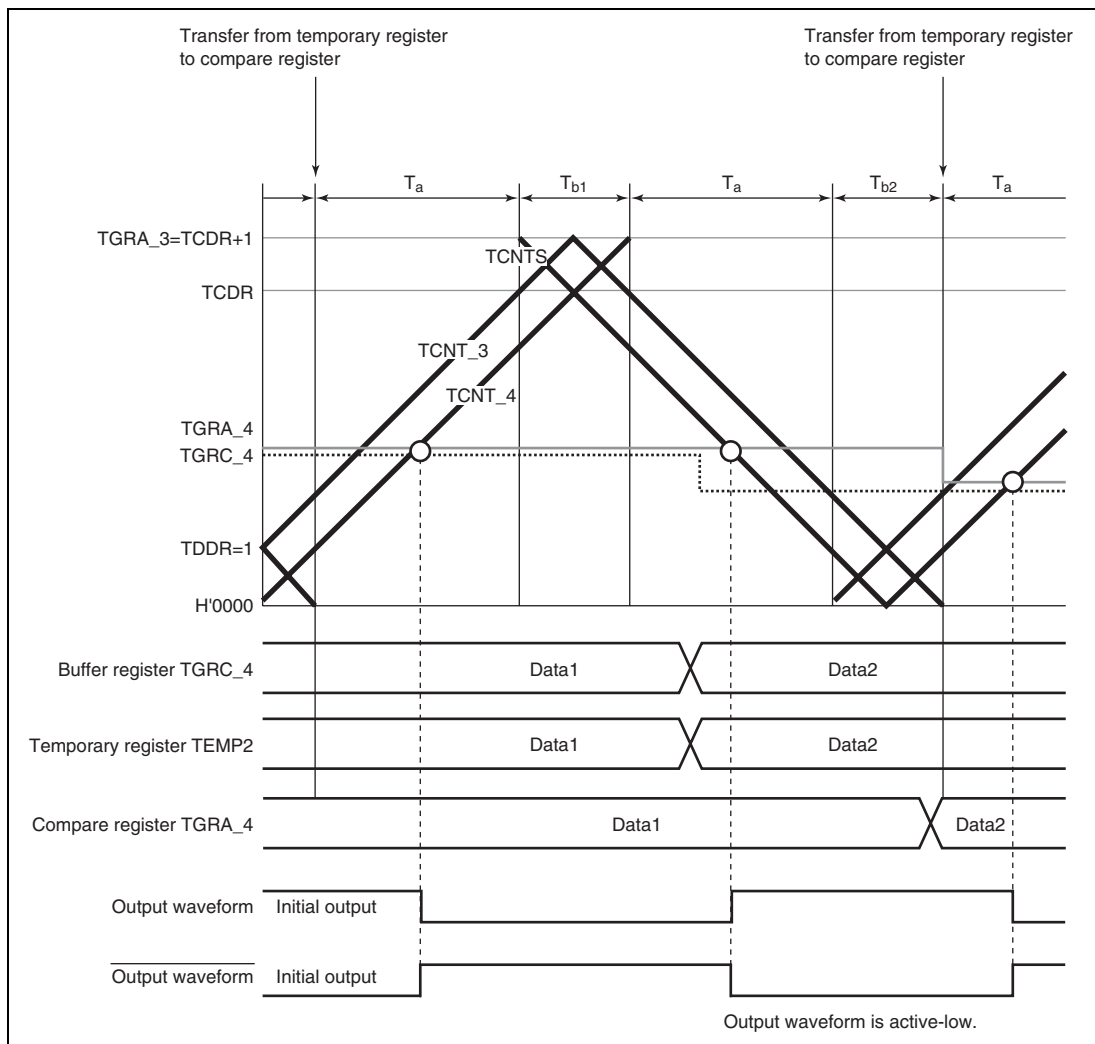


Figure 11.41 Example of Operation without Dead Time

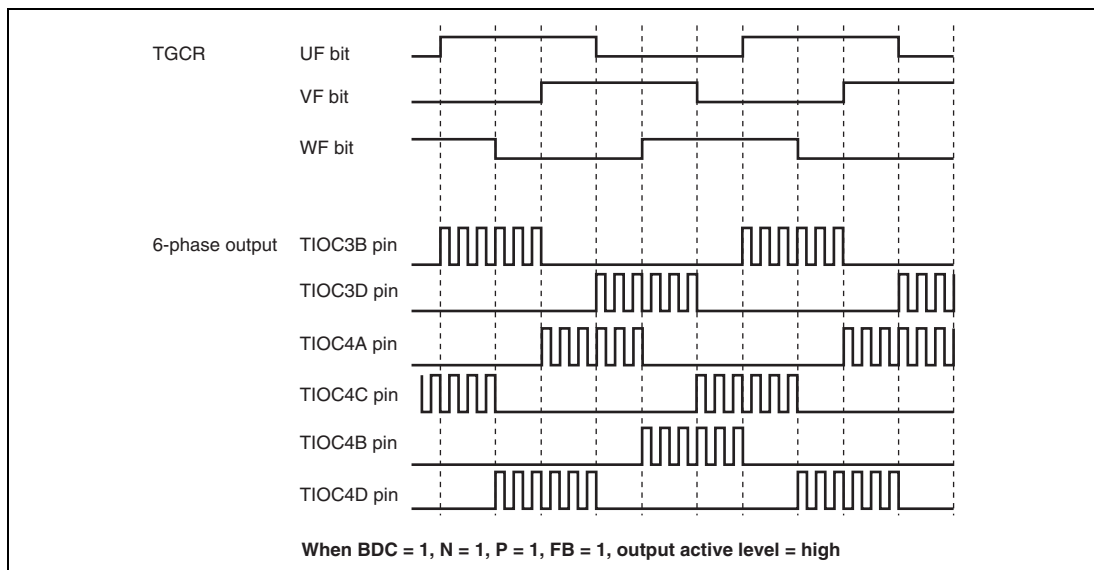


Figure 11.72 Example of Output Phase Switching by Means of UF, VF, WF Bit Settings (2)

(r) A/D Converter Start Request Setting

In complementary PWM mode, an A/D converter start request can be issued using a TGRA_3 compare-match, TCNT_4 underflow (trough), or compare-match on a channel other than channels 3 and 4.

When start requests using a TGRA_3 compare-match are specified, A/D conversion can be started at the crest of the TCNT_3 count.

A/D converter start requests can be set by setting the TTGE bit to 1 in the timer interrupt enable register (TIER). To issue an A/D converter start request at a TCNT_4 underflow (trough), set the TTGE2 bit in TIER_4 to 1.

11.8 MTU2 Output Pin Initialization

11.8.1 Operating Modes

The MTU2 has the following six operating modes. Waveform output is possible in all of these modes.

- Normal mode (channels 0 to 4)
- PWM mode 1 (channels 0 to 4)
- PWM mode 2 (channels 0 to 2)
- Phase counting modes 1 to 4 (channels 1 and 2)
- Complementary PWM mode (channels 3 and 4)
- Reset-synchronized PWM mode (channels 3 and 4)

The MTU2 output pin initialization method for each of these modes is described in this section.

11.8.2 Reset Start Operation

The MTU2 output pins (TIOC*) are initialized low by a reset and in standby mode. Since MTU2 pin function selection is performed by the pin function controller (PFC), when the PFC is set, the MTU2 pin states at that point are output to the ports. When MTU2 output is selected by the PFC immediately after a reset, the MTU2 output initial level, low, is output directly at the port. When the active level is low, the system will operate at this point, and therefore the PFC setting should be made after initialization of the MTU2 output pins is completed.

Note: Channel number and port notation are substituted for *.

Table 16.5 Bit Rates and SCBRR Settings in Asynchronous Mode (2)

Bit Rate (bits/s)	P _Φ (MHz)																	
	22			24			26			28			30			32		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	97	-0.35	3	106	-0.44	3	114	0.36	3	123	0.23	3	132	0.13	3	141	0.03
150	3	71	-0.54	3	77	0.16	3	84	-0.43	3	90	0.16	3	97	-0.35	3	103	0.16
300	2	142	0.16	2	155	0.16	2	168	0.16	2	181	0.16	2	194	0.16	2	207	0.16
600	2	71	-0.54	2	77	0.16	2	84	-0.43	2	90	0.16	2	97	-0.35	2	103	0.16
1200	1	142	0.16	1	155	0.16	1	168	0.16	1	181	0.16	1	194	0.16	1	207	0.16
2400	1	71	-0.54	1	77	0.16	1	84	-0.43	1	90	0.16	1	97	-0.35	1	103	0.16
4800	0	142	0.16	0	155	0.16	0	168	0.16	0	181	0.16	0	194	0.16	0	207	0.16
9600	0	71	-0.54	0	77	0.16	0	84	-0.43	0	90	0.16	0	97	-0.35	0	103	0.16
14400	0	47	-0.54	0	51	0.16	0	55	0.76	0	60	-0.39	0	64	0.16	0	68	0.64
19200	0	35	-0.54	0	38	0.16	0	41	0.76	0	45	-0.93	0	48	-0.35	0	51	0.16
28800	0	23	-0.54	0	25	0.16	0	27	0.76	0	29	1.27	0	32	-1.36	0	34	-0.79
31250	0	21	0.00	0	23	0.00	0	25	0.00	0	27	0.00	0	29	0.00	0	31	0.00
38400	0	17	-0.54	0	19	-2.34	0	20	0.76	0	22	-0.93	0	23	1.73	0	25	0.16

18.4.3 RSPI System Configuration Example

(1) Single Master/Single Slave (with This LSI Acting as Master)

Figure 18.2 shows a single-master/single-slave RSPI system configuration example when this LSI is used as a master. In the single-master/single-slave configuration, the SSL0 to SSL3 outputs of this LSI (master) are not used. The SSL input of the RSPI slave is fixed to 0, and the RSPI slave is always maintained in a select state. In the transfer format corresponding to the case where the CPHA bit in the RSPI control register (SPCR) is 0, there are slave devices for which the SSL signal cannot be fixed to the active level. In situations where the SSL signal cannot be fixed, the SSL output of this LSI should be connected to the SSL input of the slave device.

This LSI (master) always drives the RSPCK and MOSI signals. The RSPI slave always drives the MISO signal.

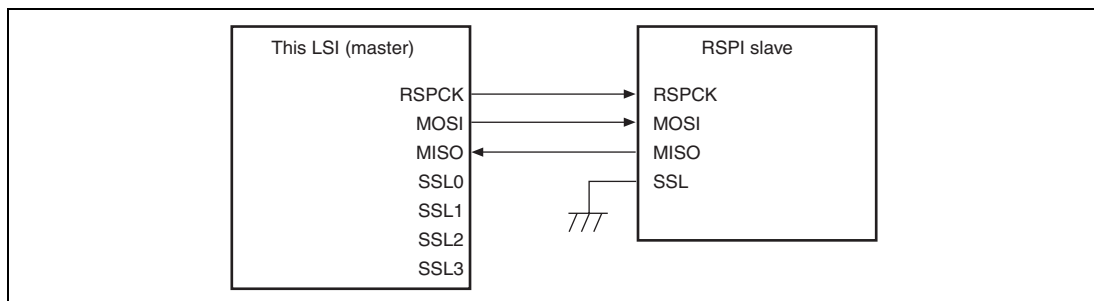


Figure 18.2 Single-Master/Single-Slave Configuration Example (This LSI = Master)

21.4.3 Message Transmission Sequence

- Message Transmission Request

The following sequence is an example to transmit a CAN frame onto the bus. As described in the previous register section, please note that IRR8 is set when one of the TXACK or ABACK bits is set, meaning one of the Mailboxes has completed its transmission or transmission abortion and is now ready to be updated for the next transmission, whereas, the GSR2 means that there is currently no transmission request made (No TXPR flags set).

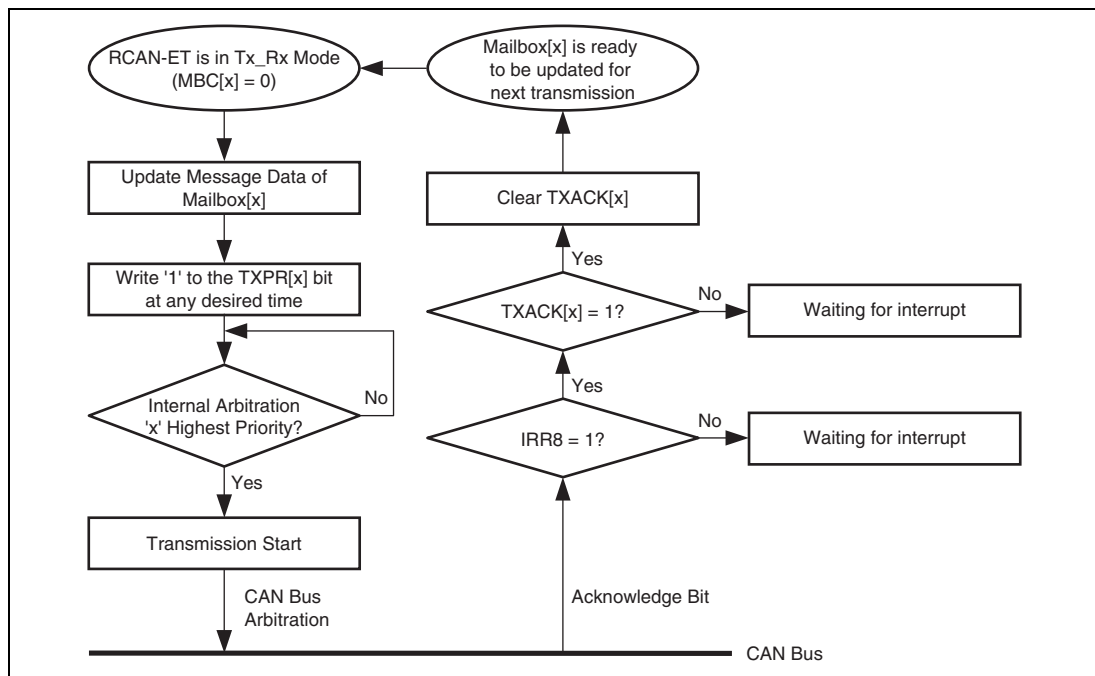


Figure 21.10 Transmission Request

- Port D Control Register L2 (PDCRL2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	PD7MD[2:0]			-	PD6MD[2:0]			-	PD5MD[2:0]			-	PD4MD[2:0]		
Initial value:	0	0	0	0*	0	0	0	0*	0	0	0	0*	0	0	0	0*
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Note: * The initial value is 1 during the on-chip ROM disabled external extension mode.

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	PD7MD[2:0]	000*	R/W	PD7 Mode Select the function of the PD7/D7/TIC5WS pin. 000: PD7 I/O (port) 001: D7 I/O (BSC) 010: Setting prohibited 011: Setting prohibited 100: Setting prohibited 101: TIC5WS input (MTU2S) 110: Setting prohibited 111: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	PD6MD[2:0]	000*	R/W	PD6 Mode Select the function of the PD6/D6/TIC5VS pin. 000: PD6 I/O (port) 001: D6 I/O (BSC) 010: Setting prohibited 011: Setting prohibited 100: Setting prohibited 101: TIC5VS input (MTU2S) 110: Setting prohibited 111: Setting prohibited

24.3.18 USBEP0s Data Register (USBEPDR0s)

USBEPDR0s is an 8-byte FIFO buffer specifically for receiving endpoint 0 setup commands. USBEPDR0s receives only setup commands requiring processing on the application side. When a command that this module automatically processes is received, it is not stored. When command data is stored normally, the SETUPTS bit in the USB interrupt flag register 1 (USBIFR1) is set.

As a setup command must be received without fail, if data is left in this buffer, it will be overwritten with new data. If reception of the next command is started while the current command is being read, command reception has priority and data read by the application is forcibly disabled. Therefore the read data is invalid.

Bit:	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0
Initial value:	-	-	-	-	-	-	-	-
R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	D7 to D0	—	R	Register for storing the setup command on control OUT transfer

25.4.3 MII Frame Timing

Each MII frame timing is shown in figure 25.4.

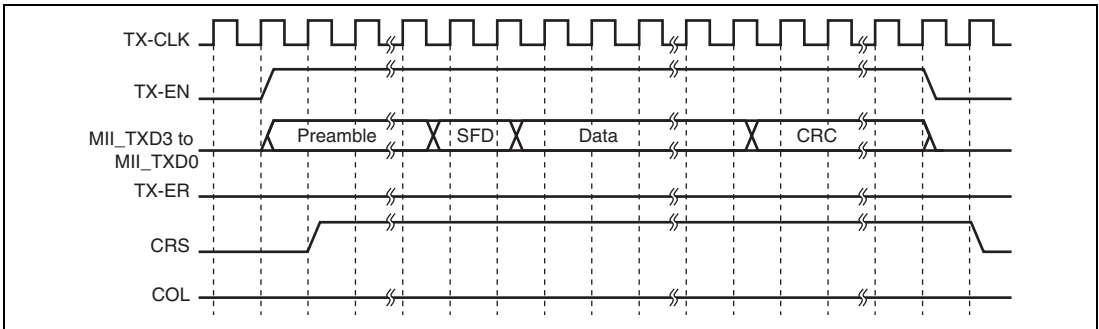


Figure 25.4 (1) MII Frame Transmit Timing (Normal Transmission)

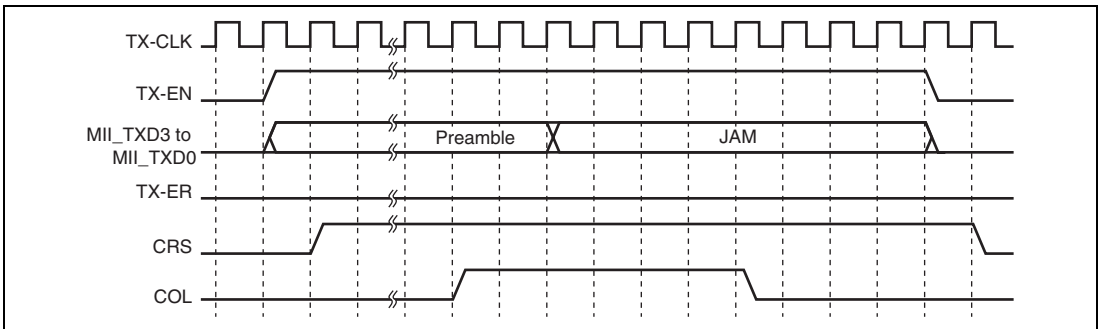


Figure 25.4 (2) MII Frame Transmit Timing (Collision)

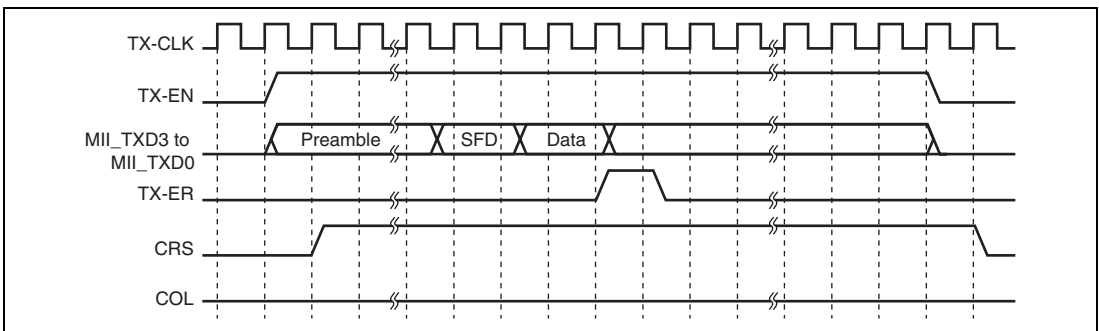


Figure 25.4 (3) MII Frame Transmit Timing (Transmit Error)

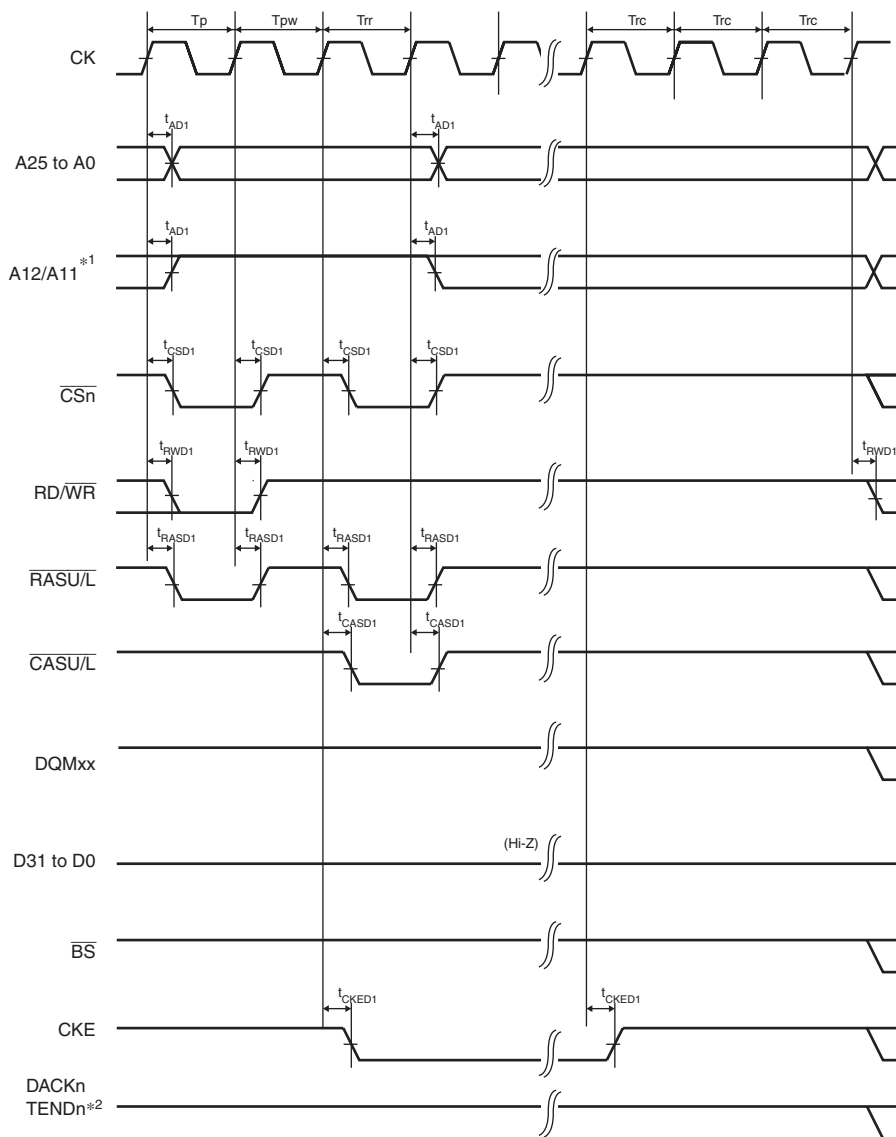
Bit	Bit Name	Initial Value	R/W	Description
21	TC	0	R/W	<p>Frame Transmit Completed</p> <p>Indicates that all the data specified by the transmit descriptor has been transmitted from the EtherC. This bit is set to 1, assuming the completion of transmission, when transmission of one frame is completed in the single-frame/single-buffer processing or when the last data of a frame has been transmitted and the transmit descriptor active bit (TACT) of the next descriptor is not set in the multi-buffer frame processing. After frame transmission, the E-DMAC writes the transfer status back to the relevant descriptor.</p> <p>0: Transfer is not completed or no transfer directive is given</p> <p>1: Transfer is completed</p>
20	TDE	0	R/W	<p>Transmit Descriptor Empty</p> <p>Indicates that the transmit descriptor active bit (TACT) in a transmit descriptor is not set when it is read by the E-DMAC if the previous descriptor does not represent the end of a frame in the multi-buffer frame processing. As a result, an incomplete frame may be sent.</p> <p>0: Transmit descriptor active bit TACT = 1 detected</p> <p>1: Transmit descriptor active bit TACT = 0 detected</p> <p>When transmit descriptor empty (TDE = 1) occurs, execute a software reset and initiate transmission. In this case, transmission starts from the address that is stored in the transmit descriptor list start address register (TDLAR).</p>
19	TFUF	0	R/W	<p>Transmit FIFO Underflow</p> <p>Indicates that an underflow has occurred in the transmit FIFO during frame transmission. Incomplete data is sent onto the line.</p> <p>0: Underflow has not occurred</p> <p>1: Underflow has occurred</p>

Bit	Bit Name	Initial Value	R/W	Description
7	FENTRYD	0	R/W	<p>FLD P/E Mode Entry</p> <p>This bit specifies the P/E mode for the FLD.</p> <p>00: The FLD is in read mode</p> <p>11: The FLD is in P/E mode</p> <p>[Write enabling conditions]</p> <p>When the following conditions are all satisfied:</p> <ul style="list-style-type: none"> • The LSI is in on-chip ROM enabled mode. • The FRDY bit in FSTATR0 is 1. • H'AA is written to FEKEY in word access. <p>[Setting condition]</p> <ul style="list-style-type: none"> • 1 is written to FENTRYD while the write enabling conditions are satisfied and FENTRYR is H'0000. <p>[Clearing conditions]</p> <ul style="list-style-type: none"> • This register is written to in byte access. • A value other than H'AA is written to FEKEY in word access. • 0 is written to FENTRYD while the write enabling conditions are satisfied. • FENTRYR is written to while FENTRYR is not H'0000 and the write enabling conditions are satisfied.
6 to 1	—	All 0	R	<p>Reserved</p> <p>The write value should always be 0; otherwise normal operation cannot be guaranteed.</p>
0	FENTRY0	0	R/W	<p>ROM P/E Mode Entry 1, 0</p> <p>Refer to section 27, Flash Memory (ROM).</p>

Note: * Write data is not retained.

Module Name	Register	Power-on Reset	Manual Reset	Software Standby	Module Standby	Sleep
MTU2	TSR_5	Initialized	Retained	Retained	Initialized	Retained
	TSTR_5	Initialized	Retained	Retained	Initialized	Retained
	TCNTU_5	Initialized	Retained	Retained	Initialized	Retained
	TCNTV_5	Initialized	Retained	Retained	Initialized	Retained
	TCNTW_5	Initialized	Retained	Retained	Initialized	Retained
	TGRU_5	Initialized	Retained	Retained	Initialized	Retained
	TGRV_5	Initialized	Retained	Retained	Initialized	Retained
	TGRW_5	Initialized	Retained	Retained	Initialized	Retained
	TCNTCMPCLR	Initialized	Retained	Retained	Initialized	Retained
	TSTR	Initialized	Retained	Retained	Initialized	Retained
	TSYR	Initialized	Retained	Retained	Initialized	Retained
	TCSYSTR	Initialized	Retained	Retained	Initialized	Retained
	TRWER	Initialized	Retained	Retained	Initialized	Retained
	TOER	Initialized	Retained	Retained	Initialized	Retained
	TOCR1	Initialized	Retained	Retained	Initialized	Retained
	TOCR2	Initialized	Retained	Retained	Initialized	Retained
	TGCR	Initialized	Retained	Retained	Initialized	Retained
	TCDR	Initialized	Retained	Retained	Initialized	Retained
	TDDR	Initialized	Retained	Retained	Initialized	Retained
	TCNTS	Initialized	Retained	Retained	Initialized	Retained
	TCBR	Initialized	Retained	Retained	Initialized	Retained
	TITCR	Initialized	Retained	Retained	Initialized	Retained
	TITCNT	Initialized	Retained	Retained	Initialized	Retained
	TBTER	Initialized	Retained	Retained	Initialized	Retained
	TDER	Initialized	Retained	Retained	Initialized	Retained
	TWCR	Initialized	Retained	Retained	Initialized	Retained
	TOLBR	Initialized	Retained	Retained	Initialized	Retained

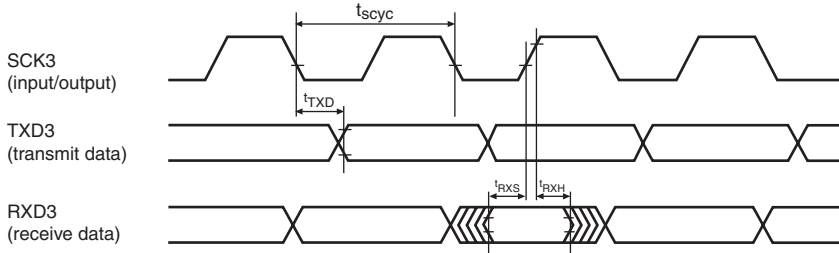
Module Name	Register	Power-on Reset	Manual Reset	Software Standby	Module Standby	Sleep
MTU2S	TCR_3S	Initialized	Retained	Retained	Initialized	Retained
	TMDR_3S	Initialized	Retained	Retained	Initialized	Retained
	TIORH_3S	Initialized	Retained	Retained	Initialized	Retained
	TIORL_3S	Initialized	Retained	Retained	Initialized	Retained
	TIER_3S	Initialized	Retained	Retained	Initialized	Retained
	TSR_3S	Initialized	Retained	Retained	Initialized	Retained
	TCNT_3S	Initialized	Retained	Retained	Initialized	Retained
	TGRA_3S	Initialized	Retained	Retained	Initialized	Retained
	TGRB_3S	Initialized	Retained	Retained	Initialized	Retained
	TGRC_3S	Initialized	Retained	Retained	Initialized	Retained
	TGRD_3S	Initialized	Retained	Retained	Initialized	Retained
	TBTM_3S	Initialized	Retained	Retained	Initialized	Retained
	TCR_4S	Initialized	Retained	Retained	Initialized	Retained
	TMDR_4S	Initialized	Retained	Retained	Initialized	Retained
	TIORH_4S	Initialized	Retained	Retained	Initialized	Retained
	TIORL_4S	Initialized	Retained	Retained	Initialized	Retained
	TIER_4S	Initialized	Retained	Retained	Initialized	Retained
	TSR_4S	Initialized	Retained	Retained	Initialized	Retained
	TCNT_4S	Initialized	Retained	Retained	Initialized	Retained
	TGRA_4S	Initialized	Retained	Retained	Initialized	Retained
	TGRB_4S	Initialized	Retained	Retained	Initialized	Retained
	TGRC_4S	Initialized	Retained	Retained	Initialized	Retained
	TGRD_4S	Initialized	Retained	Retained	Initialized	Retained
	TBTM_4S	Initialized	Retained	Retained	Initialized	Retained
	TADCRS	Initialized	Retained	Retained	Initialized	Retained
	TADCORA_4S	Initialized	Retained	Retained	Initialized	Retained
	TADCORB_4S	Initialized	Retained	Retained	Initialized	Retained
	TADCOBRA_4S	Initialized	Retained	Retained	Initialized	Retained
	TADCOBRB_4S	Initialized	Retained	Retained	Initialized	Retained



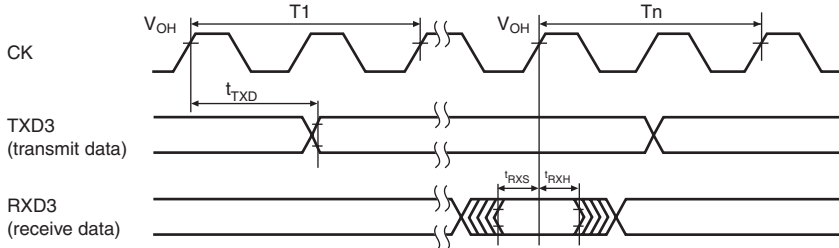
- Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

**Figure 33.33 Synchronous DRAM Self-Refreshing Timing
(WTRP = 1 Cycle)**

SCI I/O timing (clocked synchronous mode)



SCI I/O timing (asynchronous mode)

**Figure 33.48 SCIF Input/Output Timing**