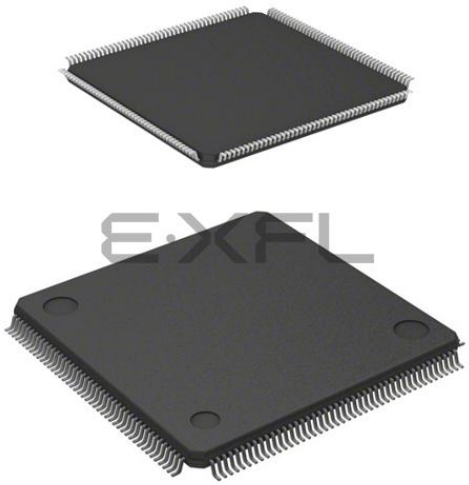
Renesas Electronics America Inc - R5F72145HDFA#V1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, Ethernet, I²C, SCI, SPI, USB
Peripherals	DMA, PWM, WDT
Number of I/O	112
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f72145hdfa-v1

Items	Specification
FPU (SH7216 Group only)	• On-chip floating-point coprocessor • Supports single-precision (32 bits) and double-precision (64 bits) • Supports IEEE 754-compliant data types and exceptions • Rounding mode: Round to Nearest and Round to Zero • Handling of denormalize numbers: Truncation to Zero • Floating-point registers Sixteen 32-bit floating-point registers (single-precision x 16 words or double-precision x 8 words) Two 32-bit floating-point system registers • Supports FMAC (multiply and accumulate) instruction • Supports FDIV (division) and FSQRT (square root) instructions • Supports FLDI0/FLDI1 (load constant 0/1) instructions • Instruction execution times Latency (FMAC/FADD/FSUB/FMUL): 3 cycles (single-precision), 8 cycles (double-precision) Pitch (FMAC/FADD/FSUB/FMUL): 1 cycle (single-precision), 6 cycles (double-precision) Note: FMAC is supported for single-precision only. • Five-stage pipeline
Operating modes	• Operating modes Extended ROM enabled mode Single-chip mode • Processing states Program execution state Exception handling state Bus mastership release state • Power-down modes Sleep mode Software standby mode Module standby mode

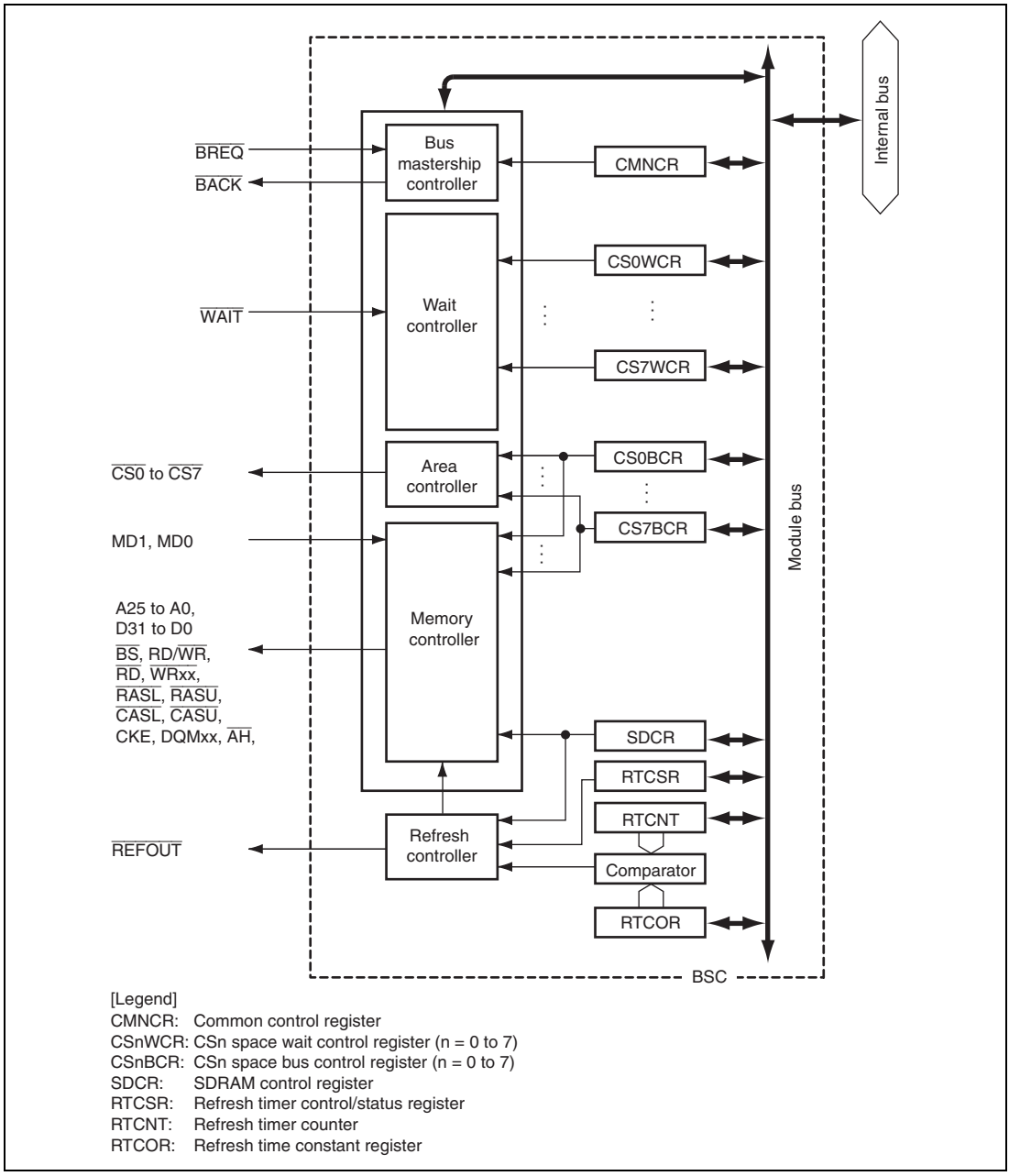
Instruction		Instruction Code	Operation	Execution Cycles	T Bit	Compatibility SH2E	SH4	SH-2A/ SH2A-FPU
BT/S	label	10001101dddddddd	Delayed branch When T = 1, disp × 2 + PC → PC, When T = 0, nop	2/1*	—	Yes	Yes	
BRA	label	1010dddddddddddd	Delayed branch, disp × 2 + PC → PC	2	—	Yes	Yes	
BRAF	Rm	0000mmmm00100011	Delayed branch, Rm + PC → PC	2	—	Yes	Yes	
BSR	label	1011dddddddddddd	Delayed branch, PC → PR, disp × 2 + PC → PC	2	—	Yes	Yes	
BSRF	Rm	0000mmmm00000011	Delayed branch, PC → PR, Rm + PC → PC	2	—	Yes	Yes	
JMP	@Rm	0100mmmm00101011	Delayed branch, Rm → PC	2	—	Yes	Yes	
JSR	@Rm	0100mmmm00001011	Delayed branch, PC → PR, Rm → PC	2	—	Yes	Yes	
JSR/N	@Rm	0100mmmm01001011	PC-2 → PR, Rm → PC	3	—			Yes
JSR/N	@@(disp8, TBR)	10000011dddddddd	PC-2 → PR, (disp × 4 + TBR) → PC	5	—			Yes
RTS		0000000000001011	Delayed branch, PR → PC	2	—	Yes	Yes	
RTS/N		0000000001101011	PR → PC	3	—			Yes
RTV/N	Rm	0000mmmm01111011	Rm → R0, PR → PC	3	—			Yes

Note: * One cycle when the program does not branch.

Transfer Mode	1st Transfer CHNE	CHNS	RCHNE	DISEL	Transfer Counter*1	2nd Transfer CHNE	CHNS	RCHNE	DISEL	Transfer Counter*1	DTC Transfer
Block	0	—	—	0	Not 0	—	—	—	—	—	Ends at 1st transfer
	0	—	—	0	0	—	—	—	—	—	Ends at 1st transfer Interrupt request to CPU
	0	—	—	1	—	—	—	—	—	—	
	1	0	—	—	—	0	—	—	0	Not 0	Ends at 2nd transfer
						0	—	—	0	0	Ends at 2nd transfer Interrupt request to CPU
						0	—	—	1	—	
	1	1	—	0	—	—	—	—	—	—	Ends at 1st transfer
	1	1	—	1	Not 0	—	—	—	—	—	Ends at 1st transfer Interrupt request to CPU
	1	1	—	1	0	0	—	—	0	Not 0	Ends at 2nd transfer
						0	—	—	0	0	Ends at 2nd transfer Interrupt request to CPU
						0	—	—	1	—	

Notes: 1. CRA in normal mode transfer, CRAL in repeat transfer mode, or CRB in block transfer mode

2. When the contents of the CRAH is written to the CRAL



[Legend]
CMNCR: Common control register
CSnWCR: CSn space wait control register (n = 0 to 7)
CSnBCR: CSn space bus control register (n = 0 to 7)
SDCR: SDRAM control register
RTCSR: Refresh timer control/status register
RTCNT: Refresh timer counter
RTCOR: Refresh time constant register

Figure 9.1 Block Diagram of BSC

Bit	Bit Name	Initial Value	R/W	Description
1	SCC	0	R/(W)	Synchronous Clearing Control Specifies whether to clear TCNT_3 and TCNT_4 in the MTU2S when synchronous counter clearing between the MTU2 and MTU2S occurs in complementary PWM mode. When using this control, place the MTU2S in complementary PWM mode. When modifying the SCC bit while the counters are operating, do not modify the CCE or WRE bits. Counter clearing synchronized with the MTU2 is disabled by the SCC bit setting only when synchronous clearing occurs outside the Tb interval at the trough. When synchronous clearing occurs in the Tb interval at the trough including the period immediately after TCNT_3 and TCNT_4 start operation, TCNT_3 and TCNT_4 in the MTU2S are cleared. For the Tb interval at the trough in complementary PWM mode, see figure 11.40. In the MTU2, this bit is reserved. It is always read as 0 and the write value should always be 0. 0: Enables clearing of TCNT_3 and TCNT_4 in the MTU2S by MTU2-MTU2S synchronous clearing operation 1: Disables clearing of TCNT_3 and TCNT_4 in the MTU2S by MTU2-MTU2S synchronous clearing operation [Setting condition] • When 1 is written to SCC after reading SCC = 0

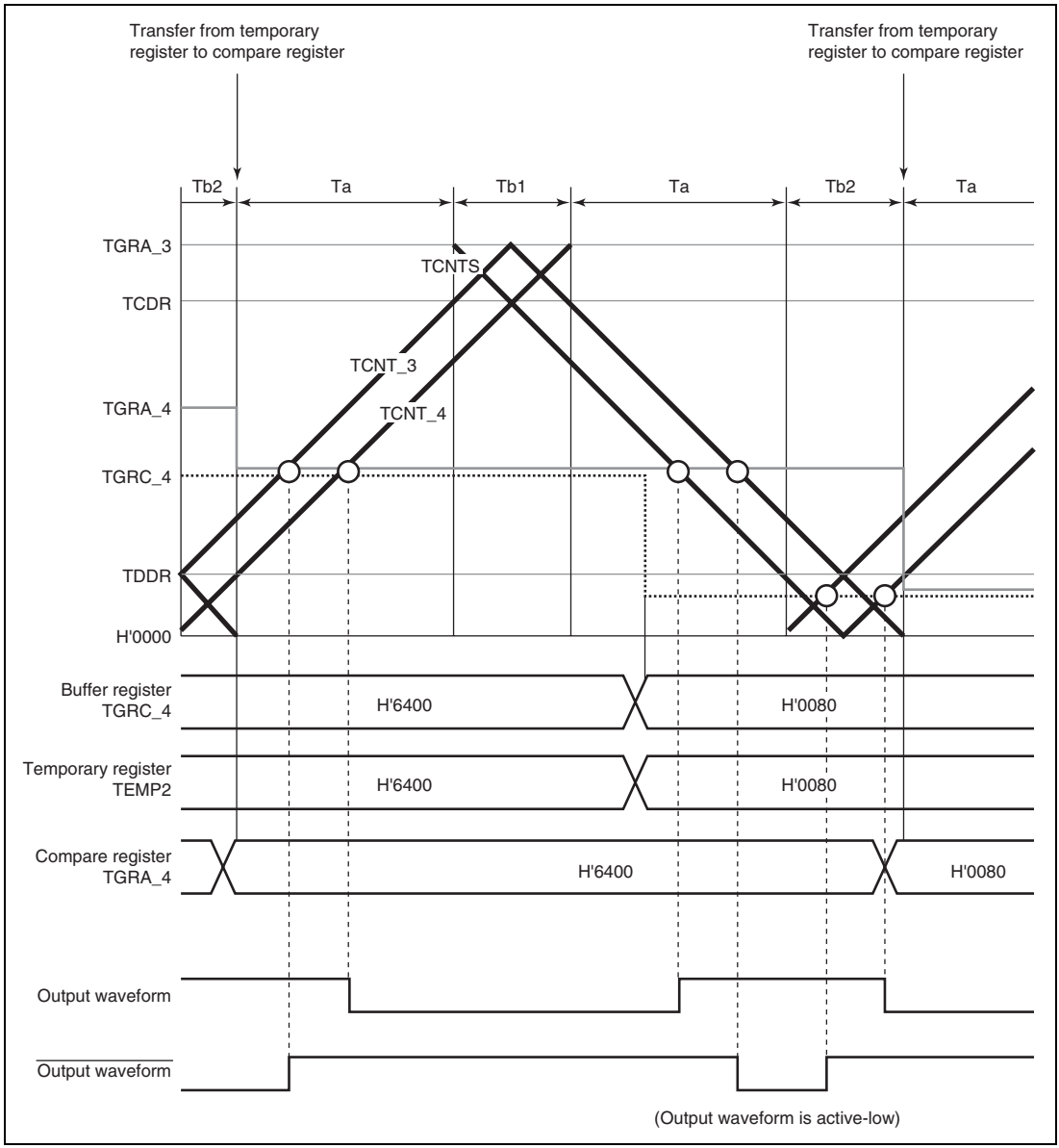


Figure 11.40 Example of Complementary PWM Mode Operation

(q) Example of AC Synchronous Motor (Brushless DC Motor) Drive Waveform Output

In complementary PWM mode, a brushless DC motor can easily be controlled using the timer gate control register (TGCR). Figures 11.69 to 11.72 show examples of brushless DC motor drive waveforms created using TGCR.

When output phase switching for a 3-phase brushless DC motor is performed by means of external signals detected with a Hall element, etc., clear the FB bit in TGCR to 0. In this case, the external signals indicating the polarity position are input to channel 0 timer input pins TIOC0A, TIOC0B, and TIOC0C (set with PFC). When an edge is detected at pin TIOC0A, TIOC0B, or TIOC0C, the output on/off state is switched automatically.

When the FB bit is 1, the output on/off state is switched when the UF, VF, or WF bit in TGCR is cleared to 0 or set to 1.

The drive waveforms are output from the complementary PWM mode 6-phase output pins. With this 6-phase output, in the case of on output, it is possible to use complementary PWM mode output and perform chopping output by setting the N bit or P bit to 1. When the N bit or P bit is 0, level output is selected.

The 6-phase output active level (on output level) can be set with the OLSN and OLSP bits in the timer output control register (TOCR) regardless of the setting of the N and P bits.

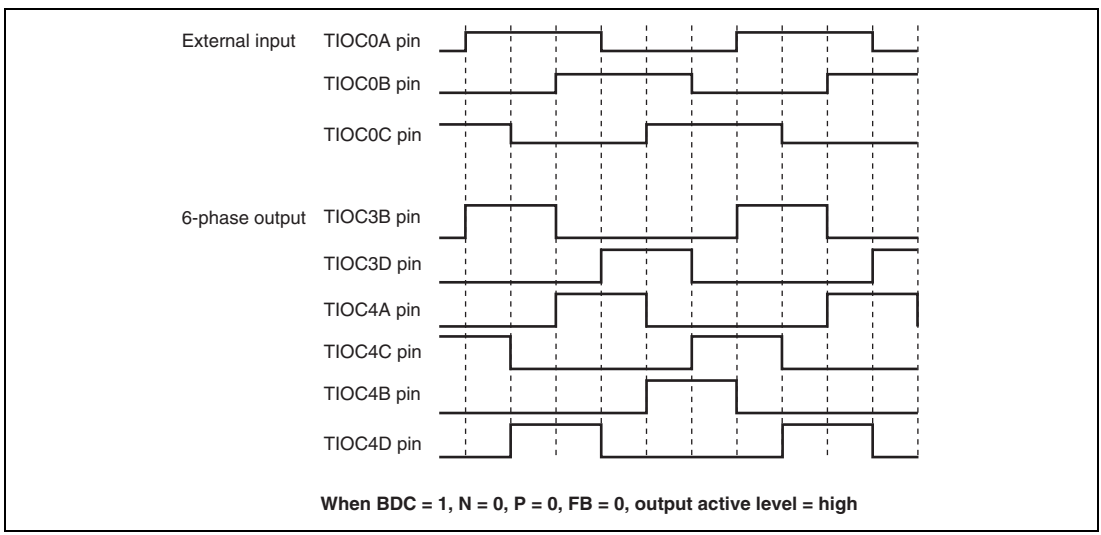


Figure 11.69 Example of Output Phase Switching by External Input (1)

Bit	Bit Name	Initial Value	R/W	Description
2	SPOM	0	R/W	RSPI Output Pin Mode Sets the RSPI output pins to CMOS output/open drain output. 0: CMOS output 1: Open-drain output
1	—	0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
0	SPLP	0	R/W	RSPI Loopback When the SPLP bit is set to 1, the RSPI shuts off the path between the MISO pin and the shift register, and between the MOSI pin and the shift register, and connects (reverses) the input path and the output path for the shift register (loopback mode). 0: Normal mode 1: Loopback mode

18.3.4 RSPI Status Register (SPSR)

SPSR indicates the operating status of the RSPI. SPSR can be read by the CPU. Writing 1 to the SPRF, SPTEF, MODF, and OVRF bits cannot be performed by the CPU. These bits can be cleared to 0 after they are read as 1.

Bit:	7	6	5	4	3	2	1	0
	SPRF	–	SPTEF	–	–	MODF	MIDLE	OVRF
Initial value:	0	0	1	0	0	0	0	0
R/W:	R/(W)*	R	R/(W)*	R	R	R/(W)*	R	R/(W)*

Note: * Only 0 can be written to this bit after reading it as 1 to clear the flag.

18.4.11 Error Processing

Figures 18.30 and 18.31 show error processing. The RSPI can recover from an error which may occur in master or slave mode, using the following error processing.

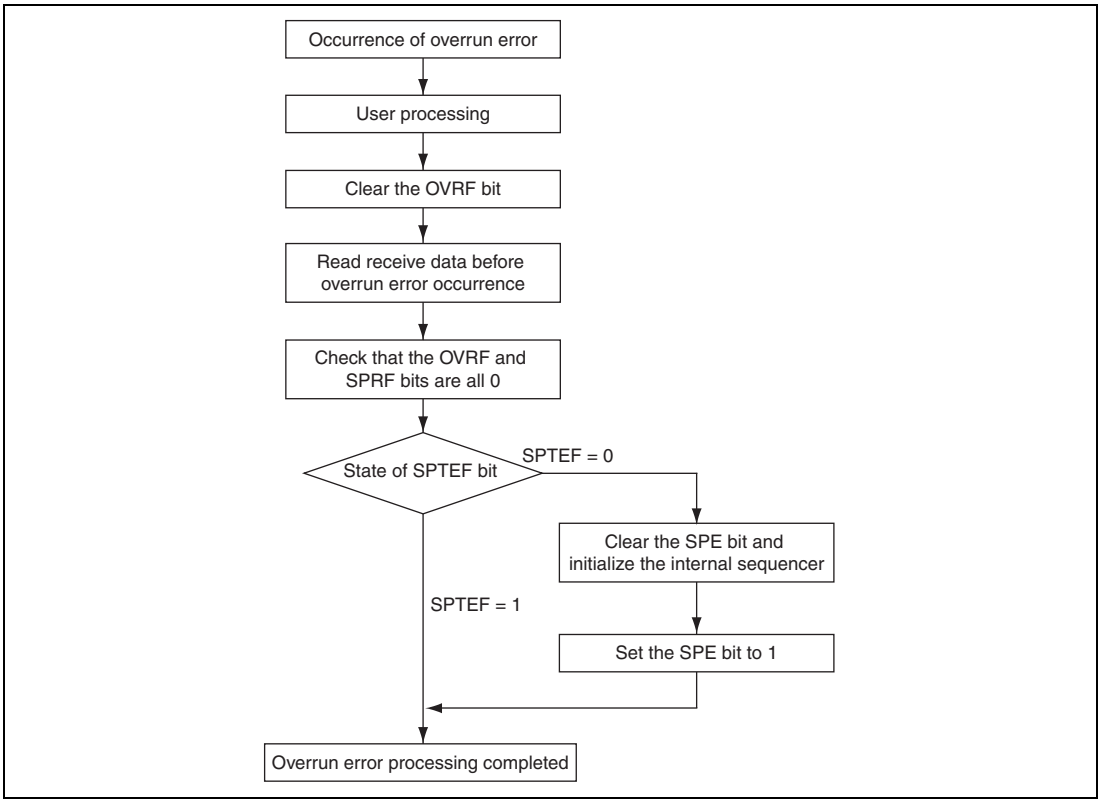


Figure 18.30 Error Processing (Overrun Error)

Bit	Bit Name	Initial Value	R/W	Description
5	SDAO	1	R/W	SDA Output Value Control This bit is used with SDAOP when modifying output level of SDA. This bit should not be manipulated during transfer. 0: When reading, SDA pin outputs low. When writing, SDA pin is changed to output low. 1: When reading, SDA pin outputs high. When writing, SDA pin is changed to output Hi-Z (outputs high by external pull-up resistance).
4	SDAOP	1	R/W	SDAO Write Protect Controls change of output level of the SDA pin by modifying the SDAO bit. To change the output level, clear SDAO and SDAOP to 0 or set SDAO to 1 and clear SDAOP to 0. This bit is always read as 1.
3	SCLO	1	R	SCL Output Level Monitors SCL output level. When SCLO is 1, SCL pin outputs high. When SCLO is 0, SCL pin outputs low.
2	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
1	IICRST	0	R/W	IIC Control Part Reset Resets the control part except for I^2C registers. If this bit is set to 1 when hang-up occurs because of communication failure during I^2C bus operation, some IIC3 registers and the control part can be reset.
0	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.

Pin number	Pin number	Pin name				
		Initial function				
		On-chip ROM unabled mode		On-chip ROM enabled mode	Single-chip mode	
BGA	LQFP	MCU mode 0	MCU mode 1	MCU mode 2	MCU mode 3	Settable function in PFC
F13	123	NMI				—
C13	134	FWE/$\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$				—
B13	135	$\overline{\text{ASEMD0}}$				—
D13	127	TCK				—
D14	128	TMS				—
D15	125	TDI				—
C15	126	TDO				—
C12	129	$\overline{\text{TRST}}$				—
B8	157	PA0				PA0/$\overline{\text{CS0}}$*1/IRQ4/CRx0/RXD0/RX_CLK
C7	158	PA1				PA1/$\overline{\text{CS1}}$*1/IRQ5/CTx0/TXD0/MII_RXD0
A7	159	PA2				PA2/$\overline{\text{CS2}}$*1/TCLKD/SSL0/SCK0/MII_RXD1
B7	160	PA3				PA3/$\overline{\text{CS3}}$*1/TCLKC/MISO/RXD1/MII_RXD2
D6	161	PA4				PA4/$\overline{\text{CS4}}$*1/TCLKB/MOSI/TXD1/MII_RXD3
C6	162	PA5				PA5/$\overline{\text{CS5}}$*1/TCLKA/RSPCK/SCK1/RX_ER
K14	103	PA6				PA6/$\overline{\text{CS6}}$*1/IRQ6/TCLKA/RSPCK/SCK1/TX_ER
K13	102	PA7				PA7/$\overline{\text{CS5}}$*1/IRQ5/TCLKB/MOSI/TXD1/MII_TXD3
K12	101	PA8				PA8/$\overline{\text{CS4}}$*1/IRQ4/TCLKC/MISO/RXD1/MII_TXD2
L15	100	PA9				PA9/$\overline{\text{CS3}}$*1/IRQ3/TCLKD/SSL0/SCK0/MII_TXD1

22.1.9 Port C Pull-Up MOS Control Register L (PCPCRL)

PCPCRL controls on/off of the input pull-up MOS of port C in bits.

- Port C Pull-Up MOS Control Register L (PCPCRL)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PC15 PCR	PC14 PCR	PC13 PCR	PC12 PCR	PC11 PCR	PC10 PCR	PC9 PCR	PC8 PCR	PC7 PCR	PC6 PCR	PC5 PCR	PC4 PCR	PC3 PCR	PC2 PCR	PC1 PCR	PC0 PCR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

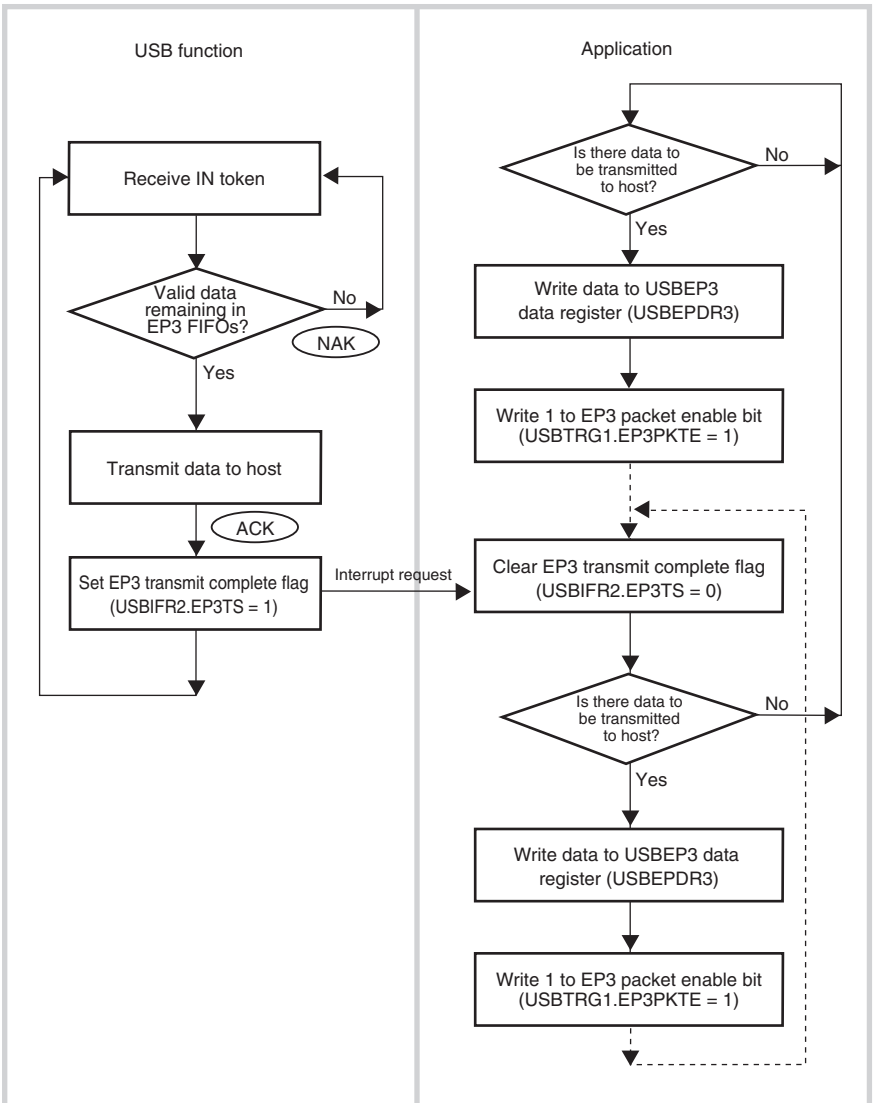
Bit	Bit Name	Initial Value	R/W	Description
15	PC15PCR	0	R/W	The corresponding input pull-up MOS turns on when one of these bits is set to 1.
14	PC14PCR	0	R/W	
13	PC13PCR	0	R/W	
12	PC12PCR	0	R/W	
11	PC11PCR	0	R/W	
10	PC10PCR	0	R/W	
9	PC9PCR	0	R/W	
8	PC8PCR	0	R/W	
7	PC7PCR	0	R/W	
6	PC6PCR	0	R/W	
5	PC5PCR	0	R/W	
4	PC4PCR	0	R/W	
3	PC3PCR	0	R/W	
2	PC2PCR	0	R/W	
1	PC1PCR	0	R/W	
0	PC0PCR	0	R/W	

- Port D Pull-Up MOS Control Register L (PDPCRL)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD15 PCR	PD14 PCR	PD13 PCR	PD12 PCR	PD11 PCR	PD10 PCR	PD9 PCR	PD8 PCR	PD7 PCR	PD6 PCR	PD5 PCR	PD4 PCR	PD3 PCR	PD2 PCR	PD1 PCR	PD0 PCR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

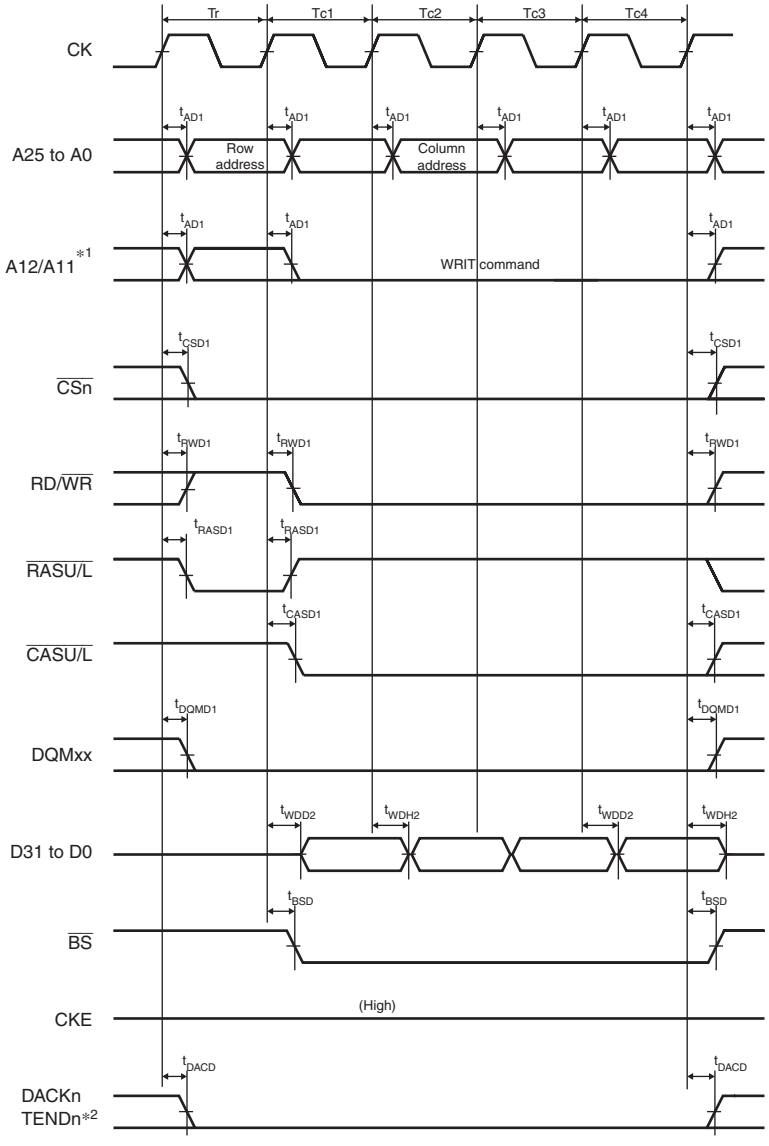
Bit	Bit Name	Initial Value	R/W	Description
15	PD15PCR	0	R/W	The corresponding input pull-up MOS turns on when one of these bits is set to 1.
14	PD14PCR	0	R/W	
13	PD13PCR	0	R/W	
12	PD12PCR	0	R/W	
11	PD11PCR	0	R/W	
10	PD10PCR	0	R/W	
9	PD9PCR	0	R/W	
8	PD8PCR	0	R/W	
7	PD7PCR	0	R/W	
6	PD6PCR	0	R/W	
5	PD5PCR	0	R/W	
4	PD4PCR	0	R/W	
3	PD3PCR	0	R/W	
2	PD2PCR	0	R/W	
1	PD1PCR	0	R/W	
0	PD0PCR	0	R/W	

24.5.7 EP3/EP6/EP9 Interrupt-IN Transfer



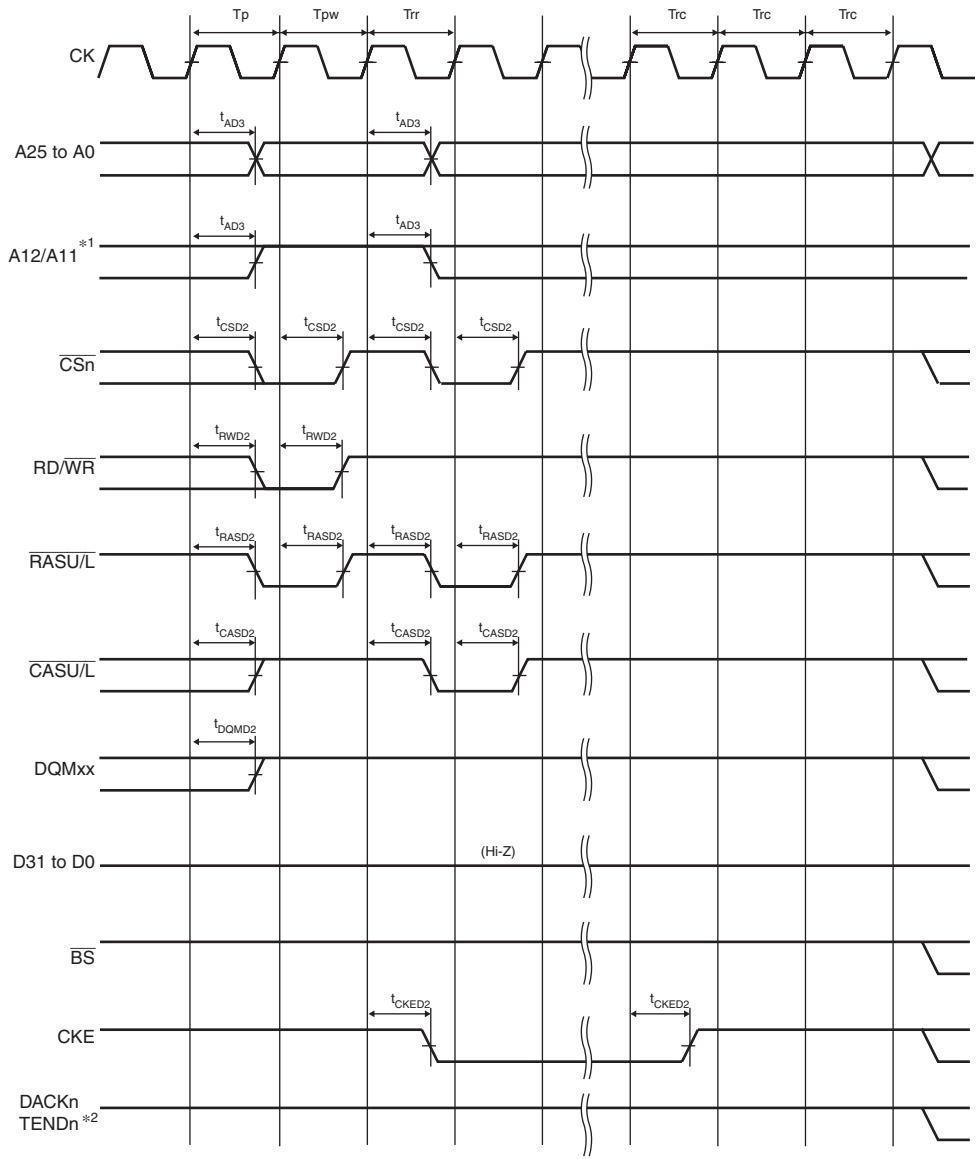
Note: This flowchart shows an example of interrupt transfer processing. However, another flow can be considered: when there is data to be transmitted, FIFO emptiness is checked by reading the EP3DE bit in the USB data status register and then data is written to the FIFO.

Figure 24.13 EP3 Interrupt-IN Transfer Operation



Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 33.29 Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Bank Active Mode: ACT + WRITE Commands, WTRCD = 0 Cycle, TRWL = 0 Cycle)



Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 33.36 Synchronous DRAM Self-Refreshing Timing in Low-Frequency Mode (WTRP = 2 Cycles)

33.3.9 Watchdog Timer Timing

Table 33.13 Watchdog Timer Timing

Conditions: $V_{cc}Q = PLLV_{cc} = DrV_{cc} = 3.0$ to 3.6 V, $AV_{cc} = AVREF = 4.5$ to 5.5 V,
$V_{ss} = PLLV_{ss} = DrV_{ss} = AVREFVSS = AV_{ss} = 0$ V,
Ta = –40°C to +85°C (Industrial specifications)

Item	Symbol	Min.	Max.	Unit	Figure
$\overline{\text{WDTOVF}}$ delay time	t_{WOVD}	—	50	ns	Figure 33.44

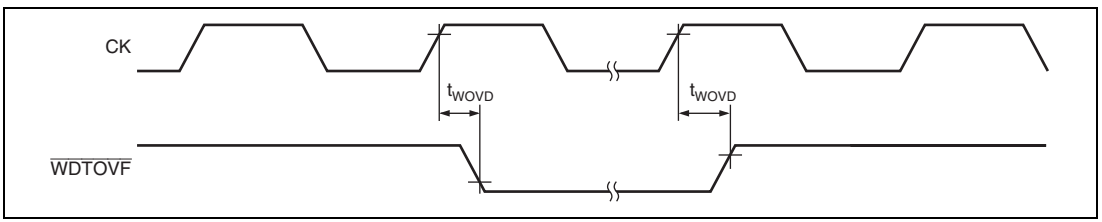


Figure 33.44 Watchdog Timer Timing

33.7 FLD Characteristics

Table 33.26 FLD (Flash Memory for Data Storage) Characteristics

Conditions: $V_{CC}Q = PLLV_{CC} = DrV_{CC} = 3.0$ to 3.6 V, $AV_{CC} = AVREF = 4.5$ to 5.5V,
$V_{SS} = PLLV_{SS} = DrV_{SS} = AVREFVSS = AV_{SS} = 0$ V,
Operating temperature range during programming/erasing:
Ta = –40°C to +85°C (Industrial specifications)

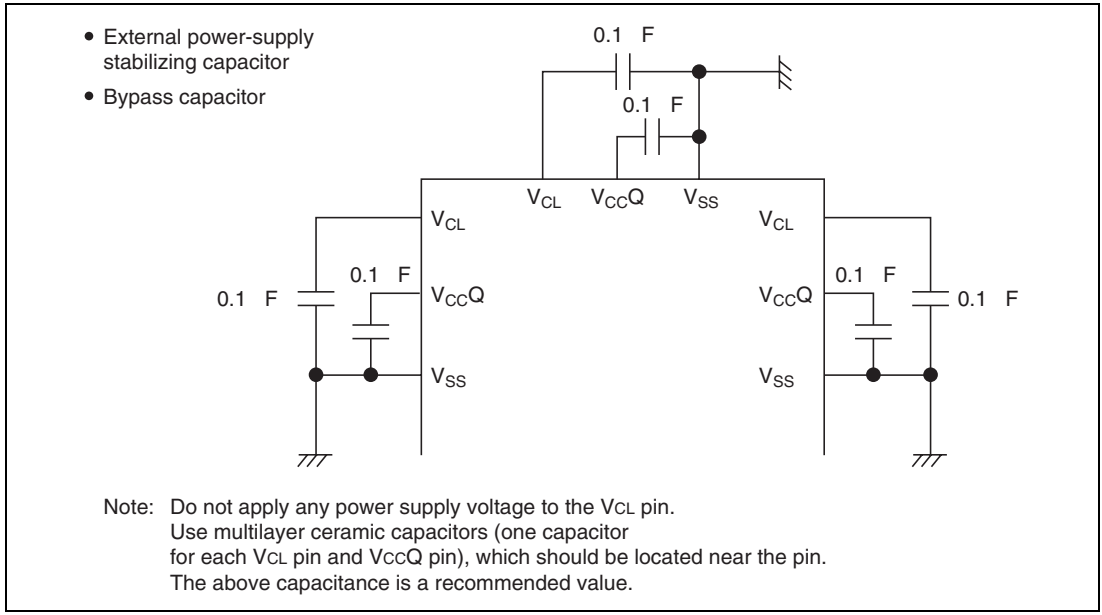
Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Figure
Programming time	8 bytes	t_{P8}	—	0.4	2	ms	Pϕ = 50 MHz	
	128 bytes	t_{P128}	—	1	5	ms		
Erasure time	8 Kbytes	t_{E8K}	—	300	900	ms	Pϕ = 50 MHz	
Blank check time	8 bytes	t_{BC8}	—	—	30	µs	Pϕ = 50 MHz	
	8 Kbytes	t_{BC8K}	—	—	2.5	ms		
Rewrite/erase cycle*1		N_{PEC}	30000*2	—	—	Times		
Suspend delay time during writing		t_{SPD}	—	—	225	µs	Pϕ = 20 MHz	Figure 33.71
			—	—	175	µs	Pϕ = 40 MHz	
			—	—	155	µs	Pϕ = 50 MHz	
First suspend delay time during erasing (in suspension priority mode)		t_{SESD1}	—	—	220	µs	Pϕ = 20 MHz	
			—	—	130	µs	Pϕ = 40 MHz	
			—	—	120	µs	Pϕ = 50 MHz	
Second suspend delay time during erasing (in suspension priority mode)		t_{SESD2}	—	—	1.7	ms	Pϕ = 50 MHz	
Suspend delay time during erasing in erasure priority mode		t_{SEED}	—	—	1.7	ms		
Resume command interval time		t_{RESI}	1.7	—	—	ms		
Data hold time*3		t_{DDRP}	10	—	—	Years		

33.8 Usage Notes

33.8.1 Notes on Connecting Capacitors

This LSI includes an internal step-down circuit to automatically reduce the internal power supply voltage to an appropriate level. Between this internal stepped-down power supply (V_{CL} pin) and the V_{SS} pin, a capacitor for stabilizing the internal voltage needs to be connected. Connection of the external capacitor is shown in figure 33.72. The external capacitor should be located near the pin. Do not apply any power supply voltage to the V_{CL} pin.

A multilayer ceramic capacitor should be inserted for each pair of power supply pins as a bypass capacitor. The bypass capacitor must be inserted as close to the power supply pins of the LSI as possible. Connect the bypass capacitor and the capacitor for stabilizing the internal voltage with the capacitance from 0.02 to 0.33 µF, after being evaluated in the system. For details on capacitors related to crystal oscillation, see section 4.9, Notes on Board Design.



Note: Do not apply any power supply voltage to the VCL pin.
Use multilayer ceramic capacitors (one capacitor for each VCL pin and VCCQ pin), which should be located near the pin.
The above capacitance is a recommended value.

Figure 33.72 Connection of Capacitors

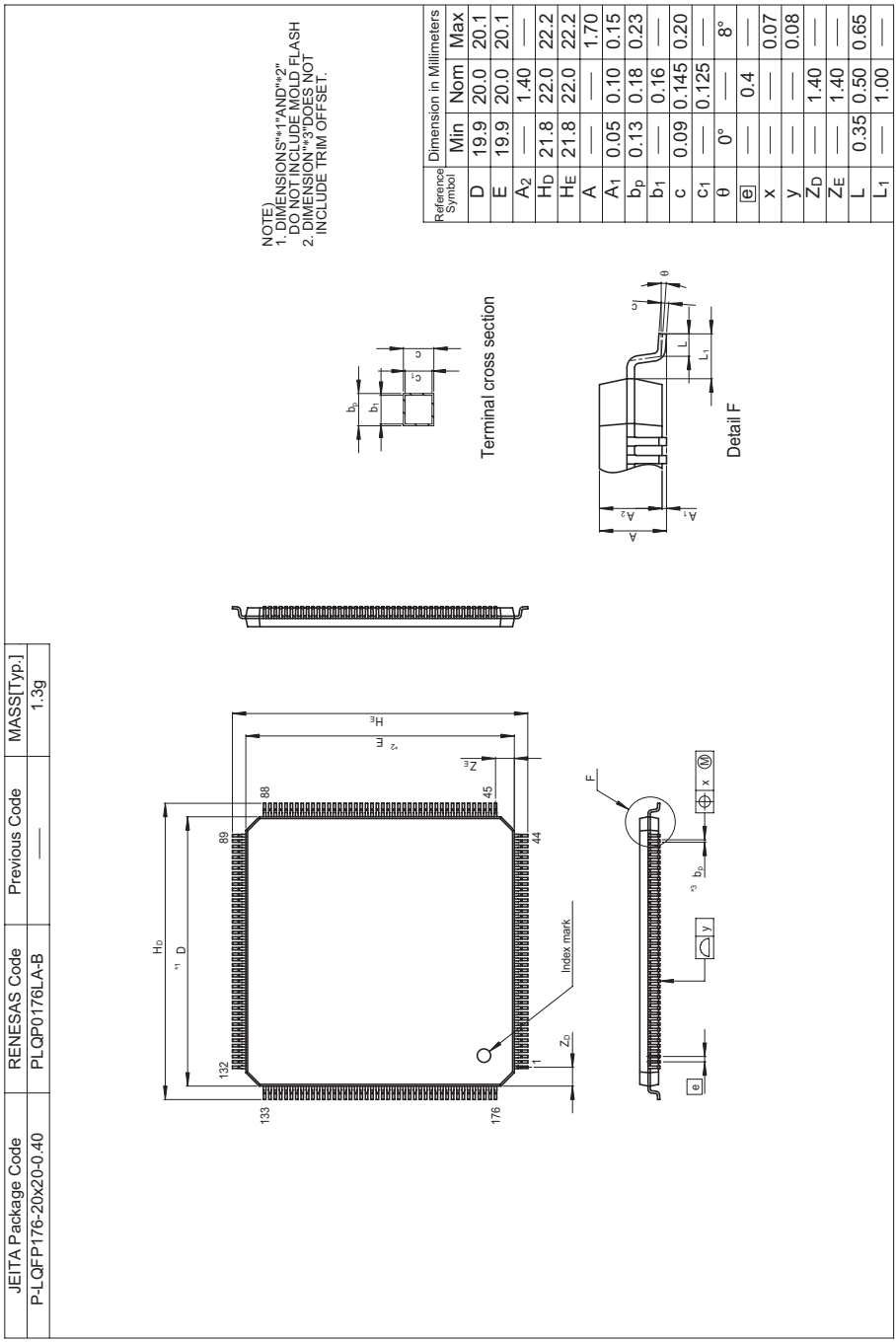


Figure C.2 Package Dimensions (2)