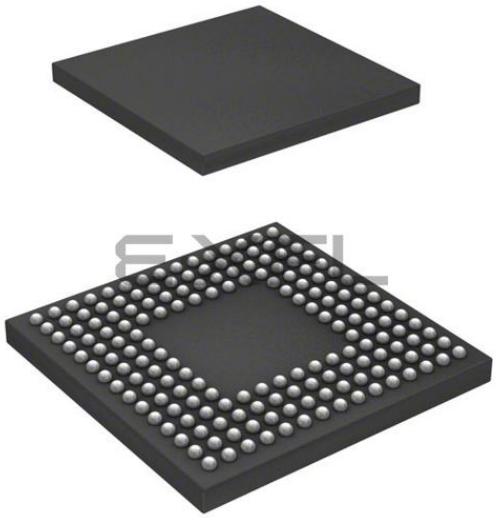
Renesas Electronics America Inc - R5F72147BDBG#U1 Datasheet



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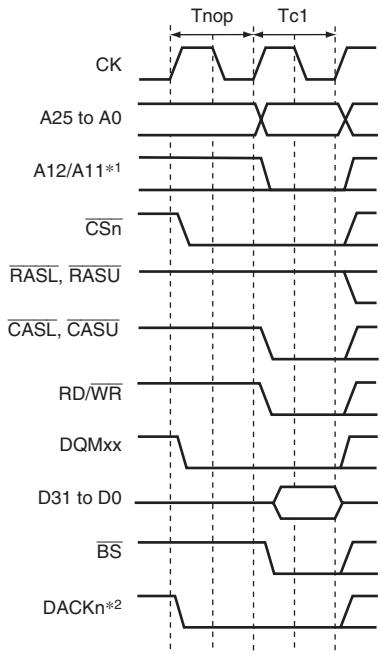
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, I²C, SCI, SPI, USB
Peripherals	DMA, PWM, WDT
Number of I/O	112
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f72147bdbg-u1



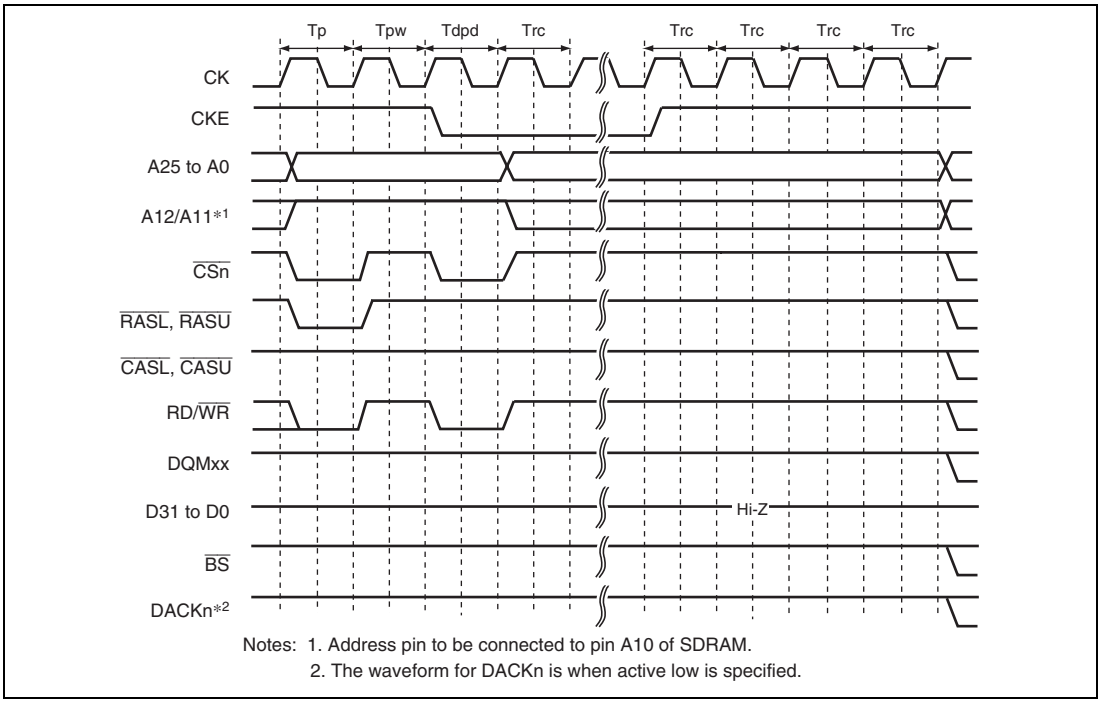
Notes: 1. Address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn is when active low is specified.

Figure 9.27 Single Write Timing (Bank Active, Same Row Addresses in the Same Bank)

- Deep power-down mode

  The low-power SDRAM supports deep power-down mode as a low-power consumption mode. In the partial self-refresh function, self-refresh is performed on a specific area. In deep power-down mode, self-refresh will not be performed on any memory area. This mode is effective in systems where all of the system memory areas are used as work areas.

If the RMODE bit in the SDCR is set to 1 while the DEEP and RFSH bits in the SDCR are set to 1, the low-power SDRAM enters deep power-down mode. If the RMODE bit is cleared to 0, the CKE signal is pulled high to cancel deep power-down mode. Before executing an access after returning from deep power-down mode, the power-up sequence must be re-executed.



Notes: 1. Address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn is when active low is specified.

Figure 9.35 Deep Power-Down Mode Transition Timing

11.3.16 Timer Synchronous Register (TSYR)

TSYR is an 8-bit readable/writable register that selects independent operation or synchronous operation for the channel 0 to 4 TCNT counters. A channel performs synchronous operation when the corresponding bit in TSYR is set to 1.

Bit:	7	6	5	4	3	2	1	0
	SYNC4	SYNC3	-	-	-	SYNC2	SYNC1	SYNC0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	SYNC4	0	R/W	Timer Synchronous operation 4 and 3
6	SYNC3	0	R/W	These bits are used to select whether operation is independent of or synchronized with other channels. When synchronous operation is selected, the TCNT synchronous presetting of multiple channels, and synchronous clearing by counter clearing on another channel, are possible. To set synchronous operation, the SYNC bits for at least two channels must be set to 1. To set synchronous clearing, in addition to the SYNC bit, the TCNT clearing source must also be set by means of bits CCLR0 to CCLR2 in TCR. 0: TCNT_4 and TCNT_3 operate independently (TCNT presetting/clearing is unrelated to other channels) 1: TCNT_4 and TCNT_3 performs synchronous operation TCNT synchronous presetting/synchronous clearing is possible
5 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Figure 11.6 illustrates periodic counter operation.

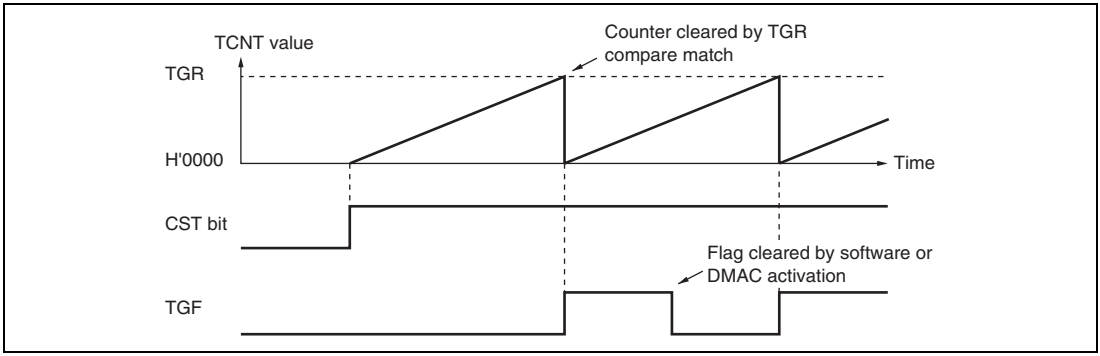


Figure 11.6 Periodic Counter Operation

(2) Waveform Output by Compare Match

The MTU2 can perform 0, 1, or toggle output from the corresponding output pin using compare match.

(a) Example of Setting Procedure for Waveform Output by Compare Match

Figure 11.7 shows an example of the setting procedure for waveform output by compare match.

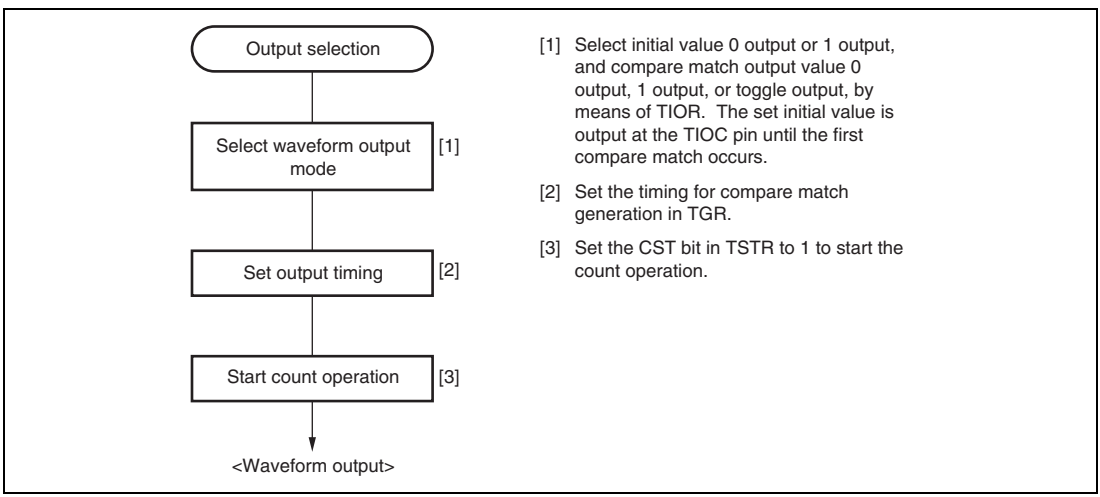


Figure 11.7 Example of Setting Procedure for Waveform Output by Compare Match

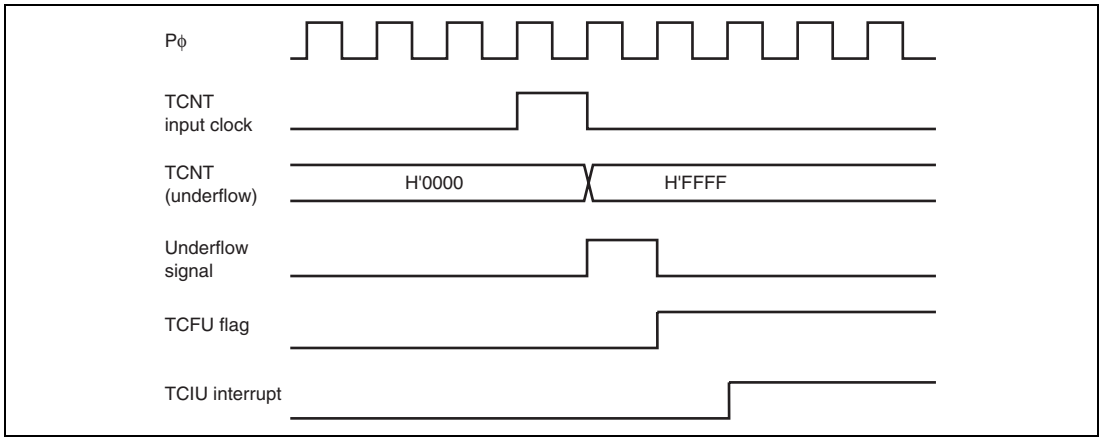


Figure 11.114 TCIU Interrupt Setting Timing

(4) Status Flag Clearing Timing

After a status flag is read as 1 by the CPU, it is cleared by writing 0 to it. When the DMAC is activated, the flag is cleared automatically. Figures 11.115 and 116 show the timing for status flag clearing by the CPU, and figure 11.117 shows the timing for status flag clearing by the DMAC.

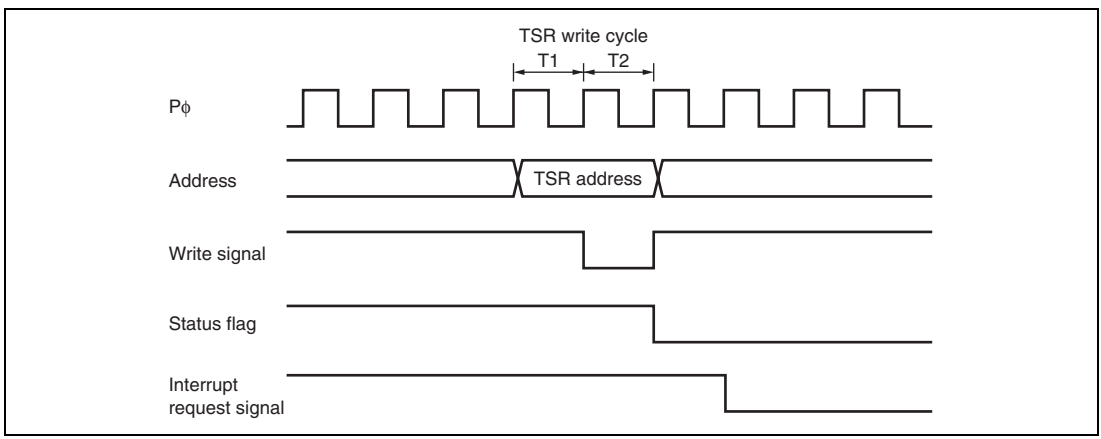


Figure 11.115 Timing for Status Flag Clearing by CPU (Channels 0 to 4)

16.7.6 Note on Using DTC

When the external clock source is used for the clock for synchronization, input the external clock after waiting for five or more cycles of the peripheral operating clock after SCTDR is modified through the DTC. If a transmit clock is input within four cycles after SCTDR is modified, a malfunction may occur (figure 16.22).

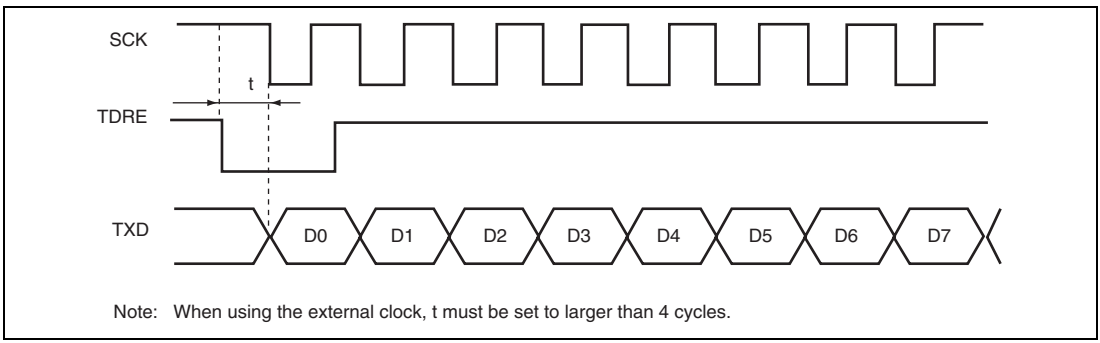


Figure 16.22 Example of Clock Synchronous Transfer Using DTC

When data is written to SCTDR by activating the DTC by a TXI interrupt, the TEND flag value becomes undefined. In this case, do not use the TEND flag as the transmit end flag.

16.7.7 Note on Using External Clock in Clock Synchronous Mode

TE and RE must be set to 1 after waiting for four or more cycles of the peripheral operating clock after the SCK external clock is changed from 0 to 1.

TE and RE must be set to 1 only while the SCK external clock is 1.

16.7.8 Module Standby Mode Setting

SCI operation can be disabled or enabled using the standby control register. The initial setting is for SCI operation to be halted. Register access is enabled by clearing module standby mode. For details, refer to section 30, Power-Down Modes.

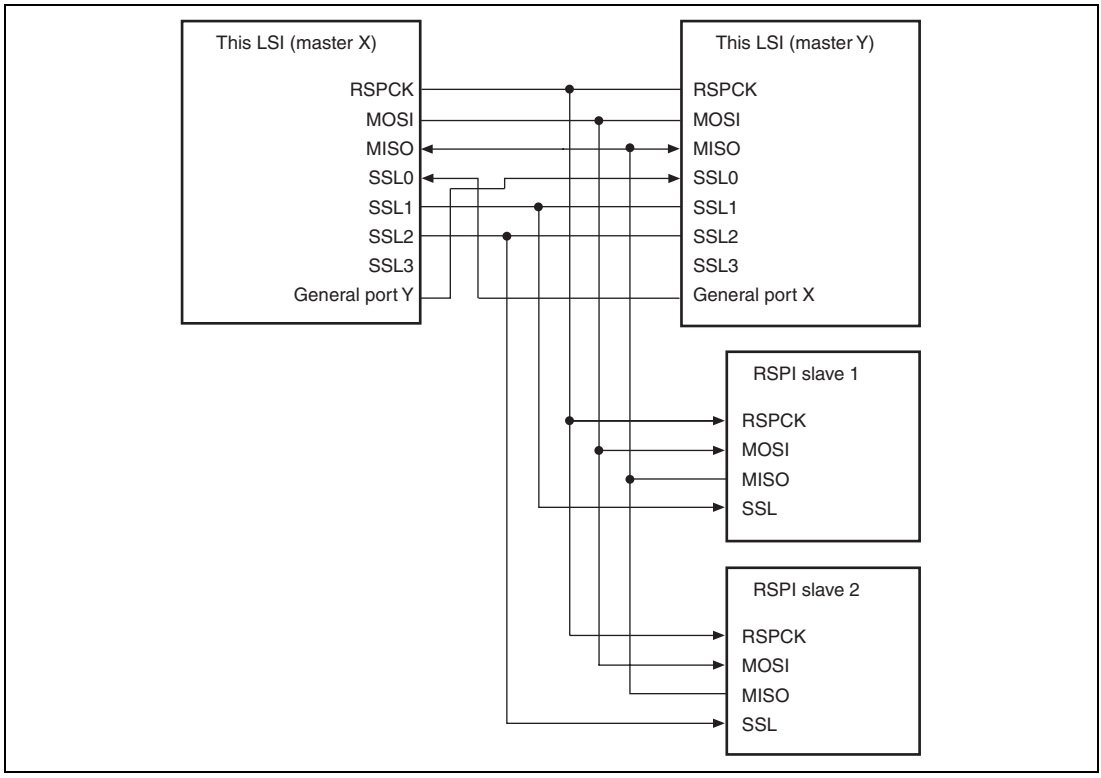


Figure 18.7 Multi-Master/Multi-Slave Configuration Example (This LSI = Master)

Bit	Bit Name	Initial Value	R/W	Description
2	AL/OVE	0	R/W	Arbitration Lost Flag/Overrun Error Flag Indicates that arbitration was lost in master mode with the I^2C bus format and that the final bit has been received while RDRF = 1 with the clocked synchronous format. When two or more master devices attempt to seize the bus at nearly the same time, if the I^2C bus interface 3 detects data differing from the data it sent, it sets AL to 1 to indicate that the bus has been occupied by another master. [Clearing condition] • When 0 is written in AL/OVE after reading AL/OVE = 1 [Setting conditions] • If the internal SDA and SDA pin disagree at the rise of SCL in master transmit mode • When the SDA pin outputs high in master mode while a start condition is detected • When the final bit is received with the clocked synchronous format while RDRF = 1
1	AAS	0	R/W	Slave Address Recognition Flag In slave receive mode, this flag is set to 1 if the first frame following a start condition matches bits SVA[6:0] in SAR. [Clearing condition] • When 0 is written in AAS after reading AAS = 1 [Setting conditions] • When the slave address is detected in slave receive mode • When the general call address is detected in slave receive mode.
0	ADZ	0	R/W	General Call Address Recognition Flag This bit is valid in slave receive mode with the I^2C bus format. [Clearing condition] • When 0 is written in ADZ after reading ADZ = 1 [Setting condition] • When the general call address is detected in slave receive mode

(2) Local Acceptance Filter Mask (LAFM)

This area is used as Local Acceptance Filter Mask (LAFM) for receive boxes**.**

LAFM: When MBC is set to 001, 010, 011 (Bin), this field is used as LAFM Field. It allows a Mailbox to accept more than one identifier. The LAFM is comprised of two 16-bit read/write areas as follows.

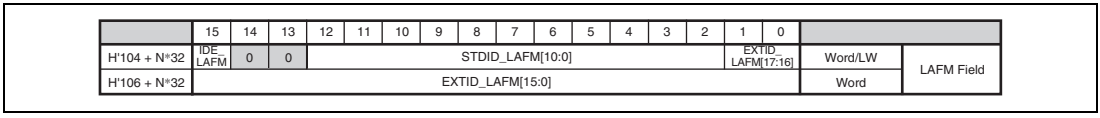


Figure 21.4 Acceptance Filter

If a bit is set in the LAFM, then the corresponding bit of a received CAN identifier is ignored when the RCAN-ET searches a Mailbox with the matching CAN identifier. If the bit is cleared, then the corresponding bit of a received CAN identifier must match to the STDID/IDE/EXTID set in the mailbox to be stored. The structure of the LAFM is same as the message control in a Mailbox. If this function is not required, it must be filled with '0'.

Important: RCAN-ET starts to find a matching identifier from Mailbox-15 down to Mailbox-0. As soon as RCAN-ET finds one matching, it stops the search. The message will be stored or not depending on the NMC and RXPR/RFPR flags. This means that, even using LAFM, a received message can only be stored into 1 Mailbox.

Important: When a message is received and a matching Mailbox is found, the whole message is stored into the Mailbox. This means that, if the LAFM is used, the STDID, RTR, IDE and EXTID may differ to the ones originally set as they are updated with the STDID, RTR, IDE and EXTID of the received message.

STD_LAFM[10:0] — Filter mask bits for the CAN base identifier [10:0] bits.

STD_LAFM[10:0]	Description
0	Corresponding STD_ID bit is cared
1	Corresponding STD_ID bit is "don't cared"

22.1.3 Port A Pull-Up MOS Control Registers H and L (PAPCRH and PAPCRL)

PAPCRH and PAPCRL control on and off of the input pull-up MOS of port A in bits.

- Port A Pull-Up MOS Control Register H (PAPCRH)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	PA21 PCR	PA20 PCR	PA19 PCR	PA18 PCR	PA17 PCR	PA16 PCR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	PA21PCR	0	R/W	The corresponding input pull-up MOS turns on when one of these bits is set to 1.
4	PA20PCR	0	R/W	
3	PA19PCR	0	R/W	
2	PA18PCR	0	R/W	
1	PA17PCR	0	R/W	
0	PA16PCR	0	R/W	

- Port C Control Register L2 (PCCRL2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	PC7MD[2:0]			-	PC6MD[2:0]			-	PC5MD[2:0]			-	PC4MD[2:0]		
Initial value:	0	0	0	0*	0	0	0	0*	0	0	0	0*	0	0	0	0*
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Note: * The initial value is 1 during the on-chip ROM disabled external extension mode.

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	PC7MD[2:0]	000*	R/W	PC7 Mode Select the function of the PC7/A7 pin. 000: PC7 I/O (port) 001: A7 output (BSC) 010: Setting prohibited 011: Setting prohibited 100: Setting prohibited 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	PC6MD[2:0]	000*	R/W	PC6 Mode Select the function of the PC6/A6 pin. 000: PC6 I/O (port) 001: A6 output (BSC) 010: Setting prohibited 011: Setting prohibited 100: Setting prohibited 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	PE10MD[2:0]	000	R/W	PE10 Mode Select the function of the PE10/DREQ3/TIOC3C/SSL3/TXD2/TX_CLK pin. 000: PE10 I/O (port) 001: Setting prohibited 010: DREQ3 input (DMAC) 011: Setting prohibited 100: TIOC3C I/O (MTU2) 101: SSL3 output (RSPI) 110: TXD2 output (SCI) 111: TX_CLK input (Ether)
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	PE9MD[2:0]	000	R/W	PE9 Mode Select the function of the PE9/DACK2/TIOC3B/TX_EN pin. 000: PE9 I/O (port) 001: Setting prohibited 010: DACK2 output (DMAC) 011: Setting prohibited 100: TIOC3B I/O (MTU2) 101: Setting prohibited 110: Setting prohibited 111: TX_EN output (Ether)
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

2. When the port input is switched from the low level to the DREQ edge or the IRQ edge for the pins that are multiplexed with I/O and DREQ or IRQ, the corresponding edge is detected.
3. Do not set functions other than settable functions. Otherwise, correct operation cannot be guaranteed.

23.6.2 Port F Data Register L (PFDRL)

PFDRL is a 16-bit read-only register that stores port F data. In this LSI, bits PF7DR to PF0DR correspond to pins PF7 to PF0, respectively (description of multiplexed functions are abbreviated here).

Even if a value is written to PFDR, the value is not written into PFDR, and it does not affect the pin state. If PFDR is read, the pin state, not the register value, is returned directly. However, when sampling the analog input of A/D converter, 1 is read. Table 23.12 summarizes read/write operations of port F data register.

- Port F data register L (PFDRL)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	PF7DR	PF6DR	PF5DR	PF4DR	PF3DR	PF2DR	PF1DR	PF0DR
Initial value:	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	PF7DR	Pin state	R	See table 23.12.
6	PF6DR	Pin state	R	
5	PF5DR	Pin state	R	
4	PF4DR	Pin state	R	
3	PF3DR	Pin state	R	
2	PF2DR	Pin state	R	
1	PF1DR	Pin state	R	
0	PF0DR	Pin state	R	

Table 23.12 Port F Data Register L (PFDRL) Read/Write Operations

Pin Function	Read	Write
General input	Pin state	Ignored (no effect on pin state)
ANn input	1	Ignored (no effect on pin state)

24.3.42 USB FIFO Clear Register 2 (USBFCLR2)

USBFCLR2 is a write-only register to initialize the FIFO buffers for each endpoint. Writing 1 to a bit clears all the data in the corresponding FIFO buffer. The corresponding interrupt flag is not cleared. Do not clear the FIFO buffer during transmission/reception. The read value of this register is undefined. Do not write a value to this register using the read value, such as a bit manipulation instruction.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	EP6 CLR	EP5 CLR	EP4 CLR
Initial value:	0	0	0	0	0	0	0	0
R/W:	-	-	-	-	-	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	—	Reserved The write value should always be 0.
2	EP6CLR	0	W	EP6 Clear Writing 1 to this bit initializes the endpoint 6 transmit FIFO buffer.
1	EP5CLR	0	W	EP5 Clear Writing 1 to this bit initializes both endpoint 5 transmit FIFO buffers.
0	EP4CLR	0	W	EP4 Clear Writing 1 to this bit initializes both endpoint 4 receive FIFO buffers.

24.5.4 Control Transfer

Control transfer consists of three stages: setup, data (not always included), and status as illustrated in figure 24.5. The data stage comprises a number of bus transactions. Operation flowcharts for each stage are shown below.

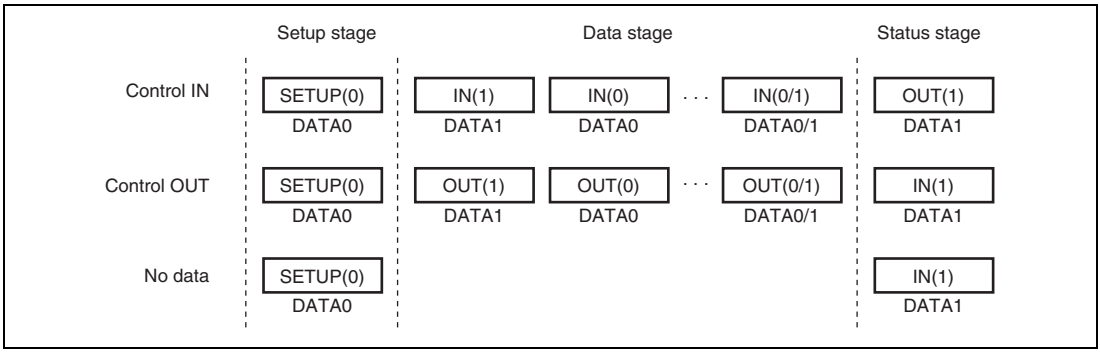


Figure 24.5 Transfer Stages in Control Transfer

25.4.4 Accessing MII Registers

MII registers in the PHY-LSI are accessed through the PHY interface register (PIR) in this LSI. Connection is made as a serial interface in accordance with the MII frame format specified in IEEE802.3u.

(1) MII Management Frame Format

Figure 25.5 shows the format of an MII management frame. To access an MII register, a management frame is implemented by the program in accordance with the procedures shown in (2) MII Register Access Procedure.

Access Type	MII Management Frame							
Item	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Bits	32	2	2	5	5	2	16	
Read	1..1	01	10	00001	RRRRR	Z0	D..D	
Write	1..1	01	01	00001	RRRRR	10	D..D	X

[Legend]

PRE: 32 consecutive 1s
ST: Write of 01 indicating start of frame
OP: Write of code indicating access type
PHYAD: Write of 0001 when the PHY-LSI address is 1 (sequential write starting with the MSB)
The PHYAD bits vary with the PHY-LSI address.
REGAD: Write of 0001 when the register address is 1 (sequential write starting with the MSB)
The REGAD bits vary with the PHY-LSI register address.
TA: Time for switching data transmission source on the MII interface
(a) Write: 10 written
(b) Read: Bus release [notation: Z0] performed
DATA: 16-bit data. Sequential write or read starting with the MSB
(a) Write: 16-bit data write
(b) Read: 16-bit data read
IDLE: Wait time until next MII management format input
(a) Write: Independent bus release [notation: X] performed
(b) Read: Bus already released at TA (control unnecessary)

Figure 25.5 MII Management Frame Format

No.	Pin Name	Type
43	PD28/D28/TIOC3DS/MII_RXD2	CONTROL
42	PD28/D28/TIOC3DS/MII_RXD2	INPUT
41	PD29/D29/TIOC3BS/MII_RXD3	OUTPUT
40	PD29/D29/TIOC3BS/MII_RXD3	CONTROL
39	PD29/D29/TIOC3BS/MII_RXD3	INPUT
38	PD30/D30/TIOC3CS/SSL3/RX_ER	OUTPUT
37	PD30/D30/TIOC3CS/SSL3/RX_ER	CONTROL
36	PD30/D30/TIOC3CS/SSL3/RX_ER	INPUT
35	PD31/D31/TIOC3AS/SSL2/RX_DV	OUTPUT
34	PD31/D31/TIOC3AS/SSL2/RX_DV	CONTROL
33	PD31/D31/TIOC3AS/SSL2/RX_DV	INPUT
32	PA12/$\overline{\text{CS0}}$/IRQ0/TIC5U/SSL1/TX_CLK	OUTPUT
31	PA12/$\overline{\text{CS0}}$/IRQ0/TIC5U/SSL1/TX_CLK	CONTROL
30	PA12/$\overline{\text{CS0}}$/IRQ0/TIC5U/SSL1/TX_CLK	INPUT
29	PA11/$\overline{\text{CS1}}$/IRQ1/TIC5V/CRx0/RXD0/TX_EN	OUTPUT
28	PA11/$\overline{\text{CS1}}$/IRQ1/TIC5V/CRx0/RXD0/TX_EN	CONTROL
27	PA11/$\overline{\text{CS1}}$/IRQ1/TIC5V/CRx0/RXD0/TX_EN	INPUT
26	PA10/$\overline{\text{CS2}}$/IRQ2/TIC5W/CTx0/TXD0/MII_TXD0	OUTPUT
25	PA10/$\overline{\text{CS2}}$/IRQ2/TIC5W/CTx0/TXD0/MII_TXD0	CONTROL
24	PA10/$\overline{\text{CS2}}$/IRQ2/TIC5W/CTx0/TXD0/MII_TXD0	INPUT
23	PA9/$\overline{\text{CS3}}$/IRQ3/TCLKD/SSL0/SCK0/MII_TXD1	OUTPUT
22	PA9/$\overline{\text{CS3}}$/IRQ3/TCLKD/SSL0/SCK0/MII_TXD1	CONTROL
21	PA9/$\overline{\text{CS3}}$/IRQ3/TCLKD/SSL0/SCK0/MII_TXD1	INPUT
20	PA8/$\overline{\text{CS4}}$/IRQ4/TCLKC/MISO/RXD1/MII_TXD2	OUTPUT
19	PA8/$\overline{\text{CS4}}$/IRQ4/TCLKC/MISO/RXD1/MII_TXD2	CONTROL
18	PA8/$\overline{\text{CS4}}$/IRQ4/TCLKC/MISO/RXD1/MII_TXD2	INPUT
17	PA7/$\overline{\text{CS5}}$/IRQ5/TCLKB/MOSI/TXD1/MII_TXD3	OUTPUT
16	PA7/$\overline{\text{CS5}}$/IRQ5/TCLKB/MOSI/TXD1/MII_TXD3	CONTROL
15	PA7/$\overline{\text{CS5}}$/IRQ5/TCLKB/MOSI/TXD1/MII_TXD3	INPUT
14	PA6/$\overline{\text{CS6}}$/IRQ6/TCLKA/RSPCK/SCK1/TX_ER	OUTPUT
13	PA6/$\overline{\text{CS6}}$/IRQ6/TCLKA/RSPCK/SCK1/TX_ER	CONTROL
12	PA6/$\overline{\text{CS6}}$/IRQ6/TCLKA/RSPCK/SCK1/TX_ER	INPUT

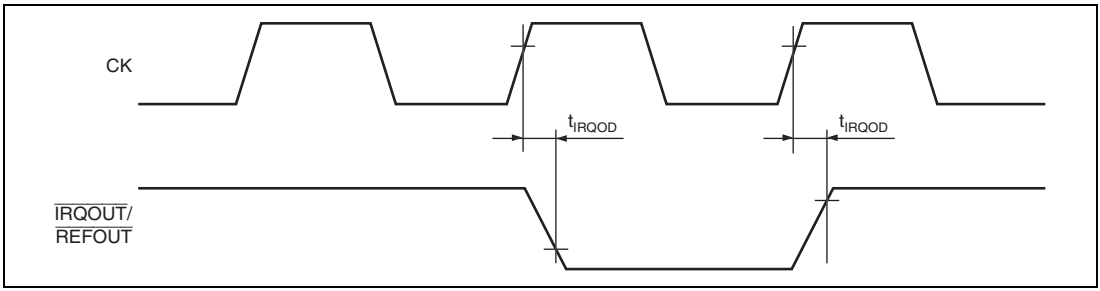


Figure 33.9 Interrupt Signal Output Timing

Q

R