Renesas Electronics America Inc - R5F72147HDFP#V1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, Ethernet, I²C, SCI, SPI, USB
Peripherals	DMA, PWM, WDT
Number of I/O	112
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f72147hdfp-v1

(8) AD Clock Frequency Control Register (ACLKCR)

The AD clock frequency control register (ACLKCR) has control bits assigned for the following functions: the frequency division ratio of the AD clock (Aϕ).

(9) Standby Control Register

The standby control register has bits for controlling the power-down modes and for selecting the USB clock. See section 30, Power-Down Modes, for more information.

(10) Oscillation Stop Detection Control Register (OSCCR)

The oscillation stop detection control register (OSCCR) has an oscillation stop detection flag and a bit for selecting flag status output through an external pin.

(11) USB-only oscillator

The oscillator for USB clock only that is connected to the resonator of 48 MHz.

When Iϕ:Bϕ = 8:1, n = 7 to 0 and I = 1.
When Bϕ:Pϕ = 1:1, m = 0.
When Bϕ:Pϕ = 2:1, m = 1, 0.
n and m depend on the internal execution state.

Synchronous logic and a layered bus structure have been adopted for this LSI. Data on each bus are input and output in synchronization with rising edges of the corresponding clock signal. The C bus, the I bus, and the peripheral bus are synchronized with the Iϕ, Bϕ, and Pϕ clock, respectively.

Figure 9.45 shows an example of the timing of write access to the peripheral bus when Iϕ:Bϕ:Pϕ = 4:1:1. Data are output to the C bus, which is connected to the CPU, in synchronization with Iϕ. When Iϕ:Bϕ = 4:1, there are 4 cycles of this clock to one cycle of Bϕ, so four transfers to the I bus can proceed in one cycle of Bϕ. Thus, a period of up to 5 × Iϕ may be required before a rising edge of Bϕ, which is the time of transfer from the C bus to the I bus (a case where this takes 3 cycles of Iϕ is indicated in figure 9.45). When Iϕ: Bϕ = 4:1, transfer of data from the C bus to the I bus takes (2 + n) × Iϕ (n = 0 to 3). The relation between the timing of data transfer to the C bus and the rising edge of Bϕ depends on the state of program execution. When Bϕ:Pϕ = 1:1, transfer of data from the I bus to the peripheral bus takes 1Bϕ + 2Pϕ. In the case shown in the figure, where n = 1 and m = 0, the time required for access is 3 × Iϕ + 2 × Bϕ + 2 × Pϕ.

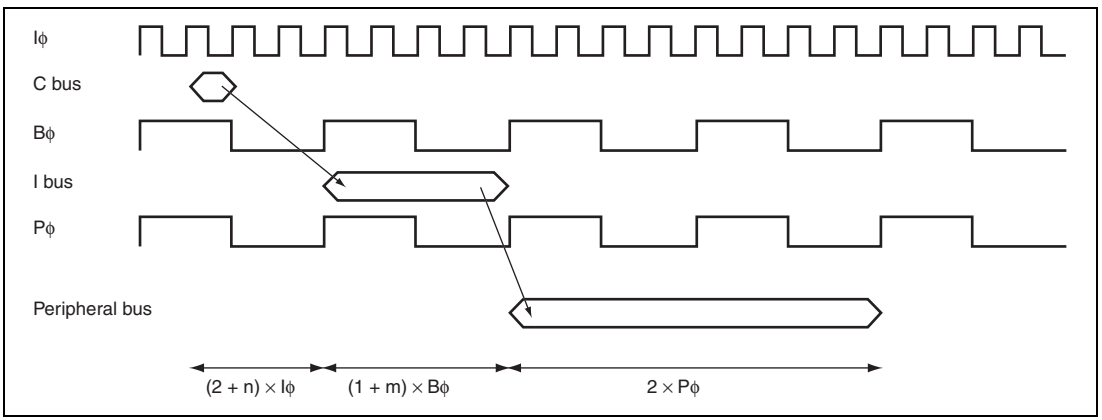


Figure 9.46 Timing of Write Access to On-Chip Peripheral I/O Registers When Iϕ;Bϕ:Pϕ = 4:1:1

Table 11.6 TPSC0 to TPSC2 (Channel 0)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
0	0	0	0	Internal clock: counts on Pϕ/1
			1	Internal clock: counts on Pϕ/4
		1	0	Internal clock: counts on Pϕ/16
			1	Internal clock: counts on Pϕ/64
	1	0	0	External clock: counts on TCLKA pin input
			1	External clock: counts on TCLKB pin input
		1	0	External clock: counts on TCLKC pin input
			1	External clock: counts on TCLKD pin input

Table 11.7 TPSC0 to TPSC2 (Channel 1)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
1	0	0	0	Internal clock: counts on Pϕ/1
			1	Internal clock: counts on Pϕ/4
		1	0	Internal clock: counts on Pϕ/16
			1	Internal clock: counts on Pϕ/64
	1	0	0	External clock: counts on TCLKA pin input
			1	External clock: counts on TCLKB pin input
		1	0	Internal clock: counts on Pϕ/256
			1	Counts on TCNT_2 overflow/underflow

Note: This setting is ignored when channel 1 is in phase counting mode.

Bit	Bit Name	Initial Value	R/W	Description
6	TTGE2	0	R/W	A/D Converter Start Request Enable 2 Enables or disables generation of A/D converter start requests by TCNT_4 underflow (trough) in complementary PWM mode. In channels 0 to 3, bit 6 is reserved. It is always read as 0 and the write value should always be 0. 0: A/D converter start request generation by TCNT_4 underflow (trough) disabled 1: A/D converter start request generation by TCNT_4 underflow (trough) enabled
5	TCIEU	0	R/W	Underflow Interrupt Enable Enables or disables interrupt requests (TCIU) by the TCFU flag when the TCFU flag in TSR is set to 1 in channels 1 and 2. In channels 0, 3, and 4, bit 5 is reserved. It is always read as 0 and the write value should always be 0. 0: Interrupt requests (TCIU) by TCFU disabled 1: Interrupt requests (TCIU) by TCFU enabled
4	TCIEV	0	R/W	Overflow Interrupt Enable Enables or disables interrupt requests (TCIV) by the TCFV flag when the TCFV flag in TSR is set to 1. 0: Interrupt requests (TCIV) by TCFV disabled 1: Interrupt requests (TCIV) by TCFV enabled
3	TGIED	0	R/W	TGR Interrupt Enable D Enables or disables interrupt requests (TGID) by the TGFD bit when the TGFD bit in TSR is set to 1 in channels 0, 3, and 4. In channels 1 and 2, bit 3 is reserved. It is always read as 0 and the write value should always be 0. 0: Interrupt requests (TGID) by TGFD bit disabled 1: Interrupt requests (TGID) by TGFD bit enabled

Bit	Bit Name	Initial Value	R/W	Description
2	CST2	0	R/W	Counter Start 2 to 0
1	CST1	0	R/W	These bits select operation or stoppage for TCNT.
0	CST0	0	R/W	If 0 is written to the CST bit during operation with the TIOC pin designated for output, the counter stops but the TIOC pin output compare output level is retained. If TIOR is written to when the CST bit is cleared to 0, the pin output level will be changed to the set initial output value. 0: TCNT_2 to TCNT_0 count operation is stopped 1: TCNT_2 to TCNT_0 performs count operation

- TSTR_5

Bit :	7	6	5	4	3	2	1	0
	-	-	-	-	-	CSTU5	CSTV5	CSTW5
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	CSTU5	0	R/W	Counter Start U5 Selects operation or stoppage for TCNTU_5. 0: TCNTU_5 count operation is stopped 1: TCNTU_5 performs count operation
1	CSTV5	0	R/W	Counter Start V5 Selects operation or stoppage for TCNTV_5. 0: TCNTV_5 count operation is stopped 1: TCNTV_5 performs count operation
0	CSTW5	0	R/W	Counter Start W5 Selects operation or stoppage for TCNTW_5. 0: TCNTW_5 count operation is stopped 1: TCNTW_5 performs count operation

11.3.21 Timer Output Control Register 2 (TOCR2)

TOCR2 is an 8-bit readable/writable register that controls output level inversion of PWM output in complementary PWM mode and reset-synchronized PWM mode.

Bit:	7	6	5	4	3	2	1	0
	BF[1:0]		OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial value	R/W	Description
7, 6	BF[1:0]	00	R/W	TOLBR Buffer Transfer Timing Select These bits select the timing for transferring data from TOLBR to TOCR2. For details, see table 11.32.
5	OLS3N	0	R/W	Output Level Select 3N*1*2 This bit selects the output level on TIOC4D in reset-synchronized PWM mode/complementary PWM mode. See table 11.33.
4	OLS3P	0	R/W	Output Level Select 3P*1*2 This bit selects the output level on TIOC4B in reset-synchronized PWM mode/complementary PWM mode. See table 11.34.
3	OLS2N	0	R/W	Output Level Select 2N*1*2 This bit selects the output level on TIOC4C in reset-synchronized PWM mode/complementary PWM mode. See table 11.35.
2	OLS2P	0	R/W	Output Level Select 2P*1*2 This bit selects the output level on TIOC4A in reset-synchronized PWM mode/complementary PWM mode. See table 11.36.
1	OLS1N	0	R/W	Output Level Select 1N*1*2 This bit selects the output level on TIOC3D in reset-synchronized PWM mode/complementary PWM mode. See table 11.37.

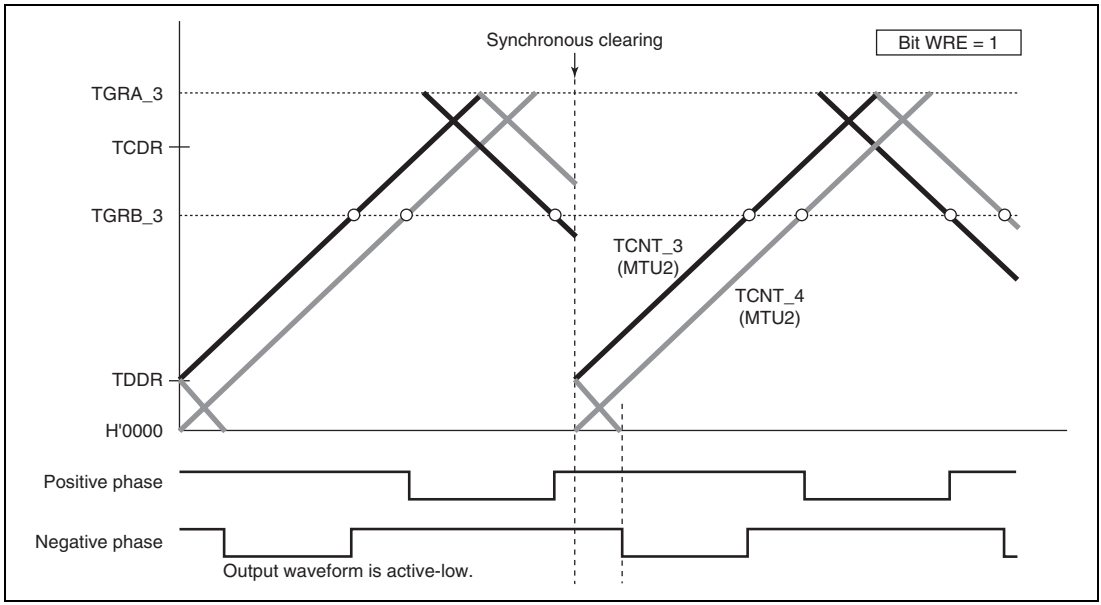


Figure 11.60 Example of Synchronous Clearing in Dead Time during Down-Counting (Timing (8) in Figure 11.56; Bit WRE of TWCR is 1)

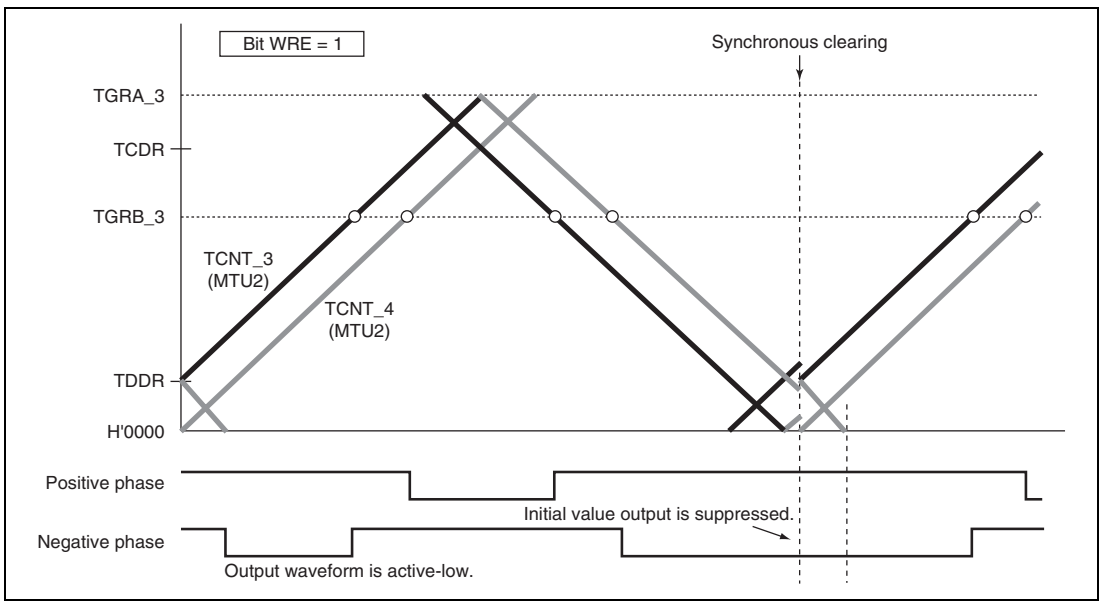


Figure 11.61 Example of Synchronous Clearing in Interval Tb at Trough (Timing (11) in Figure 11.56; Bit WRE of TWCR is 1)

17.3.11 Serial Port Register (SCSPTR)

SCSPTR controls input/output and data of pins multiplexed to SCIF function. Bits 3 and 2 can control input/output data of SCK pin. Bits 1 and 0 can input data from RXD pin and output data to TXD pin, so they control break of serial transmitting/receiving.

The CPU can always read and write to SCSPTR. SCSPTR is initialized to H'0050 by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	SCKIO	SCKDT	SPB2IO	SPB2DT
Initial value:	0	0	0	0	0	0	0	0	0	1	0	1	0	Undefined	0	Undefined
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	W	R/W	W

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
5	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
4	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
3	SCKIO	0	R/W	SCK Port Input/Output Indicates input or output of the serial port SCK pin. When the SCK pin is actually used as a port outputting the SCKDT bit value, the CKE[1:0] bits in SCSCR should be cleared to 0. 0: SCKDT bit value not output to SCK pin 1: SCKDT bit value output to SCK pin

of the SSL0 input signal depends on the setting in the SSL0P bit in the RSPI slave select polarity register (SSLP). For details on the RSPI transfer format, see section 18.4.4, Transfer Format.

(1-3) Notes on Single-Slave Operations

If the CPHA bit in RSPI command register 0(SPCMD0) is 0, the RSPI starts serial transfers when it detects the assertion edge for an SSL0 input signal. In the type of configuration shown in figure 18.4 as an example, if the RSPI is used in single-slave mode, the SSL0 signal is always fixed at active state. Therefore, when the CPHA bit is set to 0, the RSPI cannot correctly start a serial transfer. To correctly execute send/receive operation by the RSPI in a configuration in which the SSL0 input signal is fixed at active state, the CPHA bit should be set to 1. If there is a need for setting the CPHA bit to 0, the SSL0 input signal should not be fixed.

(1-4) Burst Transfer

If the CPHA bit in RSPI command register 0 (SPCMD0) is 1, continuous serial transfer (burst transfer) can be executed while retaining the assertion state for the SSL0 input signal. If the CPHA bit is 1, the period from the first RSPCK edge to the sampling timing for the reception of the final bit in an SSL0 signal active state corresponds to a serial transfer period. Even when the SSL0 input signal remains at the active level, the RSPI can accommodate burst transfers because it can detect the start of access.

If the CPHA bit is 0, for the reason given in (1-3), Notes on Single-Slave Operations, second and subsequent serial transfers during the burst transfer cannot be executed correctly.

(1-5) Initialization Flowchart

Figure 18.18 shows an example of initialization flowchart for using the RSPI in slave mode during SPI operation. For a description of how to set up an interrupt controller, the DTC/DMAC, and input/output ports, see the descriptions given in the individual blocks.

- With the module in master transmit or master receive mode, SDA at the low level, and no other device holding SCL at the low level, issue a stop condition by writing 0 to the BBSY flag and the SCP bit in ICCR2. The BBSY flag is cleared to 0 on output of the stop condition (rising edge of SDA while SCL is at the high level).
- Writing 1 to the FS bit in SAR clears the BBST flag to 0.

19.8.6 Using the IICRST Bit to Initialize the Registers

- Writing 1 to the IICRST bit sets the SDAO and SCLO bits in ICCR2 to 1.
- Writing 1 to the IICRST bit in master transmit mode or slave transmit mode sets the TDRE flag in ICSR to 1.
- During a reset due to the IICRST bit being set to 1, writing to the BBSY flag and the SCP and SDAO bits is invalid.
- Even during a reset due to the IICRST bit being set to 1, the input of a start (falling edge of SDA while SCL is at the high level) or stop (rising edge of SDA while SCL is at the high level) condition on SCL and SDA causes the BBSY flag to be set to 1 or cleared to 0, respectively.

19.8.7 Operation of I^2C Bus Interface 3 while ICE = 0

Writing 0 to the ICE bit in ICCR1 disables output on SCL and SDA. However, input on SCL and SDA remains valid. This module operates in accord with the signals input on SCL and SDA.

19.8.8 Note on Master Transmit Mode

When the ACKE bit is set to 1 in master transmit mode, issue a stop condition after confirming the falling edge of the 9th clock of SCL.

20.5 Interrupt Sources and DMAC or DTC Transfer Requests

The A/D converter generates A/D conversion end interrupts (ADI). An ADI interrupt generation is enabled when the ADIE bit in ADCR is set to 1. The DMAC or DTC can be activated by the DMAC or DTC setting when an ADI interrupt is generated. At this time, no interrupt to the CPU is generated. When the DMAC or DTC is activated by an ADI interrupt, the ADF bit in ADSR is automatically cleared at the data transfer by the DMAC or DTC.

Table 20.7 AD Interrupt Sources

A/D Converter Module	Name	DMAC Activation Request	DTC Activation Request
A/D converter module 0	ADI0	Available	Available
A/D converter module 1	ADI1	Not available	Available

24.3.3 USB Interrupt Flag Register 2 (USBIFR2)

Together with USB interrupt flag registers 0, 1, 3, and 4 (USBIFR0, USBIFR1, USBIFR3, and USBIFR4), USBIFR2 indicates interrupt status information required by the application. When an interrupt occurs, the corresponding bit is set to 1 and an interrupt request is sent to the CPU according to the combination with the USB interrupt enable register 2 (USBIER2). Clearing is performed by writing 0 to the bit to be cleared, and 1 to the other bits. However, EP1FULL, EP2ALLEMP, and EP2EMPTY are status bits, and cannot be cleared.

Bit:	7	6	5	4	3	2	1	0
	-	-	EP3 TR	EP3 TS	EP2 TR	EP2 EMPTY	EP2 ALLEMP	EP1 FULL
Initial value:	0	0	0	0	0	1	1	0
R/W:	R	R	R/(W)*	R/(W)*	R/(W)*	R	R	R

Note: * Only 0 can be written to clear the flag.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	EP3TR	0	R/(W)*	EP3 Transfer Request This bit is set to 1 if there is no valid transmit data in the FIFO buffer when an IN token for endpoint 3 is received from the host. A NACK handshake is returned to the host until data is written to the FIFO buffer and packet transmission is enabled.
4	EP3TS	0	R/(W)**	EP3 Transmit Complete This bit is set to 1 when data is transmitted to the host from endpoint 3 and an ACK handshake is returned.
3	EP2TR	0	R/(W)*	EP2 Transfer Request This bit is set to 1 if there is no valid transmit data in the FIFO buffer when an IN token for endpoint 2 is received from the host. A NACK handshake is returned to the host until data is written to the FIFO buffer and packet transmission is enabled.
2	EP2EMPTY	1	R	EP2 FIFO Empty This bit is set to 1 when at least one of the dual endpoint 2 transmit FIFO buffers is ready for transmit data to be written. EP2EMPTY is a status bit, and cannot be cleared.

27.3.3 Flash Access Status Register (FASTAT)

FASTAT indicates the access error status for the ROM and FLD. In on-chip ROM disabled mode, FASTAT is read as H'00 and writing to it is ignored. If any bit in FASTAT is set to 1, the FCU enters command-locked state (see section 27.9.3, Error Protection). To cancel a command-locked state, set FASTAT to H'10, and then issue a status-clear command to the FCU. FASTAT is initialized by a power-on reset.

Bit:	7	6	5	4	3	2	1	0
	ROMAE	—	—	CMDLK	EEPAE	EEPIFE	EEPRPE	EEPWPE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R	R	R	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * Only 0 can be written to clear the flag after 1 is read.

Bit	Bit Name	Initial Value	R/W	Description
7	ROMAE	0	R/(W)*	Access Error Indicates whether or not a ROM access error has been generated. If this bit becomes 1, the ILGLERR bit in FSTATR0 is set to 1 and the FCU enters a command-locked state. 0: No ROM access error has occurred. 1: A ROM access error has occurred. [Setting conditions] • An access command is issued to ROM program/erase addresses H'80800000 to H'808FFFFF while the FENTRY0 bit in FENTRYR is 1 in ROM P/E normal mode. • An access command is issued to ROM program/erase addresses H'80800000 to H'808FFFFF while the FENTRY0 bit in FENTRYR is 0. • A read access command is issued to ROM read addresses H'00000000 to H'000FFFFF while the FENTRYR register value is not H'0000. • A block erase, program, or lock bit program command is issued while the user boot MAT is selected.

Table 28.8 shows the correlation between each FCU mode/state and its acceptable commands. When an unacceptable command is issued, the FCU enters the command-locked state (see section 28.7.3, Error Protection).

To make sure that the FCU accepts a command, enter the mode in which the FCU can accept the target command, check the FRDY, ILGLERR, ERSERR, and PRGERR bit values in FSTATR0, and the FCUERR bit values in FSTATR1, and then issue the target FCU command. The CMDLK bit in FASTAT holds a value obtained by logical ORing the ILGLERR, ERSERR, and PRGERR bit values in FSTATR0 and the FCUERR bit values in the FSTATR1. Therefore the FCU's error occurrence state can be checked by reading the CMDLK bit. In table 28.8, the CMDLK bit is used as the bit to indicate the error occurrence state. The FRDY bit of FSTATR0 is 0 during the programming/erasure, programming/erasure suspension, and blank check processes. While the FRDY bit is 0, the P/E suspend command can be accepted only when the SUSRDY bit in FSTATR0 is 1.

Table 28.8 includes 0 and 1 in single cells of the ERSSPD, PRGSPD, and FRDY bit rows for the sake of simplification. The ERSSPD bits 1 and 0 indicate the erasure suspension and programming suspension processes, respectively. The PRGSPD bits 1 and 0 indicate the programming suspension and erasure suspension processes, respectively. The FRDY bit value can be either 1 or 0, which is a value held by the bit prior to a transition to the command lock state.

32.3 Register States in Each Operating Mode

Module Name	Register	Power-on Reset	Manual Reset	Software Standby	Module Standby	Sleep
CPG	FRQCR	Initialized*[1]	Retained	Retained	—	Retained
	MCLKCR	Initialized	Retained	Retained	—	Retained
	ACLKCR	Initialized	Retained	Retained	—	Retained
	OSCCR	Initialized	Retained	Retained	—	Retained
INTC	ICR0	Initialized	Retained	Retained	—	Retained
	ICR1	Initialized	Retained	Retained	—	Retained
	IRQRR	Initialized	Retained	Retained	—	Retained
	IBCR	Initialized	Retained	Retained	—	Retained
	IBNR	Initialized	Retained*[2]	Retained	—	Retained
	IPR01	Initialized	Retained	Retained	—	Retained
	IPR02	Initialized	Retained	Retained	—	Retained
	IPR05	Initialized	Retained	Retained	—	Retained
	IPR06	Initialized	Retained	Retained	—	Retained
	IPR07	Initialized	Retained	Retained	—	Retained
	IPR08	Initialized	Retained	Retained	—	Retained
	IPR09	Initialized	Retained	Retained	—	Retained
	IPR10	Initialized	Retained	Retained	—	Retained
	IPR11	Initialized	Retained	Retained	—	Retained
	IPR12	Initialized	Retained	Retained	—	Retained
	IPR13	Initialized	Retained	Retained	—	Retained
	IPR14	Initialized	Retained	Retained	—	Retained
	IPR15	Initialized	Retained	Retained	—	Retained
	IPR16	Initialized	Retained	Retained	—	Retained
	IPR17	Initialized	Retained	Retained	—	Retained
	IPR18	Initialized	Retained	Retained	—	Retained
	IPR19	Initialized	Retained	Retained	—	Retained
	USDTENDRR	Initialized	Retained	Retained	—	Retained

33.3.3 Bus Timing

Table 33.7 Bus Timing

Conditions: $V_{cc}Q = PLLV_{cc} = DrV_{cc} = 3.0$ to 3.6 V, $AV_{cc} = AVREF = 4.5$ V to 5.5 V,
$V_{ss} = PLLV_{ss} = DrV_{ss} = AVREFVSS = AV_{ss} = 0$ V,
Ta = –40°C to +85°C (Industrial specifications)

		Bϕ = 50 MHz*[1]			
Item	**Symbol**	**Min.**	**Max.**	**Unit**	**Figure**
Address delay time 1	t_{AD1}	1	18	ns	Figures 33.10 to 33.34
Address delay time 2	t_{AD2}	$1/2t_{cyc} + 1$	$1/2t_{cyc} + 18$	ns	Figure 33.17
Address delay time 3	t_{AD3}	$1/2t_{cyc} + 1$	$1/2t_{cyc} + 18$	ns	Figures 33.35, 33.36
Address setup time	t_{AS}	0	—	ns	Figures 33.10 to 33.13, 33.17
Address hold time	t_{AH}	0	—	ns	Figures 33.10 to 33.13
$\overline{BS}$ delay time	t_{BSD}	—	18	ns	Figures 33.10 to 33.31, 33.35
$\overline{CS}$ delay time 1	t_{CSD1}	1	18	ns	Figures 33.10 to 33.34
$\overline{CS}$ delay time 2	t_{CSD2}	$1/2t_{cyc} + 1$	$1/2t_{cyc} + 18$	ns	Figures 33.35, 33.36
$\overline{CS}$ setup time	t_{CSS}	0	—	ns	Figures 33.10 to 33.13
$\overline{CS}$ hold time	t_{CSH}	0	—	ns	Figures 33.10 to 33.13
Read write delay time 1	t_{RWD1}	1	18	ns	Figures 33.10 to 33.34
Read write delay time 2	t_{RWD2}	$1/2t_{cyc} + 1$	$1/2t_{cyc} + 18$	ns	Figures 33.35, 33.36
Read strobe delay time	t_{RSD}	$1/2t_{cyc} + 1$	$1/2t_{cyc} + 18$	ns	Figures 33.10 to 33.14, 33.17
Read data setup time 1	t_{RDS1}	$1/2t_{cyc} + 14$	—	ns	Figures 33.10 to 33.14, 33.16
Read data setup time 2	t_{RDS2}	14	—	ns	Figures 33.18 to 33.21, 33.26 to 33.28
Read data setup time 3	t_{RDS3}	$1/2t_{cyc} + 14$	—	ns	Figure 33.17
Read data setup time 4	t_{RDS4}	$1/2t_{cyc} + 14$	—	ns	Figure 33.35

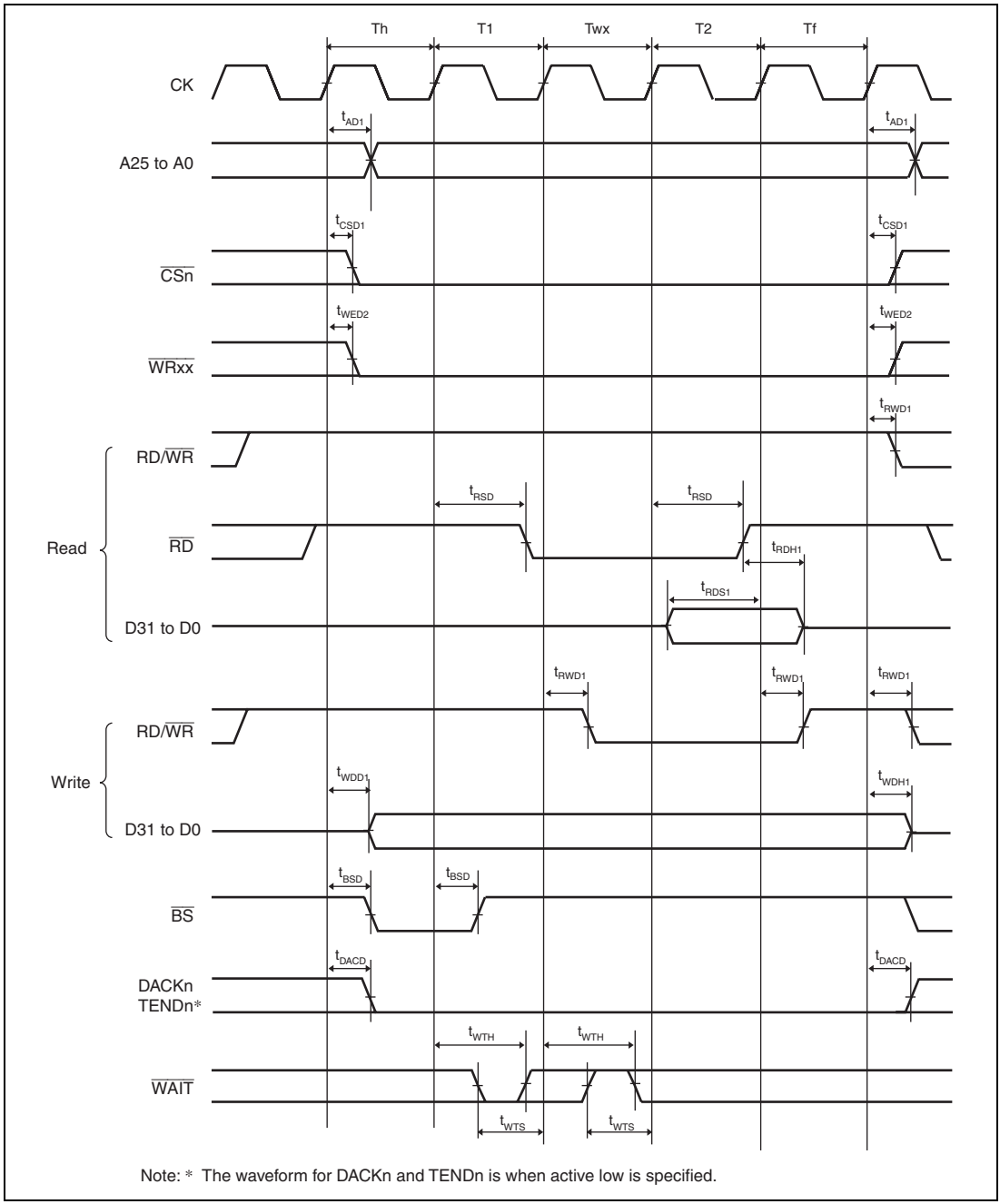
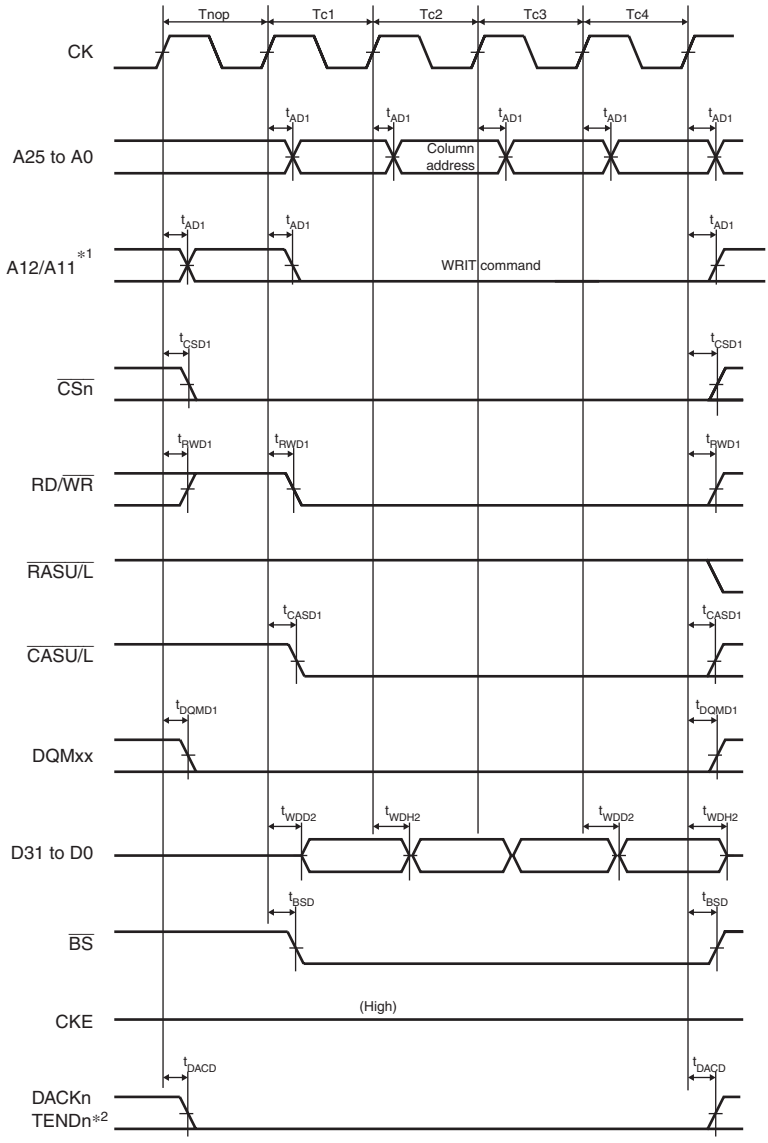


Figure 33.16 Bus Cycle of SRAM with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, One Asynchronous External Wait Cycle, BAS = 1 (Write Cycle WE Control))



Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 33.30 Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Bank Active Mode: WRITE Command, Same Row Address, WTRCD = 0 Cycle, TRWL = 0 Cycle)

33.3.16 I/O Port Timing

Table 33.20 I/O Port Timing

Conditions: $V_{CC}Q = PLLV_{CC} = DrV_{CC} = 3.0$ to 3.6 V, $AV_{CC} = AVREF = 4.5$ to 5.5V,
$V_{SS} = PLLV_{SS} = DrV_{SS} = AVREFVSS = AV_{SS} = 0$ V,
Ta = –40°C to +85°C (Industrial specifications)

Item	Symbol	Min.	Max.	Unit	Figure
Output data delay time	t_{PORTD}	—	50	ns	Figure 33.57
Input data setup time	t_{PORTS}	20	—		
Input data hold time	t_{PORTH}	20	—		

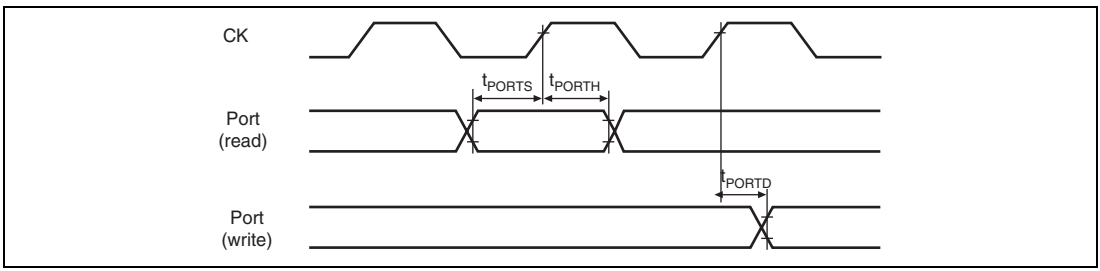


Figure 33.57 I/O Port Timing

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>Table 9.17 Relationship between Access Size and Number of Bursts</td><td>342</td><td>Added
<table>
<tr><th>Bus Width</th><th>Access Size</th><th>Number of Bursts</th></tr>
<tr><td>16 bits</td><td>8 bits</td><td>1</td></tr>
<tr><td></td><td>16 bits</td><td>1</td></tr>
<tr><td></td><td>32 bits</td><td>2</td></tr>
<tr><td></td><td>16 bytes</td><td>8</td></tr>
<tr><td>32 bits</td><td>8 bits</td><td>1</td></tr>
<tr><td></td><td>16 bits</td><td>1</td></tr>
<tr><td></td><td>32 bits</td><td>1</td></tr>
<tr><td></td><td>16 bytes</td><td>4</td></tr>
</table></td></tr>
<tr><td>Figure 9.18 Burst Read Basic Timing (CAS Latency 1, Auto-Precharge)
to
Figure 9.25 Burst Read Timing (Bank Active, Different Row Addresses in the Same Bank, CAS Latency 1),
Figure 9.27 Single Write Timing (Bank Active, Same Row Addresses in the Same Bank)
to
Figure 9.36 Burst ROM Access Timing (Clock Asynchronous) (Bus Width = 32 Bits, 16-Byte Transfer (Number of Burst 4), Wait Cycles Inserted in First Access = 2, Wait Cycles Inserted in Second and Subsequent Access Cycles = 1)</td><td>343
to
352
354
to
371</td><td>Amended
D31 to D0</td></tr>
</table>