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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, I²C, SCI, SPI, USB
Peripherals	DMA, PWM, WDT
Number of I/O	112
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f72165adfp-v1

1.4 Pin Functions

Table 1.2 lists functions of each pin.

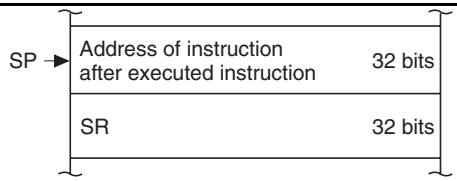
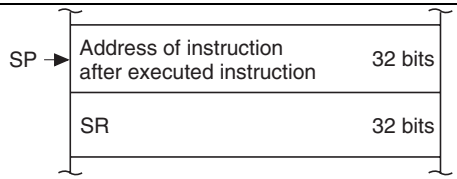
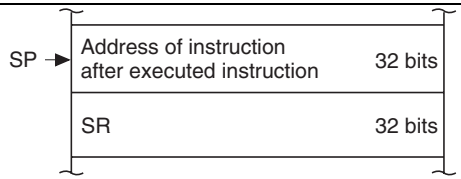
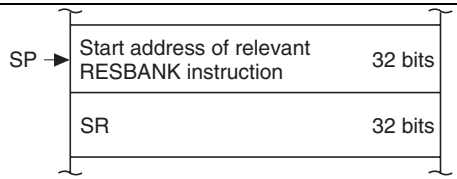
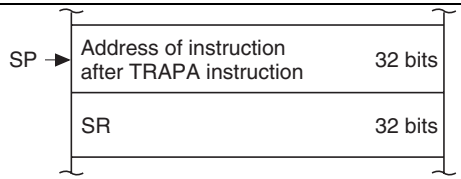
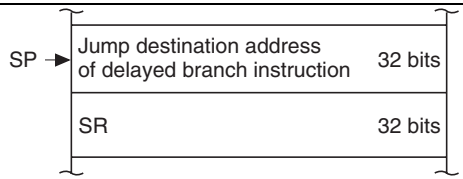
Table 1.2 Pin Functions

Classification	Symbol	I/O	Name	Function
Power supply	V_{CL}	Input	Internal step-down power supply	External capacitance pins for internal step-down power supply. All the V_{CL} pins must be connected to the V_{SS} pins via a 0.1-μF capacitor (should be placed close to the pins). The system power supply must not be directly connected to the V_{CL} pins.
	V_{SS}	Input	Ground	Ground pins. All the V_{SS} pins must be connected to the system power supply (0 V). This LSI does not operate correctly if there is a pin left open.
	$V_{CC}Q$	Input	Power supply	Power supply pins. All the $V_{CC}Q$ pins must be connected to the system power supply. This LSI does not operate if there is a pin left open.
	$PLLV_{CC}$	Input	PLL power supply	Power supply for the on-chip PLL oscillator. Apply the same electric potential as that on the $V_{CC}Q$ pin.
	$PLLV_{SS}$	Input	Ground for PLL	Ground pin for the on-chip PLL oscillator.
Clock	EXTAL	Input	External clock	Connected to a crystal resonator. An external clock signal may also be input to the EXTAL pin.
	XTAL	Output	Crystal	Connected to a crystal resonator.
	USBEXTAL	Input	Crystal for USB	Connected to a resonator for the USB.
	USBXTAL	Output	Crystal for USB	Connected to a resonator for the USB.
	CK	Output	System clock	Supplies the system clock to external devices.

5.8 Stack Status after Exception Handling Ends

The status of the stack after exception handling ends is as shown in table 5.11.

Table 5.11 Stack Status After Exception Handling Ends

Exception Type	Stack Status
Address error	
Interrupt	
Register bank error (overflow) FPU exception	
Register bank error (underflow)	
Trap instruction	
Slot illegal instruction	

6.10.4 Notes on Canceling Software Standby Mode with an IRQx Interrupt Request

When canceling software standby mode using an IRQx interrupt request, change the IRQ sense select setting of ICRx in a state in which no IRQx interrupt requests are generated and clear the IRQxF flag in IRQRRx to 0 by the automatic clearing function of the IRQx interrupt processing.

If the IRQxF flag in the IRQ interrupt request register x (IRQRRx) is 1, changing the setting of the IRQ sense select bits in the interrupt control register x (ICRx) or clearing the IRQxF flag in IRQRRx to 0 will clear the relevant IRQx interrupt request but will not clear the software standby cancellation request.

	1st Transfer					2nd Transfer					
Transfer Mode	**CHNE**	**CHNS**	**RCHNE**	**DISEL**	**Transfer Counter**[*1]	**CHNE**	**CHNS**	**RCHNE**	**DISEL**	**Transfer Counter**[*1]	**DTC Transfer**
Repeat	0	—	—	0	—	—	—	—	—	—	Ends at 1st transfer
	0	—	—	1	—	—	—	—	—	—	Ends at 1st transfer Interrupt request to CPU
	1	0	—	—	—	0	—	—	0	—	Ends at 2nd transfer
						0	—	—	1	—	Ends at 2nd transfer Interrupt request to CPU
	1	1	—	0	Not 0	—	—	—	—	—	Ends at 1st transfer
	1	1	—	1	Not 0	—	—	—	—	—	Ends at 1st transfer Interrupt request to CPU
	1	1	0	0	0[*2]	—	—	—	—	—	Ends at 1st transfer
	1	1	0	1	0[*2]	—	—	—	—	—	Ends at 1st transfer Interrupt request to CPU
	1	1	1	—	0[*2]	0	—	—	0	—	Ends at 2nd transfer
						0	—	—	1	—	Ends at 2nd transfer Interrupt request to CPU

Bit	Bit Name	Initial Value	R/W	Description
10 to 7	WR[3:0]	1010	R/W	Number of Read Access Wait Cycles Specify the number of cycles that are necessary for read access. 0000: No cycle 0001: 1 cycle 0010: 2 cycles 0011: 3 cycles 0100: 4 cycles 0101: 5 cycles 0110: 6 cycles 0111: 8 cycles 1000: 10 cycles 1001: 12 cycles 1010: 14 cycles 1011: 18 cycles 1100: 24 cycles 1101: Reserved (setting prohibited) 1110: Reserved (setting prohibited) 1111: Reserved (setting prohibited)
6	WM	0	R/W	External Wait Mask Specification Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access wait cycle is 0. 0: External wait input is valid 1: External wait input is ignored
5 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
11	DTBST	0	R/W	DTC Burst Enable Selects whether the DTC continues operation without releasing the bus when multiple DTC activation requests are generated. 0: The DTC releases the bus every time a DTC activation request has been processed. 1: The DTC continues operation without releasing the bus until all DTC activation requests have been processed. Notes: When this bit is set to 1, the following restrictions apply. 1. Clock setting through the frequency control register (FRQCR) must be Iϕ : Bϕ : Pϕ: Mϕ: Aϕ = 16 : 4 : 4 : 4 : 4, 16 : 4 : 4 : 8 : 4, 8 : 4 : 4 : 4 : 4, or 8 : 4 : 4 : 8 : 4 2. The vector information must be stored in the on-chip ROM or on-chip RAM. 3. The transfer information must be stored in the on-chip RAM. 4. Transfer must be between the on-chip RAM and an on-chip peripheral module or between the external memory and an on-chip peripheral module. 5. Do not set the DTBST bit to 1, when the activation source is low-level setting for IRQ7 to IRQ0 and the RRS bit is set to 1.

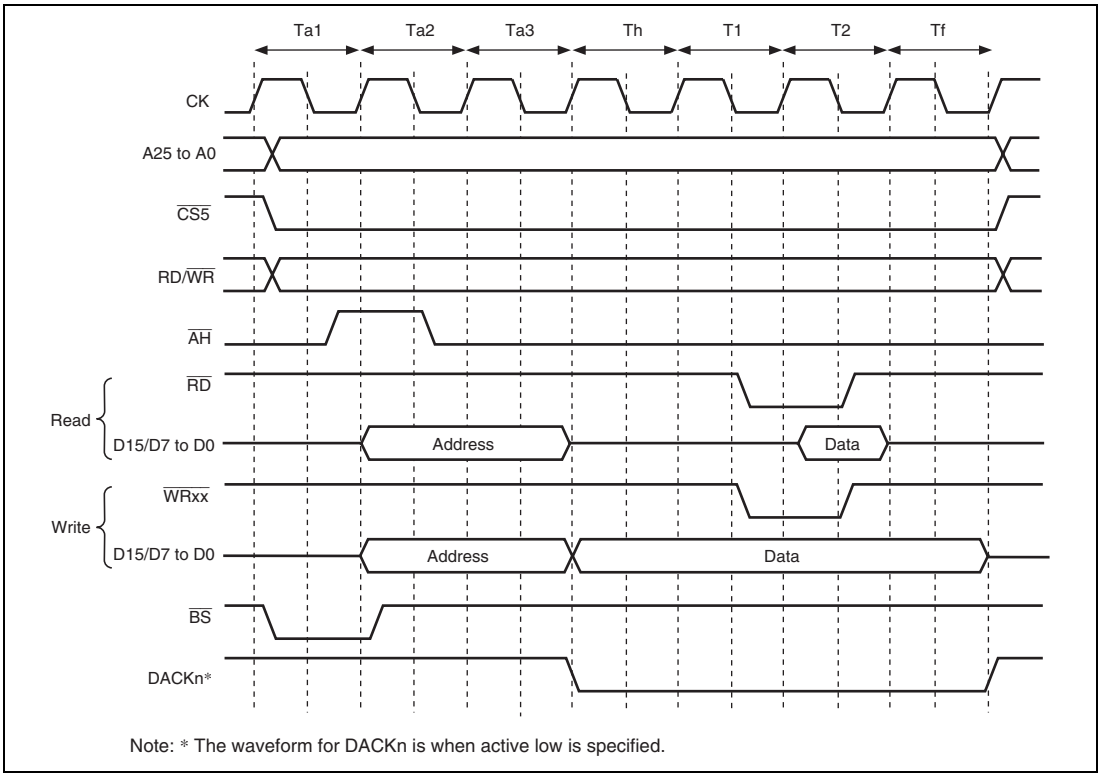


Figure 9.14 Access Timing for MPX Space (Address Cycle No Wait, Assertion Extension Cycle 1.5, Data Cycle No Wait, Negation Extension Cycle 1.5)

Table 9.20 Relationship between Bus Width, Access Size, and Number of Bursts

Bus Width	Access Size	CSnWCR. BST[1:0] Bits	Number of Bursts	Access Count
8 bits	8 bits	Not affected	1	1
	16 bits	Not affected	2	1
	32 bits	Not affected	4	1
	16 bytes*2	x0	16	1
		10	4	4
16 bits	8 bits	Not affected	1	1
	16 bits	Not affected	1	1
	32 bits	Not affected	2	1
	16 bytes*2	00	8	1
		01	2	4
		10*1	4	2
			2, 4, 2	3
32 bits	8 bits	Not affected	1	1
	16 bits	Not affected	1	1
	32 bits	Not affected	1	1
	16 bytes*2	Not affected	4	1

Notes: 1. When the bus width is 16 bits, the access size is 16 bits, and the BST[1:0] bits in CSnWCR are 10, the number of bursts and access count depend on the access start address. At address H'xxx0 or H'xxx8, 4-4 burst access is performed. At address H'xxx4 or H'xxxC, 2-4-2 burst access is performed.

2. Only the DMAC is capable of transfer with 16 bytes as the unit of access. The maximum unit of access for the DTC, E-DMAC, and CPU is 32 bits.

13.4 Operation

Table 13.4 shows the target pins for high-impedance control and conditions to place the pins in high-impedance state.

Table 13.4 Target Pins and Conditions for High-Impedance Control

Pins	Conditions	Detailed Conditions
MTU2 high-current pins (PE9/TIOC3B and PE11/TIOC3D)	Input level detection, output level comparison, or SPOER setting	MTU2P1CZE ((POE3F+POE2F+POE1F+POE0F) + (OSF1 • OCE1) + (MTU2CH34HIZ))
MTU2 high-current pins (PE12/TIOC4A and PE14/TIOC4C)	Input level detection, output level comparison, or SPOER setting	MTU2P2CZE ((POE3F+POE2F+POE1F+POE0F) + (OSF1 • OCE1) + (MTU2CH34HIZ))
MTU2 high-current pins (PE13/TIOC4B and PE15/TIOC4D)	Input level detection, output level comparison, or SPOER setting	MTU2P3CZE ((POE3F+POE2F+POE1F+POE0F) + (OSF1 • OCE1) + (MTU2CH34HIZ))
MTU2S high-current pins (PE5/TIOC3BS and PE6/TIOC3DS)	Input level detection, output level comparison, or SPOER setting	MTU2SP1CZE (POE4F + (OSF2 • OCE2) + (MTU2SHIZ))
MTU2S high-current pins (PE0/TIOC4A and PE2/TIOC4CS)	Input level detection, output level comparison, or SPOER setting	MTU2SP2CZE (POE4F + (OSF2 • OCE2) + (MTU2SHIZ))
MTU2S high-current pins (PE1/TIOC4BS and PE3/TIOC4DS)	Input level detection, output level comparison, or SPOER setting	MTU2SP3CZE (POE4F + (OSF2 • OCE2) + (MTU2SHIZ))
MTU2S high-current pins (PD10/TIOC3BS and PD11/TIOC3DS)	Input level detection, output level comparison, or SPOER setting	MTU2SP4CZE (POE4F +(OSF2 • OCE2) + (MTU2SHIZ))
MTU2S high-current pins (PD12/TIOC4AS and PD14/TIOC4CS)	Input level detection, output level comparison, or SPOER setting	MTU2SP5CZE (POE4F + (OSF2 • OCE2) + (MTU2SHIZ))
MTU2S high-current pins (PD13/TIOC4BS and PD15/TIOC4DS)	Input level detection, output level comparison, or SPOER setting	MTU2SP6CZE (POE4F + (OSF2 • OCE2) + (MTU2SHIZ))
MTU2S high-current pins (PD29/TIOC3BS and PD28/TIOC3DS)	Input level detection, output level comparison, or SPOER setting	MTU2SP7CZE (POE4F + (OSF2 • OCE2) + (MTU2SHIZ))

Bit	Bit Name	Initial Value	R/W	Description
5	RSTS	0	R/W	Reset Select Selects the type of reset when the WTCNT overflows in watchdog timer mode. In interval timer mode, this setting is ignored. 0: Power-on reset 1: Manual reset
4 to 0	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.

15.3.4 Notes on Register Access

The watchdog timer counter (WTCNT), watchdog timer control/status register (WTCSR), and watchdog reset control/status register (WRCSR) are more difficult to write to than other registers. The procedures for reading or writing to these registers are given below.

(1) Writing to WTCNT and WTCSR

These registers must be written by a word transfer instruction. They cannot be written by a byte or longword transfer instruction.

When writing to WTCNT, set the upper byte to H'5A and transfer the lower byte as the write data, as shown in figure 15.2. When writing to WTCSR, set the upper byte to H'A5 and transfer the lower byte as the write data. This transfer procedure writes the lower byte data to WTCNT or WTCSR.

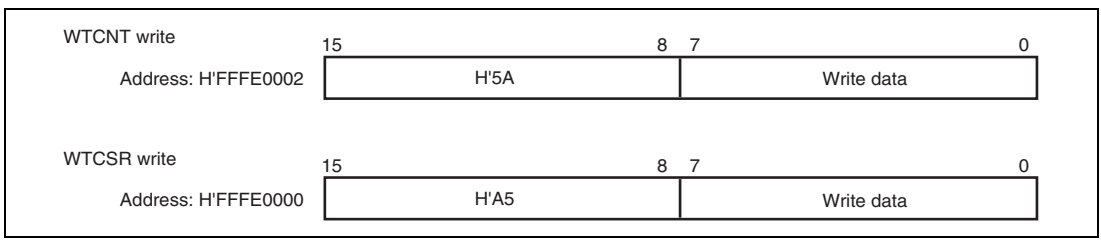
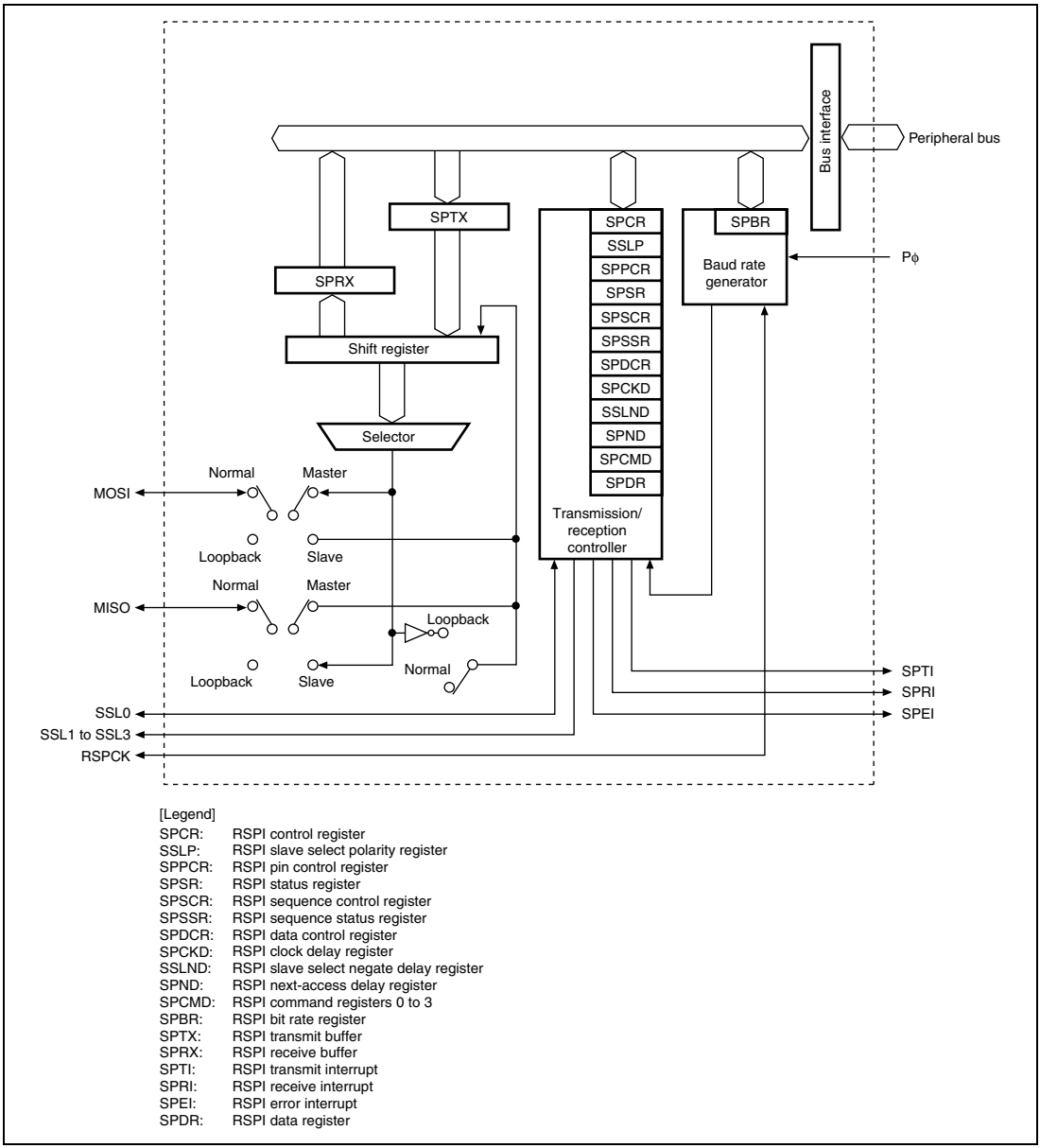


Figure 15.2 Writing to WTCNT and WTCSR



[Legend]

SPCR:	RSPI control register
SSLP:	RSPI slave select polarity register
SPPCR:	RSPI pin control register
SPSR:	RSPI status register
SPSCR:	RSPI sequence control register
SPSSR:	RSPI sequence status register
SPDCR:	RSPI data control register
SPCKD:	RSPI clock delay register
SSLND:	RSPI slave select negate delay register
SPND:	RSPI next-access delay register
SPCMD:	RSPI command registers 0 to 3
SPBR:	RSPI bit rate register
SPTX:	RSPI transmit buffer
SPRX:	RSPI receive buffer
SPTI:	RSPI transmit interrupt
SPRI:	RSPI receive interrupt
SPEI:	RSPI error interrupt
SPDR:	RSPI data register

Figure 18.1 Block Diagram of RSPI

3. If the serial transfer terminates with the OVRF bit being 1 (an overrun error), the RSPI keeps the SPRF bit at 0 and does not update it. Likewise, the RSPI does not copy the data in the shift register to the receive buffer. When in master mode, the RSPI does not update bits SPECM1 and SPECM0 of SPSSR. If, in an overrun error state, the RSPI does not copy the received data from the shift register to the receive buffer, upon termination of the serial transfer, the RSPI determines that the shift register is empty; in this manner, data transfer is enabled from the transmit buffer to the shift register.
4. If the CPU writes a 0 to the OVRF bit after reading SPSR when the OVRF bit is 1, the RSPI clears the OVRF bit.

The occurrence of an overrun can be checked either by reading SPSR or by using an RSPI error interrupt and reading SPSR. When using an RSPI error interrupt, set the SPEIE bit in the RSPI control register (SPCR) to 1. When executing a serial transfer without using an RSPI error interrupt, measures should be taken to ensure the early detection of overrun errors, such as reading SPSR immediately after SPDR is read. When the RSPI is run in master mode, the pointer value to SPCMD can be checked by reading bits SPECM2 to SPECM0 of SPSSR.

If an overrun error occurs and the OVRF bit is set to 1, normal reception operations cannot be performed until such time as the OVRF bit is cleared. The OVRF bit is cleared to 0 under the following conditions:

- After reading SPSR in a condition in which the OVRF bit is set to 1, the CPU writes a 0 to the OVRF bit.
- System reset

24.3.39 USB Trigger Register 3 (USBTRG3)

USBTRG3 generates one-shot triggers to control the transmit/receive sequence for each endpoint.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	EP6 PKTE	EP5 PKTE	EP4 RDFN
Initial value:	0	0	0	0	0	0	0	0
R/W:	-	-	-	-	-	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	—	Reserved The write value should always be 0.
2	EP9PKTE	0	W	EP9 Packet Enable After one packet of data has been written to the endpoint 9 transmit FIFO buffer, the transmit data is fixed by writing 1 to this bit.
1	EP8PKTE	0	W	EP8 Packet Enable After one packet of data has been written to the endpoint 8 transmit FIFO buffer, the transmit data is fixed by writing 1 to this bit.
0	EP7RDFN	0	W	EP7 Read Complete Write 1 to this bit after one packet of data has been read from the endpoint 7 receive FIFO buffer. Writing 1 to this bit initializes the FIFO that was read, enabling the next packet to be received.

Table 24.5 USBTRNTREG0 Setting and Pin Output State

Pin Input	Register Setting				Pin Output State	
VBUS	PTSTE	txenl	txenl	txdata	USD+	USD-
0	×	×	×	×	Hi-Z	Hi-Z
1	0	×	×	×	—	—
1	1	0	0	0	0	1
1	1	0	0	1	1	0
1	1	0	1	×	0	0
1	1	1	×	×	Hi-Z	Hi-Z

[Legend]

×: Don't care

—: Uncontrollable pin state in normal operation, depending on the USB operating status and port settings.

Section 25 Ethernet Controller (EtherC) (SH7216A, SH7214A, SH7216G, and SH7214G only)

This LSI has an on-chip Ethernet controller (EtherC) conforming to the Ethernet or the IEEE802.3 MAC (Media Access Control) layer standard. Connecting a physical-layer LSI (PHY-LSI) conforming to this standard enables the EtherC to transmit and receive Ethernet/IEEE802.3 frames. The EtherC has one MAC layer interface port. The EtherC is connected to the Ethernet Direct Memory Access Controller (E-DMAC) for Ethernet controller inside the LSI, and carries out high-speed data transfer to and from the memory.

Figure 25.1 shows a configuration of the EtherC.

25.1 Features

- Transmission and reception of Ethernet/IEEE802.3 frames
- Supports 10/100 Mbps data transfer
- Supports full-duplex and half-duplex modes
- Conforms to IEEE802.3u standard MII (Media Independent Interface)
- Magic Packet detection and Wake-On-LAN (WOL) signal output
- Conforms to IEEE802.3x flow control

26.2.14 Receive FIFO Overflow Counter Register (RFOCR)

RFOCR is a register that indicates the number of overflows having occurred in the receive FIFO. The counter is cleared to 0 by writing any value to this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OVER[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	OVER[15:0]	All 0	R/W	Receive FIFO Overflow Count Indicates the count of overflows having occurred in the receive FIFO. The counter stops when the count value reaches H'FFFF.

If the host has sent an undefined command, this LSI returns a response indicating a command error in the format shown below. The command field holds the first byte of the undefined command sent from the host.

Error response	H'80	Command

In inquiry/selection host command wait state, send selection commands from the host in the order of device selection, clock mode selection, and new bit rate selection to set up this LSI according to the responses to inquiry commands. Note that the supported device inquiry and clock mode inquiry commands are the only inquiry commands that can be sent before the clock mode selection command; other inquiry commands must not be issued before the clock mode selection command. If commands are issued in an incorrect order, this LSI returns a response indicating a command error. Figure 27.11 shows an example of the procedure to use inquiry/selection host commands.

28.8.5 Reset during Programming or Erasure

To reset the FCU by setting the FRESET bit in the FRESETR register during programming or erasure, hold the FCU in the reset state for a period of t_{RESW2} (see section 33, Electrical Characteristics). Since a high voltage is applied to the FLD during programming and erasure, the FCU has to be held in the reset state long enough to ensure that the voltage applied to the memory unit has dropped. Do not read from the FLD while the FCU is in the reset state.

When a power-on reset is generated by asserting the $\overline{RES}$ pin during programming or erasure of the flash memory, hold the reset state for a period of t_{RESW2} (see section 33, Electrical Characteristics). In a power-on reset, not only does the voltage applied to the memory unit have to drop, but the power supply for the FLD and its internal circuitry also have to be initialized. Thus, the reset state must be maintained over a longer period than in the case of resetting the FCU.

When executing a power-on reset by asserting the $\overline{RES}$ pin or the FCU reset with the FRESET bit set in FRESETR during programming/erasure, all data including a lock bit of a programming/erasure target area are undefined.

While programming or erasure is performed, do not generate an internal reset caused by WDT counter overflow. A reset caused by WDT cannot ensure a sufficient time required for voltage drop for the memory unit, initialization of the power supply for the FLD, or initialization of its internal circuit.

28.8.6 Suspension by Programming/Erasure Suspension

When suspending programming/erasure processing with the programming/erasure suspend command, make sure to complete the operations with the resume command.

28.8.7 Prohibition of Additional Programming

One area cannot be programmed twice in succession. To program an area that has already been programmed, be sure to erase the area before reprogramming.

28.8.8 Program for Reading

Execute program code for reading the FLD from on-chip RAM or on-chip ROM.

30.3.5 Standby Control Register 5 (STBCR5)

STBCR5 is an 8-bit readable/writable register that controls the operation of modules in power-down modes. STBCR5 is initialized to H'FF by a power-on reset but retains its previous value by a manual reset or in software standby mode. Only byte access is possible.

Bit:	7	6	5	4	3	2	1	0
	MSTP57	MSTP56	MSTP55	-	MSTP53	MSTP52	-	MSTP50
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R	R/W	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	MSTP57	1	R/W	Module Stop 57 When the MSTP57 bit is set to 1, the supply of the clock to the SCI0 is halted. 0: SCI0 runs. 1: Clock supply to SCI0 halted.
6	MSTP56	1	R/W	Module Stop 56 When the MSTP56 bit is set to 1, the supply of the clock to the SCI1 is halted. 0: SCI1 runs. 1: Clock supply to SCI1 halted.
5	MSTP55	1	R/W	Module Stop 55 When the MSTP55 bit is set to 1, the supply of the clock to the SCI2 is halted. 0: SCI2 runs. 1: Clock supply to SCI2 halted.
4	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.