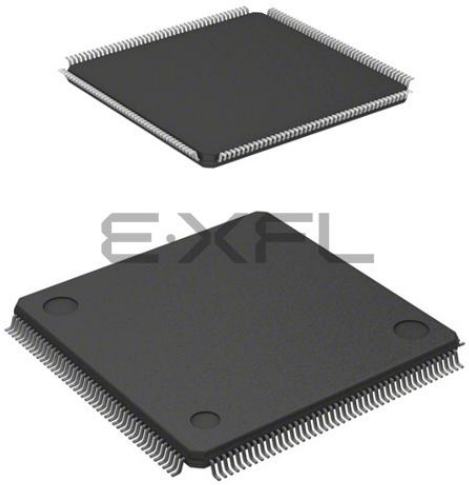
Renesas Electronics America Inc - R5F72165BDFA#V1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, I²C, SCI, SPI, USB
Peripherals	DMA, PWM, WDT
Number of I/O	112
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f72165bdfa-v1

5.5.3 Interrupt Exception Handling

When an interrupt occurs, its priority level is ascertained by the interrupt controller (INTC). NMI is always accepted, but other interrupts are only accepted if they have a priority level higher than the priority level set in the interrupt mask level bits (I3 to I0) of the status register (SR).

When an interrupt is accepted, interrupt exception handling begins. In interrupt exception handling, the CPU fetches the exception service routine start address which corresponds to the accepted interrupt from the exception handling vector table, and saves SR and the program counter (PC) to the stack. In the case of interrupt exception handling other than NMI or UBC with usage of the register banks enabled, general registers R0 to R14, control register GBR, system registers MACH, MACL, and PR, and the vector table address offset of the interrupt exception handling to be executed are saved in the register banks. In the case of exception handling due to an address error, NMI interrupt, UBC interrupt, or instruction, saving is not performed to the register banks. If saving has been performed to all register banks (0 to 14), automatic saving to the stack is performed instead of register bank saving. In this case, an interrupt controller setting must have been made so that register bank overflow exceptions are not accepted (the BOVE bit in IBNR of the INTC is 0). If a setting to accept register bank overflow exceptions has been made (the BOVE bit in IBNR of the INTC is 1), register bank overflow exception occurs. Next, the priority level value of the accepted interrupt is written to the I3 to I0 bits in SR. For NMI, however, the priority level is 16, but the value set in the I3 to I0 bits is H'F (level 15). Then, after jumping to the start address fetched from the exception handling vector table, program execution starts. The jump that occurs is not a delayed branch. See section 6.6, Operation, for further details of interrupt exception handling.

8.5.9 DTC Bus Release Timing

The DTC requests the bus mastership of the internal bus (I bus) to the bus arbiter when an activation request occurs. The DTC releases the bus after a vector read, transfer information read, a single data transfer, or transfer information write-back. The DTC does not release the bus mastership during transfer information read, a single data transfer, or write-back of transfer information.

The bus release timing can be specified through the bus function extending register (BSCEHR). For details see section 9.4.8, Bus Function Extending Register (BSCEHR). The difference in bus release timing according to the register setting is summarized in table 8.11. Settings other than shown in the table are prohibited. The value of BSCEHR must not be modified while the DTC is active.

Figure 8.16 is a timing chart showing an example of bus release timing.

Table 8.11 DTC Bus Release Timing

	Bus Function Extending Register (BSCEHR) Setting		Bus Release Timing (O: Bus must be released; x: Bus is not released)				
						After Write-Back of Transfer Information	
	DTLOCK	DTBST	After Vector Read	After Transfer Information Read	After a Single data Transfer	Normal Transfer	Continuous Transfer
Setting 1	0	0	×	×	×	O	O
Setting 2*1	0	1	×	×	×	O	×
Setting 3*2	1	0	O	O	O	O	O

Notes: 1. The following restrictions apply to setting 2.
- The clock setting through the frequency control register (FRQCR) must be Iϕ : Bϕ : Pϕ : Mϕ : Aϕ = 16 : 4 : 4 : 4 : 4, 16 : 4 : 4 : 8 : 4, 8 : 4 : 4 : 8 : 4, or 8 : 4 : 4 : 4 : 4.
- The vector information must be stored in the flash memory (ROM) or on-chip RAM.
- The transfer information must be stored in the on-chip RAM.
- Transfer must be between the on-chip RAM and an on-chip peripheral module or between the external memory and an on-chip peripheral module.

2. The following restriction applies to setting 3.
- Use the DTPR bit in BSCEHR with this bit set to 0. Setting this bit to 1 is prohibited.

Bit	Bit Name	Initial Value	R/W	Description
10 to 7	WR[3:0]	1010	R/W	Number of Read Access Wait Cycles Specify the number of cycles that are necessary for read access. 0000: No cycle 0001: 1 cycle 0010: 2 cycles 0011: 3 cycles 0100: 4 cycles 0101: 5 cycles 0110: 6 cycles 0111: 8 cycles 1000: 10 cycles 1001: 12 cycles 1010: 14 cycles 1011: 18 cycles 1100: 24 cycles 1101: Reserved (setting prohibited) 1110: Reserved (setting prohibited) 1111: Reserved (setting prohibited)
6	WM	0	R/W	External Wait Mask Specification Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access wait cycle is 0. 0: External wait input is valid 1: External wait input is ignored
5 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	HW[1:0]	00	R/W	Delay Cycles from RD, $\overline{\text{WRxx}}$ Negation to Address, $\overline{\text{CSn}}$ Negation Specify the number of delay cycles from RD and $\overline{\text{WRxx}}$ negation to address and $\overline{\text{CSn}}$ negation. 00: 0.5 cycles 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles

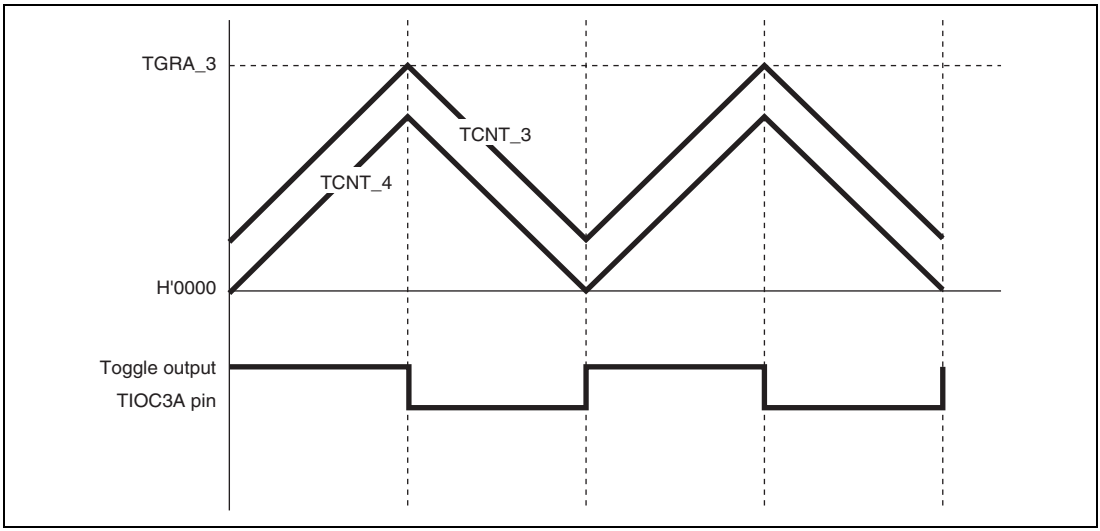


Figure 11.54 Example of Toggle Output Waveform Synchronized with PWM Output

11.7.3 Caution on Period Setting

When counter clearing on compare match is set, TCNT is cleared in the final state in which it matches the TGR value (the point at which the count value matched by TCNT is updated). Consequently, the actual counter frequency is given by the following formula:

- Channel 0 to 4

$$f = \frac{P\phi}{(N + 1)}$$

- Channel 5

$$f = \frac{P\phi}{N}$$

Where f: Counter frequency
Pϕ: Peripheral clock operating frequency
N: TGR set value

11.7.4 Contention between TCNT Write and Clear Operations

If the counter clear signal is generated in the T2 state of a TCNT write cycle, TCNT clearing takes precedence and the TCNT write is not performed.

Figure 11.121 shows the timing in this case.

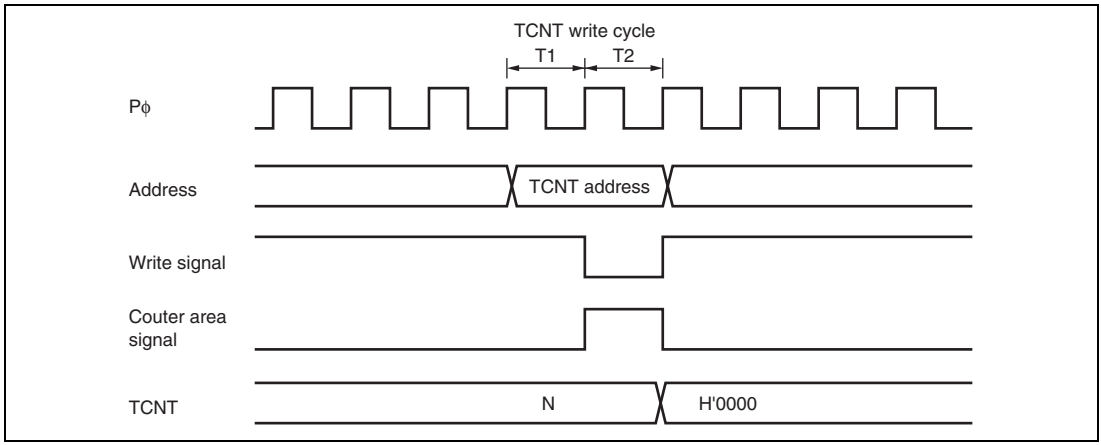


Figure 11.121 Contention between TCNT Write and Clear Operations

Bit	Bit Name	Initial Value	R/W	Description
6	MTU2PB3ZE	0	R/W*	MTU2PB3 High-Impedance Enable Specifies whether to place the PB3/TIOC0C pin for channel 0 in the MTU2 in high-impedance state when either POE8F or MTU2CH0HIZ bit is set to 1. 0: Does not place the pin in high-impedance state 1: Places the pin in high-impedance state
5	MTU2PB2ZE	0	R/W*	MTU2PB2 High-Impedance Enable Specifies whether to place the PB2/TIOC0B pin for channel 0 in the MTU2 in high-impedance state when either POE8F or MTU2CH0HIZ bit is set to 1. 0: Does not place the pin in high-impedance state 1: Places the pin in high-impedance state
4	MTU2PB1ZE	0	R/W*	MTU2PB1 High-Impedance Enable Specifies whether to place the PB1/TIOC0A pin for channel 0 in the MTU2 in high-impedance state when either POE8F or MTU2CH0HIZ bit is set to 1. 0: Does not place the pin in high-impedance state 1: Places the pin in high-impedance state
3	MTU2PE3ZE	0	R/W*	MTU2PE3 High-Impedance Enable Specifies whether to place the PE3/TIOC0D pin for channel 0 in the MTU2 in high-impedance state when either POE8F or MTU2CH0HIZ bit is set to 1. 0: Does not place the pin in high-impedance state 1: Places the pin in high-impedance state
2	MTU2PE2ZE	0	R/W*	MTU2PE2 High-Impedance Enable Specifies whether to place the PE2/TIOC0C pin for channel 0 in the MTU2 in high-impedance state when either POE8F or MTU2CH0HIZ bit is set to 1. 0: Does not place the pin in high-impedance state 1: Places the pin in high-impedance state
1	MTU2PE1ZE	0	R/W*	MTU2PE1 High-Impedance Enable Specifies whether to place the PE1/TIOC0B pin for channel 0 in the MTU2 in high-impedance state when either POE8F or MTU2CH0HIZ bit is set to 1. 0: Does not place the pin in high-impedance state 1: Places the pin in high-impedance state

14.4 Interrupts

14.4.1 Interrupt Sources and DTC/DMAC Transfer Requests

The CMT has channels and each of them to which a different vector address is allocated has a compare match interrupt. When both the interrupt request flag (CMF) and the interrupt enable bit (CMIE) are set to 1, the corresponding interrupt request is output. When the interrupt is used to activate a CPU interrupt, the priority of channels can be changed by the interrupt controller settings. For details, see section 6, Interrupt Controller (INTC).

Clear the CMF bit to 0 by the user exception handling routine. If this operation is not carried out, another interrupt will be generated. The direct memory access controller (DMAC) can be set to be activated when a compare match interrupt is requested. In this case, an interrupt is not issued to the CPU. If the setting to activate the DMAC has not been made, an interrupt request is sent to the CPU. The CMF bit is automatically cleared to 0 when data is transferred by the DMAC.

The data transfer controller (DTC) can be activated by an interrupt request. In this case, the priority between channels is fixed. For details, refer to section 8, Data Transfer Controller (DTC).

Table 14.2 Interrupt Sources

Channel	Interrupt Source	Interrupt Enable Bit	Interrupt Flag	DMAC/DTC Activation	Priority
0	CMI0	CMIE	CMF	Possible	High
1	CMI1	CMIE	CMF	Possible	Low

Bit	Bit Name	Initial Value	R/W	Description
5	RSTS	0	R/W	Reset Select Selects the type of reset when the WTCNT overflows in watchdog timer mode. In interval timer mode, this setting is ignored. 0: Power-on reset 1: Manual reset
4 to 0	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.

15.3.4 Notes on Register Access

The watchdog timer counter (WTCNT), watchdog timer control/status register (WTCSR), and watchdog reset control/status register (WRCSR) are more difficult to write to than other registers. The procedures for reading or writing to these registers are given below.

(1) Writing to WTCNT and WTCSR

These registers must be written by a word transfer instruction. They cannot be written by a byte or longword transfer instruction.

When writing to WTCNT, set the upper byte to H'5A and transfer the lower byte as the write data, as shown in figure 15.2. When writing to WTCSR, set the upper byte to H'A5 and transfer the lower byte as the write data. This transfer procedure writes the lower byte data to WTCNT or WTCSR.

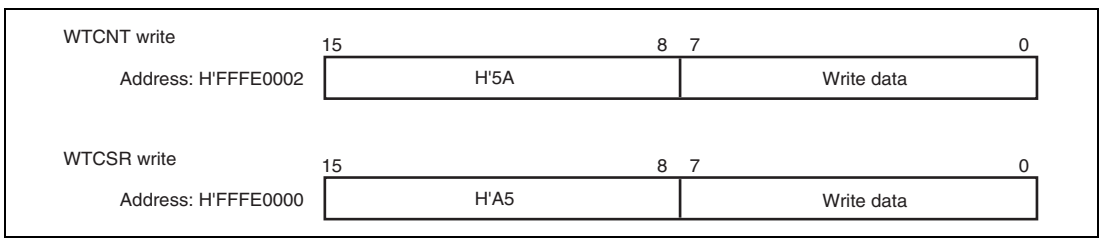


Figure 15.2 Writing to WTCNT and WTCSR

(1) Transmit/Receive Formats

Table 16.16 shows the transfer formats that can be selected in asynchronous mode. Any of 12 transfer formats can be selected according to the SCSMR settings.

Table 16.16 Serial Transfer Formats (Asynchronous Mode)

SCSMR Settings				Serial Transfer Format and Frame Length											
CHR	PE	MP	STOP	1	2	3	4	5	6	7	8	9	10	11	12
0	0	0	0	S	8-bit data								STOP		
0	0	0	1	S	8-bit data								STOP	STOP	
0	1	0	0	S	8-bit data								P	STOP	
0	1	0	1	S	8-bit data								P	STOP	STOP
1	0	0	0	S	7-bit data							STOP			
1	0	0	1	S	7-bit data							STOP	STOP		
1	1	0	0	S	7-bit data							P	STOP		
1	1	0	1	S	7-bit data							P	STOP	STOP	
0	x	1	0	S	8-bit data								MPB	STOP	
0	x	1	1	S	8-bit data								MPB	STOP	STOP
1	x	1	0	S	7-bit data							MPB	STOP		
1	x	1	1	S	7-bit data							MPB	STOP	STOP	

[Legend]
S: Start bit
STOP: Stop bit
P: Parity bit
MPB: Multiprocessor bit
x: Don't care

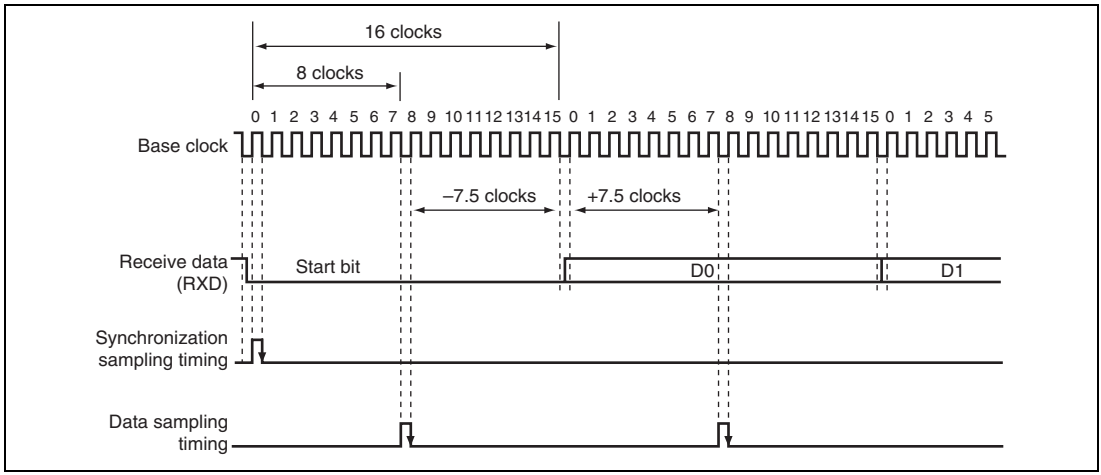


Figure 16.21 Receive Data Sampling Timing in Asynchronous Mode

The receive margin in asynchronous mode can therefore be expressed as shown in equation 1.

Equation 1:

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5)\,F - \frac{|D - 0.5|}{N}(1+F) \right| \times 100\ \%$$

Where: M: Receive margin (%)
N: Ratio of bit rate to clock (N = 16)
D: Clock duty (D = 0 to 1.0)
L: Frame length (L = 9 to 12)
F: Absolute deviation of clock frequency

From equation 1, if F = 0 and D = 0.5, the receive margin is 46.875%, as given by equation 2.

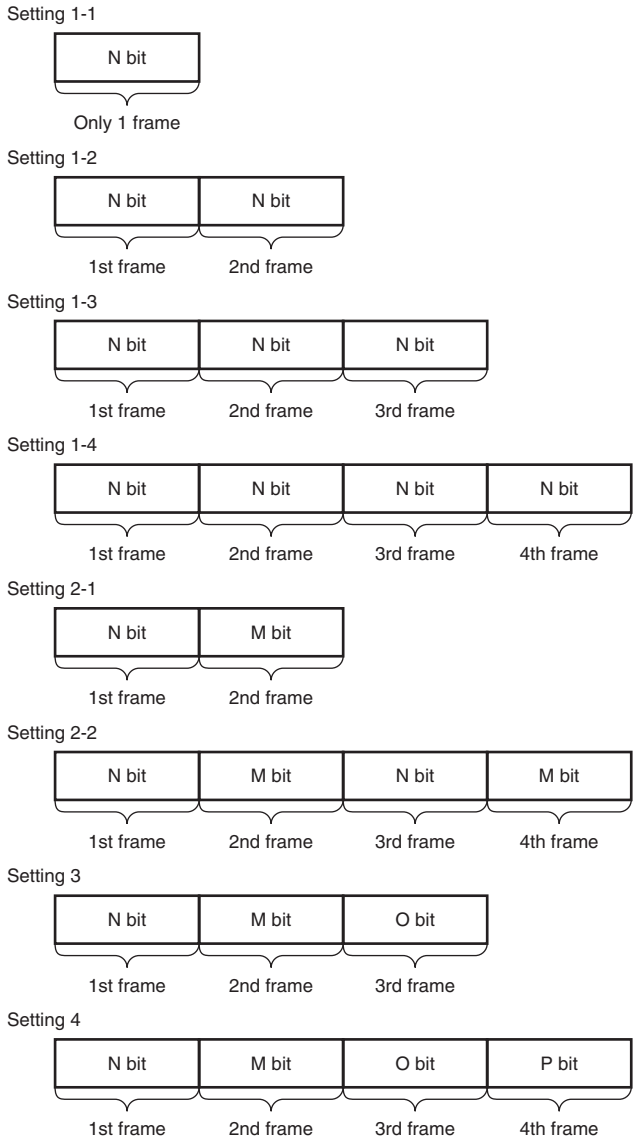
Equation 2:

When D = 0.5 and F = 0:

$$M = (0.5 - 1/(2 \times 16)) \times 100\%$$
$$= 46.875\%$$

This is a theoretical value. A reasonable margin to allow in system designs is 20% to 30%.

Data can be transferred or received at a time upon transmission or reception activation according to the setting combinations, 1-1 to 4, as follows:



19.2 Input/Output Pins

Table 19.1 shows the pin configuration of the I^2C bus interface 3.

Table 19.1 Pin Configuration

Pin Name	Symbol	I/O	Function
Serial clock	SCL	I/O	I^2C serial clock input/output
Serial data	SDA	I/O	I^2C serial data input/output

Figure 19.2 shows an example of I/O pin connections to external circuits.

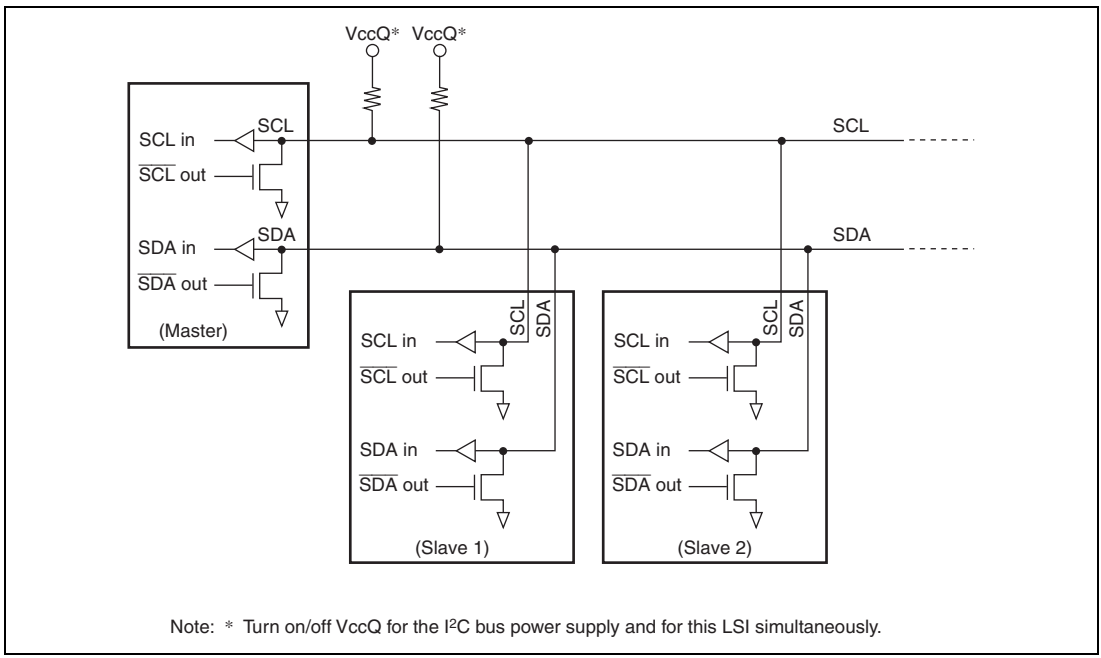


Figure 19.2 External Circuit Connections of I/O Pins

21.5 Interrupt Sources

Table 21.2 lists the RCAN-ET interrupt sources. With the exception of the reset processing interrupt (IRR0) by a power-on reset, these sources can be masked. Masking is implemented using the mailbox interrupt mask register 0 (MBIMR0) and interrupt mask register (IMR). For details on the interrupt vector of each interrupt source, see section 6, Interrupt Controller (INTC).

Table 21.2 RCAN-ET Interrupt Sources

Module	Interrupt	Description	Interrupt Flag	DTC Activation
RCAN-ET	ERS_0	Error Passive Mode (TEC ≥ 128 or REC ≥ 128)	IRR5	Not possible
		Bus Off (TEC ≥ 256)/Bus Off recovery	IRR6	
		Error warning (TEC ≥ 96)	IRR3	
		Error warning (REC ≥ 96)	IRR4	
	OVR_0	Message error detection	IRR13*1	
		Reset/halt/CAN sleep transition	IRR0	
		Overload frame transmission	IRR7	
		Unread message overwrite (overrun)	IRR9	
		Detection of CAN bus operation in CAN sleep mode	IRR12	
	RM0_0*2	Data frame reception	IRR1*3	Possible*4
	RM1_0*2	Remote frame reception	IRR2*3	
	SLE_0	Message transmission/transmission disabled (slot empty)	IRR8	Not possible

Notes: 1. Available only in Test Mode.
2. RM0_0 is an interrupt generated by the remote request pending flag for mailbox 0 (RFPR0[0]) or the data frame receive flag for mailbox 0 (RXPR0[0]). RM1_0 is an interrupt generated by the remote request pending flag for mailbox n (RFPR0[n]) or the data frame receive flag for mailbox n (RXPR0[n]) (n = 1 to 15).
3. IRR1 is a data frame received interrupt flag for mailboxes 0 to 15, and IRR2 is a remote frame request interrupt flag for mailboxes 0 to 15.
4. The DTC can be activated only by the RM0_0 interrupt.

Bit	Bit Name	Initial Value	R/W	Description
0	EP5DMAE*	0	R/W	EP1 DMA/DTC Transfer Enable When this bit is set, DMA/DTC transfer is enabled from the endpoint 1 receive FIFO buffer to the memory. If at least one byte of receive data is remaining in the FIFO buffer, a transfer request is asserted to the DMAC or DTC. During DMA/DTC transfer, when all the received data is read, an EP1 read completion trigger is given. Also, as EP1-related interrupt requests to the CPU are not automatically masked, interrupt requests should be masked as necessary in the USB interrupt enable register.

Note: * To start DMA transfer, set the DME bit in DMAOR before setting this bit.
To start DTC transfer, set the corresponding DTCE bit in DTCER before setting this bit.

Section 25 Ethernet Controller (EtherC) (SH7216A, SH7214A, SH7216G, and SH7214G only)

This LSI has an on-chip Ethernet controller (EtherC) conforming to the Ethernet or the IEEE802.3 MAC (Media Access Control) layer standard. Connecting a physical-layer LSI (PHY-LSI) conforming to this standard enables the EtherC to transmit and receive Ethernet/IEEE802.3 frames. The EtherC has one MAC layer interface port. The EtherC is connected to the Ethernet Direct Memory Access Controller (E-DMAC) for Ethernet controller inside the LSI, and carries out high-speed data transfer to and from the memory.

Figure 25.1 shows a configuration of the EtherC.

25.1 Features

- Transmission and reception of Ethernet/IEEE802.3 frames
- Supports 10/100 Mbps data transfer
- Supports full-duplex and half-duplex modes
- Conforms to IEEE802.3u standard MII (Media Independent Interface)
- Magic Packet detection and Wake-On-LAN (WOL) signal output
- Conforms to IEEE802.3x flow control

26.3 Operation

The E-DMAC, connected to the EtherC, allows efficient transfer of transmit/receive data between the EtherC and memory (buffers) without CPU intervention. The E-DMAC automatically reads the control information referred to as descriptors. The descriptors corresponding to each buffer store buffer pointers and other information. The E-DMAC reads transmit data from the transmit buffer and writes receive data to the receive buffer according to the control information. Arranging such multiple descriptors in a row (i.e., making a descriptor list) allows continuous transmission or reception.

26.3.1 Descriptor Lists and Data Buffers

The communication program creates a transmit descriptor list and a receive descriptor list in a memory space prior to transmission and reception, and sets the start addresses of these lists to the transmit descriptor list start address register and receive descriptor list start address register.

The start addresses of the descriptor lists should be placed on the address boundaries in accordance with the descriptor length specified by the E-DMAC mode register (EDMR). The start address of the transmit buffer can be placed on a longword, word, or byte boundary.

(1) Transmit Descriptor

Figure 26.2 shows the relationship between a transmit descriptor and a transmit buffer. The descriptor can relate one transmit frame to one transmit buffer (single-frame/single-buffer operation) or multiple transmit buffers (single-frame/multi-buffer operation).

When the transmit buffer length (TBL) is to be set to 1 to 16 bytes, the buffer address needs to be placed on a 32-byte boundary. When the transmit buffer length (TBL) is set below 42 bytes, operation cannot be guaranteed.

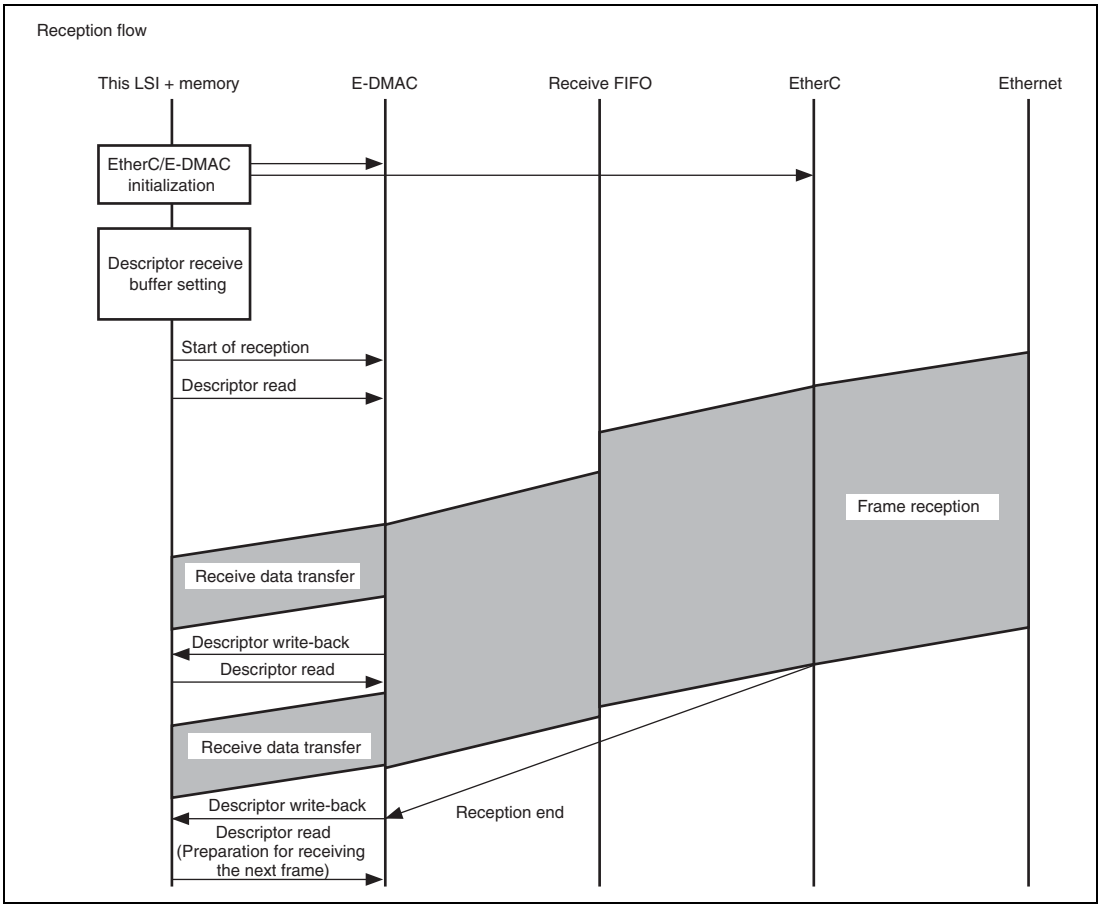


Figure 26.5 Example of Reception Flow

Module Name	Register Name	Abbreviation	Number of Bits	Address	Access Size
POE2	Port output enable control register 1	POECR1	8	H'FFFE500B	8
	Port output enable control register 2	POECR2	16	H'FFFE500C	16
CMT	Compare match timer start register	CMSTR	16	H'FFFEC000	16
	Compare match timer control/ status register_0	CMCSR_0	16	H'FFFEC002	16
	Compare match counter_0	CMCNT_0	16	H'FFFEC004	16
	Compare match constant register_0	CMCOR_0	16	H'FFFEC006	16
	Compare match timer control/ status register_1	CMCSR_1	16	H'FFFEC008	16
	Compare match counter_1	CMCNT_1	16	H'FFFEC00A	16
	Compare match constant register_1	CMCOR_1	16	H'FFFEC00C	16
WDT	Watchdog timer control/status register	WTCSR	16	H'FFFE0000	*1
	Watchdog timer counter	WTCNT	16	H'FFFE0002	*1
	Watchdog reset control/status register	WRCSR	16	H'FFFE0004	*1
SCI (channel 0)	Serial mode register_0	SCSMR_0	8	H'FFFF8000	8
	Bit rate register_0	SCBRR_0	8	H'FFFF8002	8
	Serial control register_0	SCSCR_0	8	H'FFFF8004	8
	Transmit data register_0	SCTDR_0	8	H'FFFF8006	8
	Serial status register_0	SCSSR_0	8	H'FFFF8008	8
	Receive data register_0	SCRDR_0	8	H'FFFF800A	8
	Serial direction control register_0	SCSDCR_0	8	H'FFFF800C	8
	Serial port register_0	SCSPTR_0	8	H'FFFF800E	8
SCI (channel 1)	Serial mode register_1	SCSMR_1	8	H'FFFF8800	8
	Bit rate register_1	SCBRR_1	8	H'FFFF8802	8
	Serial control register_1	SCSCR_1	8	H'FFFF8804	8
	Transmit data register_1	SCTDR_1	8	H'FFFF8806	8
	Serial status register_1	SCSSR_1	8	H'FFFF8808	8
	Receive data register_1	SCRDR_1	8	H'FFFF880A	8
	Serial direction control register_1	SCSDCR_1	8	H'FFFF880C	8
	Serial port register_1	SCSPTR_1	8	H'FFFF880E	8
SCI (channel 2)	Serial mode register_2	SCSMR_2	8	H'FFFF9000	8
	Bit rate register_2	SCBRR_2	8	H'FFFF9002	8

33.2 DC Characteristics

Tables 33.2 and 33.3 list DC characteristics.

Table 33.2 DC Characteristics (1) [Common Items]

Conditions: Ta = –40°C to +85°C (Industrial specifications)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power supply voltage		$V_{CC}Q$, $PLLV_{CC}$, DrV_{CC}*3	3.0	3.3	3.6	V	
Analog power supply voltage		AV_{CC}	4.5	5.0	5.5	V	
Supply current*1	Normal operation	I_{CC}	—	150	200	mA	Iϕ = 200 MHz Bϕ = 50 MHz Pϕ = 50 MHz
			—	85	120	mA	Iϕ = 100 MHz Bϕ = 50 MHz Pϕ = 50 MHz
	Software standby mode	I_{stby}	—	30	70	mA	VccQ = 3.3 V
	Sleep mode	I_{sleep}	—	100	140	mA	Iϕ = 200 MHz Bϕ = 50 MHz Pϕ = 50 MHz
			—	80	110	mA	Iϕ = 100 MHz Bϕ = 50 MHz Pϕ = 50 MHz
Input leakage current	All input pins	$\|I_{in}\|$	—	—	1	µA	V_{in} = 0.5 to $V_{CC}Q$ – 0.5 V
Three-state leakage current	Input/output pins, all output pins (off state)	$\|I_{STI}\|$	—	—	1	µA	V_{in} = 0.5 to $V_{CC}Q$ – 0.5 V
Input capacitance	All pins	C_{in}	—	—	20	pF	
Analog power supply current	During A/D conversion	AI_{CC}	—	3	4	mA	Per 1 module
	Waiting for A/D conversion		—	30	50	mA	Per 1 module

33.5 USB Characteristics

Table 33.24 USB Characteristics (USD+ and USD- Pins)

Conditions: $V_{CC}Q = PLLV_{CC} = DrV_{CC} = 3.0$ to 3.6 V, $AV_{CC} = AVREF = 4.5$ to 5.5V,
$V_{SS} = PLLV_{SS} = DrV_{SS} = AVREFVSS = AV_{SS} = DrV_{SS} = 0$ V,
Ta = –40°C to +85°C (Industrial specifications)

Item		Symbol	Specifications Min.	Max.	Unit	Test Condition	Figure
Input characteristics	Input high level voltage	V_{IH}	2.0	—	V		Figures 33.69 and 33.70
	Input low level voltage	V_{IL}	—	0.8	V		
	Differential input sense	V_{DI}	0.2	—	V	I(D+) – (D –)I DrV_{CC}* = 3.3 to 3.6 V	
	Differential common mode range	V_{CM}	0.8	2.5	V		
Output characteristics	Output high level voltage	V_{OH}	2.8	—	V	R_L of 15 kΩ to V_{SS}	
	Output low level voltage	V_{OL}	—	0.3	V	R_L of 1.5 kΩ to 3.6 V	
	Crossover voltage	V_{CRS}	1.3	2.0	V		
	Rise time	t_R	4	20	ns		
	Fall time	t_F	4	20	ns		
	Rise time/fall time matching	t_{RFM}	90	111.11	%	(t_R/t_F)	
	Output resistance	Z_{DRV}	28	44	Ω	Including Rs = 22 Ω	

Note: * Be sure to supply the DrV_{CC} with the same voltage as the $V_{CC}Q$.

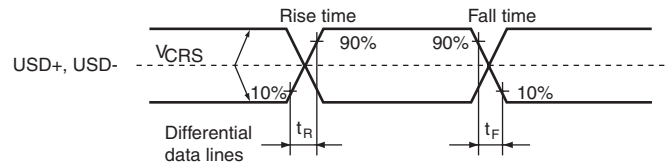


Figure 33.69 Data Signal Timing