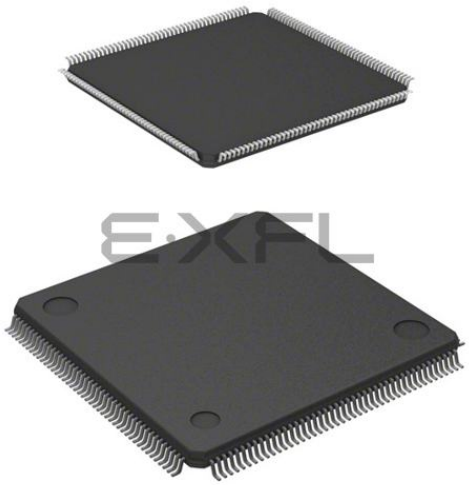
Renesas Electronics America Inc - R5F72165GDFA#V1 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, Ethernet, I²C, SCI, SPI, USB
Peripherals	DMA, PWM, WDT
Number of I/O	112
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f72165gdfa-v1

6.4 Interrupt Sources

There are six types of interrupt sources: NMI, user break, H-UDI, IRQ, memory error, and on-chip peripheral modules. Each interrupt has a priority level (0 to 16), with 0 the lowest and 16 the highest. When set to level 0, that interrupt is masked at all times.

6.4.1 NMI Interrupt

The NMI interrupt has a priority level of 16 and is accepted at all times. NMI interrupt requests are edge-detected, and the NMI edge select bit (NMIE) in interrupt control register 0 (ICR0) selects whether the rising edge or falling edge is detected.

Though the priority level of the NMI interrupt is 16, the NMI interrupt exception handling sets the interrupt mask level bits (I3 to I0) in the status register (SR) to level 15.

6.4.2 User Break Interrupt

A user break interrupt which occurs when a break condition set in the user break controller (UBC) matches has a priority level of 15. The user break interrupt exception handling sets the I3 to I0 bits in SR to level 15. For user break interrupts, see section 7, User Break Controller (UBC).

6.4.3 H-UDI Interrupt

The user debugging interface (H-UDI) interrupt has a priority level of 15, and occurs at serial input of an H-UDI interrupt instruction. H-UDI interrupt requests are edge-detected and retained until they are accepted. The H-UDI interrupt exception handling sets the I3 to I0 bits in SR to level 15. For H-UDI interrupts, see section 31, User Debugging Interface (H-UDI).

8.2 Register Descriptions

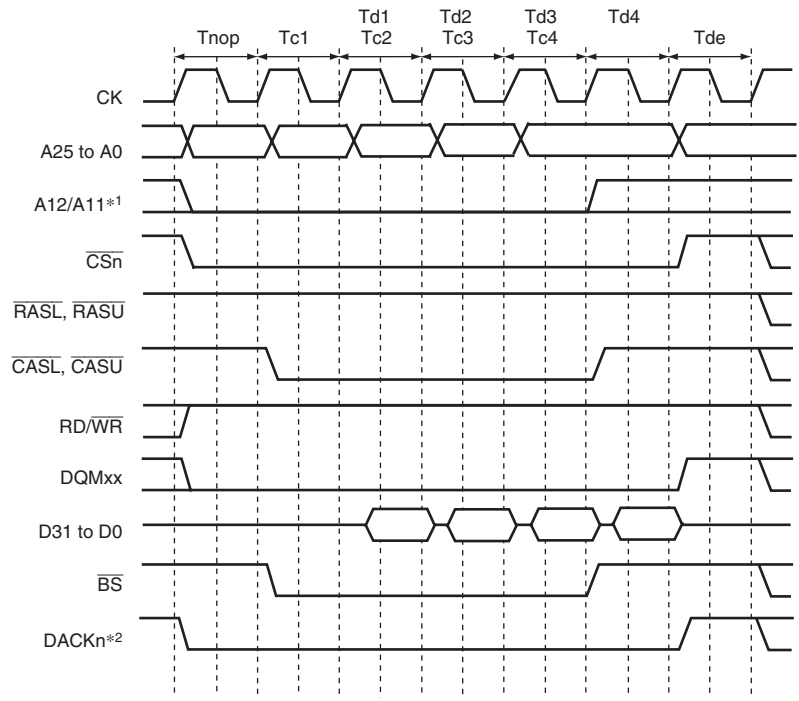
DTC has the following registers. For details on the addresses of these registers and the states of these registers in each processing state, see section 32, List of Registers.

These six registers MRA, MRB, SAR, DAR, CRA, and CRB cannot be directly accessed by the CPU. The contents of these registers are stored in the data area as transfer information. When a DTC activation request occurs, the DTC reads a start address of transfer information that is stored in the data area according to the vector address, reads the transfer information, and transfers data. After the data transfer is complete, it writes a set of updated transfer information back to the data area.

On the other hand, DTCERA to DTCERE, DTCCR, and DTCVBR can be directly accessed by the CPU.

Table 8.1 Register Configuration

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
DTC enable register A	DTCERA	R/W	H'0000	H'FFFE6000	8, 16
DTC enable register B	DTCERB	R/W	H'0000	H'FFFE6002	8, 16
DTC enable register C	DTCERC	R/W	H'0000	H'FFFE6004	8, 16
DTC enable register D	DTCERD	R/W	H'0000	H'FFFE6006	8, 16
DTC enable register E	DTCERE	R/W	H'0000	H'FFFE6008	8, 16
DTC control register	DTCCR	R/W	H'00	H'FFFE6010	8
DTC vector base register	DTCVBR	R/W	H'00000000	H'FFFE6014	8, 16, 32
Bus function extending register	BSCEHR	R/W	H'0000	H'FFFE3C1A	16



Notes: 1. Address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn is when active low is specified.

Figure 9.24 Burst Read Timing (Bank Active, Same Row Addresses in the Same Bank, CAS Latency 1)

10.6 Usage Notes

10.6.1 Setting of the Half-End Flag and the Half-End Interrupt

Since the following points for caution apply in cases where reference to the state of the half-end flag in the CHCR register or the half-end interrupt is used in conjunction with the reload function, please take care on these points.

Ensure that the reloaded number of transfers (the value set in RDMATCR) is always the same as the number of transfers that was initially set (the value set in DMATCR). If the initial setting in DMATCR and the value for the second and later transfers in RDMATCR are different, the timing with which the half-end flag is set may be faster than half the number of transfers, or the half-end flag might not be set at all. The same considerations apply to the half-end interrupt.

10.6.2 Timing of DACK and TEND Outputs

When the external memory is MPX-I/O or burst MPX-I/O, assertion of the DACK output has the same timing as the data cycle. For details, see the respective figures under section 9.5.5, MPX-I/O Interface, in section 9, Bus State Controller (BSC).

When the memory is other than the MPX-I/O or burst MPX-I/O, the DACK output is asserted with the same timing as the corresponding CS signal.

The TEND output does not depend on the type of memory and is always asserted with the same timing as the corresponding CS signal.

10.6.3 CHCR Setting

When changing the CHCR setting, the DE bit of the relevant channel must be cleared before the change.

10.6.4 Note on Activation of Multiple Channels

The same internal request must not be set to more than one channel.

10.6.5 Note on Transfer Request Input

A transfer request should be input after the DMAC settings have been made.

Table 11.27 TIORL_4 (Channel 4)

				Description	
Bit 3 IOC3	**Bit 2 IOC2**	**Bit 1 IOC1**	**Bit 0 IOC0**	**TGRC_4 Function**	**TIOC4C Pin Function**
0	0	0	0	Output compare register*2	Output retained*1
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	X	0	0	Input capture register*2	Input capture at rising edge
			1		Input capture at falling edge
		1	X		Input capture at both edges

[Legend]

X: Don't care

Notes: 1. After power-on reset, 0 is output until TIOR is set.

2. When the BFA bit in TMDR_4 is set to 1 and TGRC_4 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

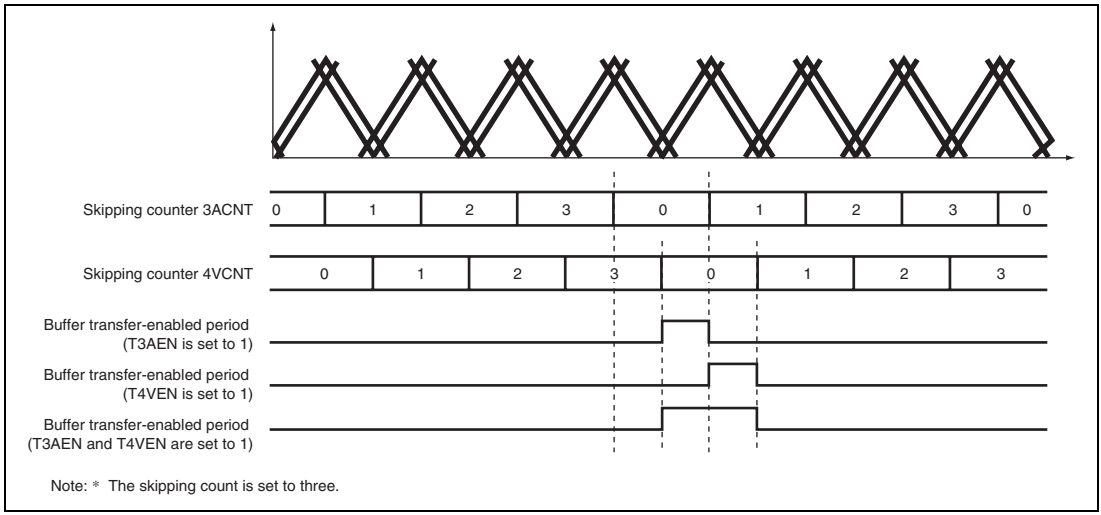


Figure 11.78 Relationship between Bits T3AEN and T4VEN in TITCR and Buffer Transfer-Enabled Period

(4) Complementary PWM Mode Output Protection Function

Complementary PWM mode output has the following protection functions.

(a) Register and Counter Miswrite Prevention Function

With the exception of the buffer registers, which can be rewritten at any time, access by the CPU can be enabled or disabled for the mode registers, control registers, compare registers, and counters used in complementary PWM mode by means of the RWE bit in the timer read/write enable register (TRWER). The applicable registers are some (21 in total) of the registers in channels 3 and 4 shown in the following:

- TCR_3 and TCR_4, TMDR_3 and TMDR_4, TIORH_3 and TIORH_4, TIORL_3 and TIORL_4, TIER_3 and TIER_4, TCNT_3 and TCNT_4, TGRA_3 and TGRA_4, TGRB_3 and TGRB_4, TOER, TOCR, TGCR, TCDR, and TDDR.

This function enables miswriting due to CPU runaway to be prevented by disabling CPU access to the mode registers, control registers, and counters. When the applicable registers are read in the access-disabled state, undefined values are returned. Writing to these registers is ignored.

11.7.3 Caution on Period Setting

When counter clearing on compare match is set, TCNT is cleared in the final state in which it matches the TGR value (the point at which the count value matched by TCNT is updated). Consequently, the actual counter frequency is given by the following formula:

- Channel 0 to 4

$$f = \frac{P\phi}{(N + 1)}$$

- Channel 5

$$f = \frac{P\phi}{N}$$

Where f: Counter frequency
Pϕ: Peripheral clock operating frequency
N: TGR set value

11.7.4 Contention between TCNT Write and Clear Operations

If the counter clear signal is generated in the T2 state of a TCNT write cycle, TCNT clearing takes precedence and the TCNT write is not performed.

Figure 11.121 shows the timing in this case.

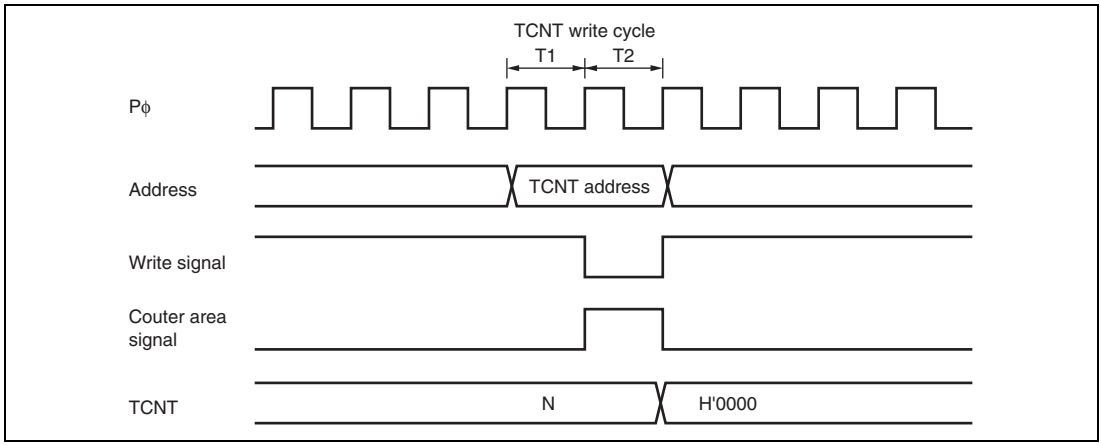


Figure 11.121 Contention between TCNT Write and Clear Operations

(25) Operation when Error Occurs during Complementary PWM Mode Operation, and Operation is Restarted in Reset-Synchronized PWM Mode

Figure 11.163 shows an explanatory diagram of the case where an error occurs in complementary PWM mode and operation is restarted in reset-synchronized PWM mode.

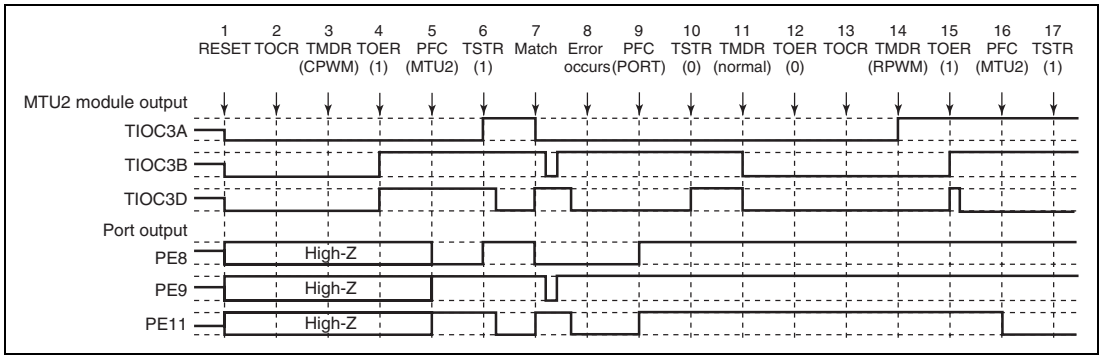


Figure 11.163 Error Occurrence in Complementary PWM Mode, Recovery in Reset-Synchronized PWM Mode

1 to 10 are the same as in figure 11.159.

11. Set normal mode. (MTU2 output goes low.)
12. Disable channel 3 and 4 output with TOER.
13. Select the reset-synchronized PWM mode output level and cyclic output enabling/disabling with TOCR.
14. Set reset-synchronized PWM.
15. Enable channel 3 and 4 output with TOER.
16. Set MTU2 output with the PFC.
17. Operation is restarted by TSTR.

16.3.7 Serial Status Register (SCSSR)

SCSSR is an 8-bit register that contains status flags to indicate the SCI operating state.

The CPU can always read and write to SCSSR, but cannot write 1 to status flags TDRE, RDRF, ORER, PER, and FER. These flags can be cleared to 0 only after 1 is read from the flags. The TEND flag is a read-only bit and cannot be modified.

Bit:	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Initial value:	1	0	0	0	0	1	0	0
R/W:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Note: * Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

Bit	Bit Name	Initial value	R/W	Description
7	TDRE	1	R/(W)*	Transmit Data Register Empty Indicates whether data has been transferred from the transmit data register (SCTDR) to the transmit shift register (SCTSR) and SCTDR has become ready to be written with next serial transmit data. 0: Indicates that SCTDR holds valid transmit data [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DTC is activated by a TXI interrupt and transmit data is transferred to SCTDR while the DISEL bit of MRB in the DTC is 0 (except when the DTC transfer counter value has become H'0000). 1: Indicates that SCTDR does not hold valid transmit data [Setting conditions] • By a power-on reset or in module standby mode • When the TE bit in SCSCR is 0 • When data is transferred from SCTDR to SCTSR and data can be written to SCTDR

In serial reception, the SCI operates as described below.

1. The SCI monitors the transmission line, and if a 0 start bit is detected, performs internal synchronization and starts reception.
2. The received data is stored in SCRSR in LSB-to-MSB order.
3. The parity bit and stop bit are received.
   After receiving these bits, the SCI carries out the following checks.
   A. Parity check: The SCI counts the number of 1s in the received data and checks whether the count matches the even or odd parity specified by the O/$\overline{E}$ bit in the serial mode register (SCSMR).
   B. Stop bit check: The SCI checks whether the stop bit is 1. If there are two stop bits, only the first is checked.
   C. Status check: The SCI checks whether the RDRF flag is 0 and the received data can be transferred from the receive shift register (SCRSR) to SCRDR.

   If all the above checks are passed, the RDRF flag is set to 1 and the received data is stored in SCRDR. If a receive error is detected, the SCI operates as shown in table 16.17.

   Note: When a receive error occurs, subsequent reception cannot be continued. In addition, the RDRF flag will not be set to 1 after reception; be sure to clear the error flag to 0.

4. If the EIO bit in SCSPTR is cleared to 0 and the RIE bit in SCSCR is set to 1 when the RDRF flag changes to 1, a receive-data-full interrupt (RXI) request is generated. If the RIE bit in SCSCR is set to 1 when the ORER, PER, or FER flag changes to 1, a receive error interrupt (ERI) request is generated.

Table 16.17 Receive Errors and Error Conditions

Receive Error	Abbreviation	Error Condition	Data Transfer
Overrun error	ORER	When the next data reception is completed while the RDRF flag in SCSSR is set to 1	The received data is not transferred from SCRSR to SCRDR.
Framing error	FER	When the stop bit is 0	The received data is transferred from SCRSR to SCRDR.
Parity error	PER	When the received data does not match the even or odd parity specified in SCSMR	The received data is transferred from SCRSR to SCRDR.

- Transmitting Serial Data (Asynchronous Mode)

Figure 17.4 shows a sample flowchart for serial transmission. Use the following procedure for serial data transmission after enabling the SCIF for transmission.

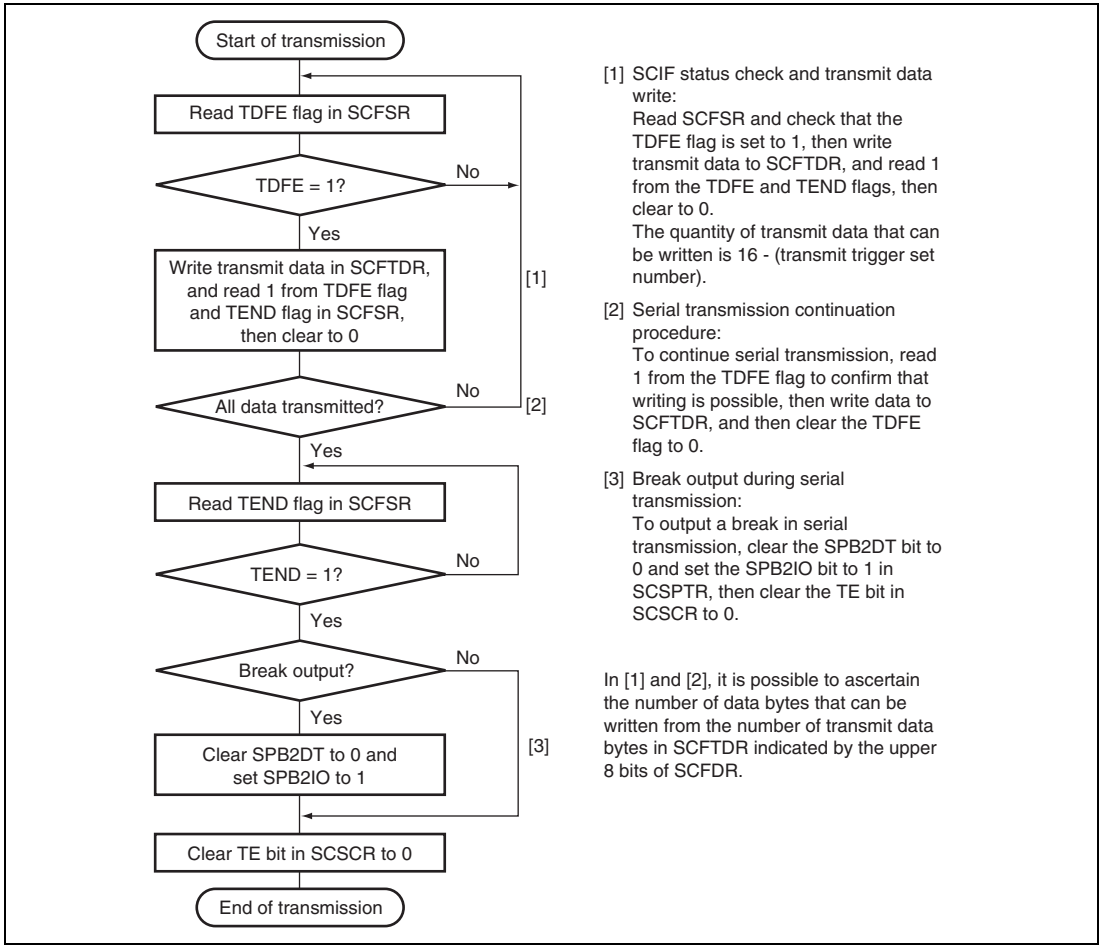


Figure 17.4 Sample Flowchart for Transmitting Serial Data

(1-4) Transfer Operation Flowchart (CPHA = 1)

Figure 18.26 shows an example of transfer operation flowchart for the RSPI during clock synchronous operation.

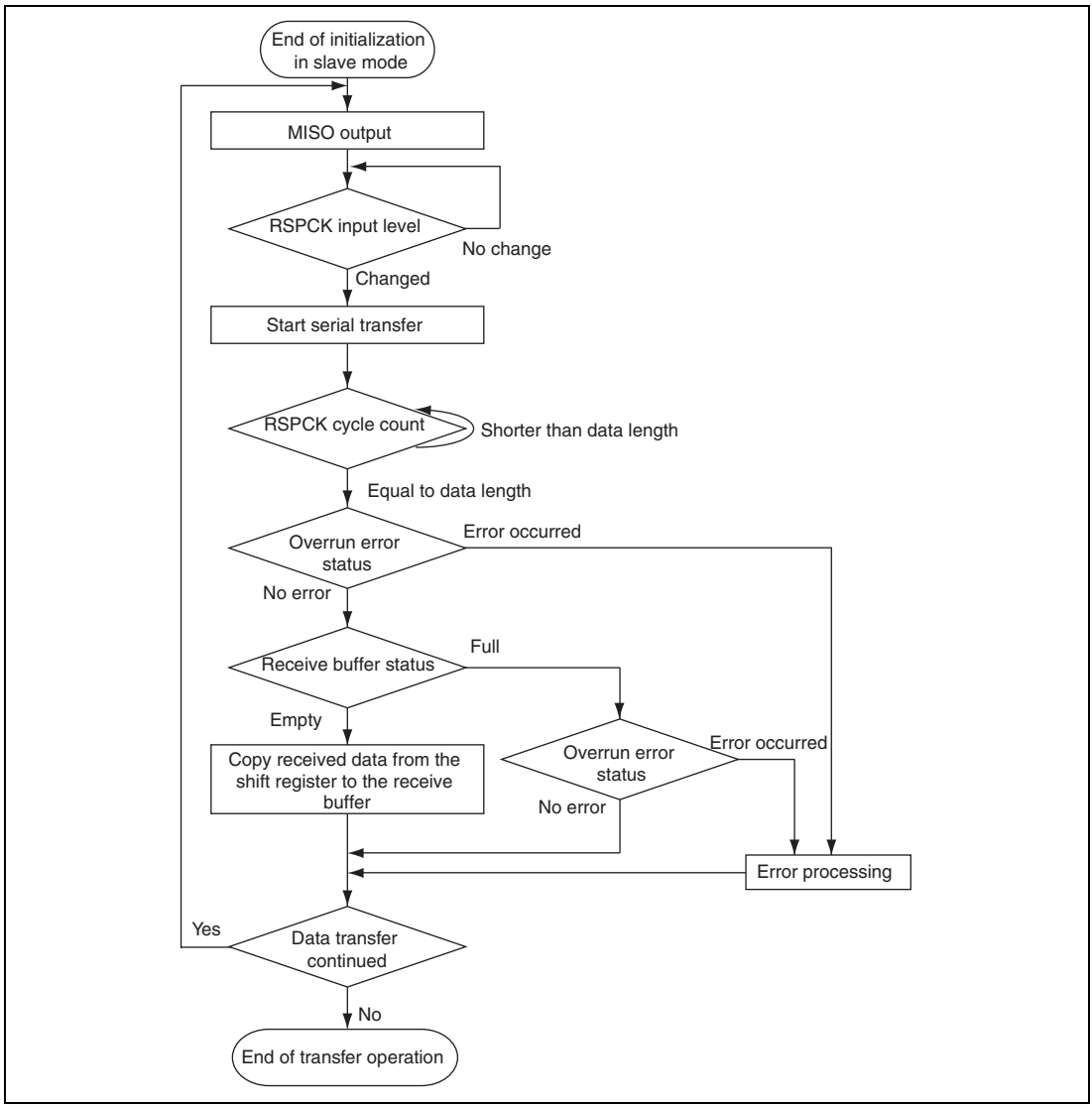


Figure 18.26 Example of Transfer Operation Flowchart in Slave Mode (CPHA = 1)

24.3.35 USB Data Status Register 3 (USBDASTS3)

USBDASTS3 indicates whether the transmit FIFO buffer contains valid data. The EP8DE or EP9DE bit is set to 1 when data is written to the corresponding FIFO buffer and the packet enable state is set. This bit is cleared when data has been completely transmitted to the host.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	EP9DE	EP8DE	-
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

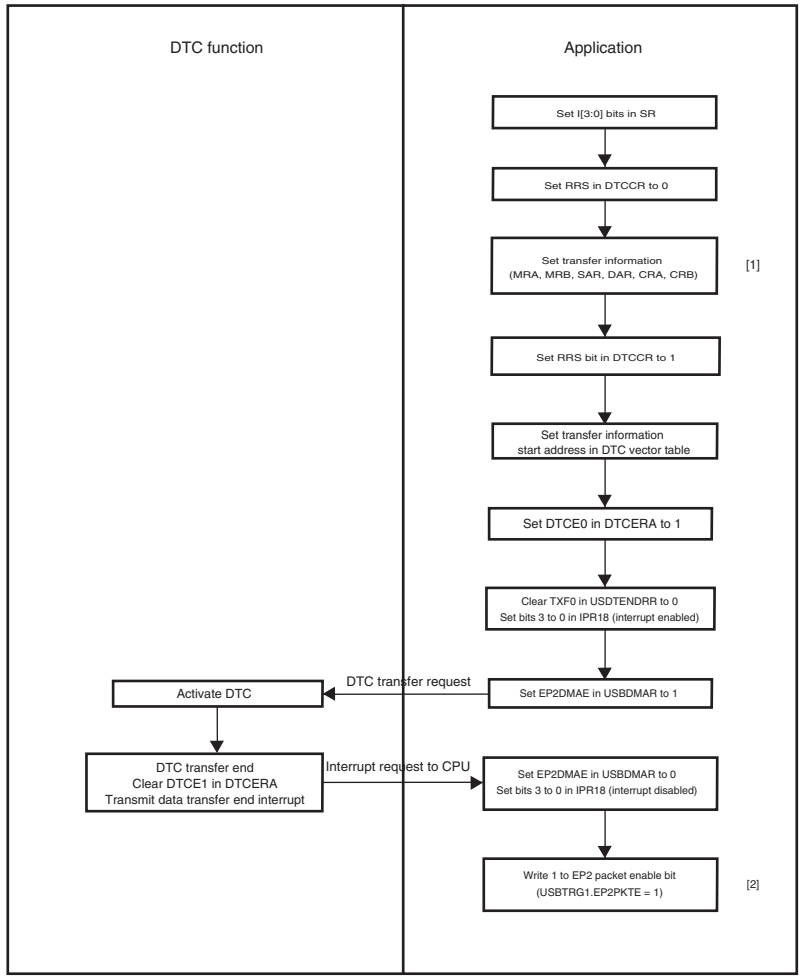
Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	EP9DE	0	R	EP9 Data Present This bit is set to 1 when the endpoint 9 FIFO buffer contains valid data.
1	EP8DE	0	R	EP8 Data Present This bit is set to 1 when the endpoint 8 FIFO buffer contains valid data.
0	—	0	R	Reserved This bit is always read as 0.

24.3.42 USB FIFO Clear Register 2 (USBFCLR2)

USBFCLR2 is a write-only register to initialize the FIFO buffers for each endpoint. Writing 1 to a bit clears all the data in the corresponding FIFO buffer. The corresponding interrupt flag is not cleared. Do not clear the FIFO buffer during transmission/reception. The read value of this register is undefined. Do not write a value to this register using the read value, such as a bit manipulation instruction.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	EP6 CLR	EP5 CLR	EP4 CLR
Initial value:	0	0	0	0	0	0	0	0
R/W:	-	-	-	-	-	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	—	Reserved The write value should always be 0.
2	EP6CLR	0	W	EP6 Clear Writing 1 to this bit initializes the endpoint 6 transmit FIFO buffer.
1	EP5CLR	0	W	EP5 Clear Writing 1 to this bit initializes both endpoint 5 transmit FIFO buffers.
0	EP4CLR	0	W	EP4 Clear Writing 1 to this bit initializes both endpoint 4 receive FIFO buffers.



[1] For block transfer mode, a block size of 64 bytes or less must be set in CRA.

[2] Not necessary when transmit data size is a multiple of 64 bytes.

Figure 24.26 Example of DTC Transfer for Bulk-IN Transfer (EP2) (When Transmit Data Size is Determined Before Receiving IN Token)

Section 25 Ethernet Controller (EtherC) (SH7216A, SH7214A, SH7216G, and SH7214G only)

This LSI has an on-chip Ethernet controller (EtherC) conforming to the Ethernet or the IEEE802.3 MAC (Media Access Control) layer standard. Connecting a physical-layer LSI (PHY-LSI) conforming to this standard enables the EtherC to transmit and receive Ethernet/IEEE802.3 frames. The EtherC has one MAC layer interface port. The EtherC is connected to the Ethernet Direct Memory Access Controller (E-DMAC) for Ethernet controller inside the LSI, and carries out high-speed data transfer to and from the memory.

Figure 25.1 shows a configuration of the EtherC.

25.1 Features

- Transmission and reception of Ethernet/IEEE802.3 frames
- Supports 10/100 Mbps data transfer
- Supports full-duplex and half-duplex modes
- Conforms to IEEE802.3u standard MII (Media Independent Interface)
- Magic Packet detection and Wake-On-LAN (WOL) signal output
- Conforms to IEEE802.3x flow control

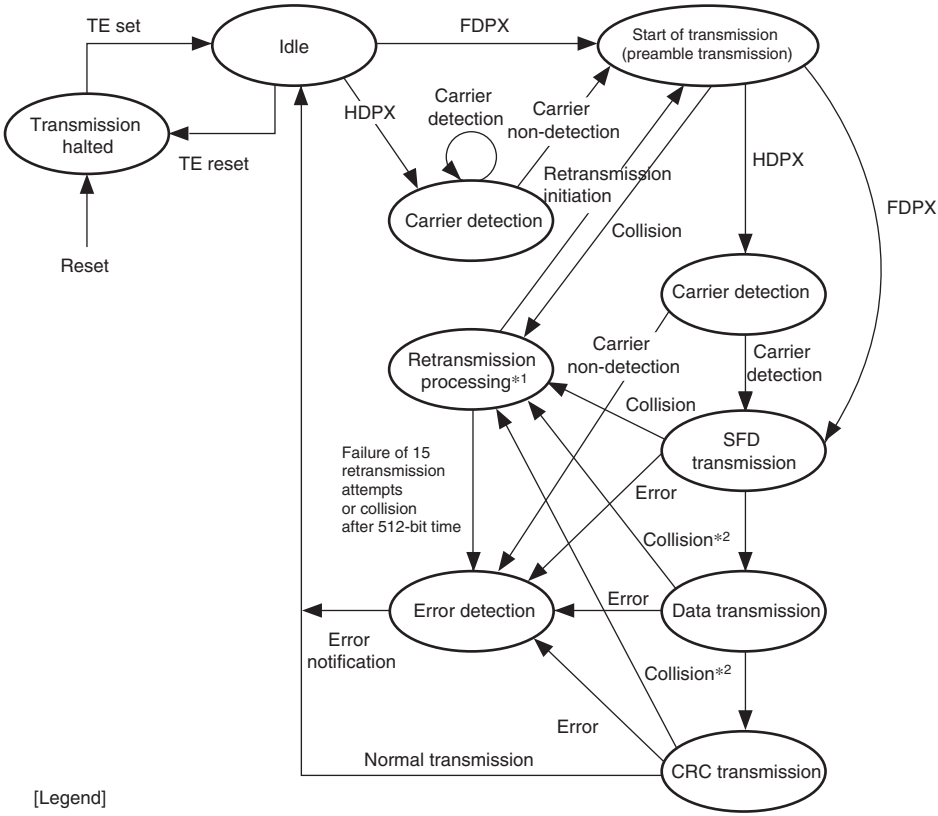
25.3.19 IPG Register (IPGR)

IPGR is used to set an IPG (Inter Packet Gap) value. This register must not be modified while the transmitting and receiving functions of the EtherC mode register (ECMR) are enabled. (For details, see section 25.4.6, Operation by IPG Setting.)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	IPG[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4 to 0	IPG[4:0]	H'14	R/W	Inter Packet Gap An IPG value is set in units of 4-bit time. H'00: 16-bit time H'01: 20-bit time : : H'14: 96-bit time (default) : : H'1F: 140-bit time



[Legend]
FDPX: Full Duplex
HDPX: Half Duplex
SFD: Start Frame Delimiter

Notes:1. Retransmission processing includes both jam transmission resultant from collision detection and the adjustment of transmission intervals by the back-off algorithm.
2. Retransmission is performed only during transmission of 512-bit (or less) data including the preamble and SFD. If a collision is detected while data exceeding 512 bits is being transmitted, only jam is transmitted and the retransmission processing by the back-off algorithm is not performed.

Figure 25.2 EtherC Transmitter State Transitions

Module Name	Register Name	Abbreviation	Number of Bits	Address	Access Size
RSPI	RSPI bit rate register	SPBR	8	H'FFFFB00A	8, 16
	RSPI data control register	SPDCR	8	H'FFFFB00B	8
	RSPI clock delay register	SPCKD	8	H'FFFFB00C	8, 16
	RSPI slave select negation delay register	SSLND	8	H'FFFFB00D	8
	RSPI next-access delay register	SPND	8	H'FFFFB00E	8
	RSPI command register 0	SPCMD0	16	H'FFFFB010	16
	RSPI command register 1	SPCMD1	16	H'FFFFB012	16
	RSPI command register 2	SPCMD2	16	H'FFFFB014	16
	RSPI command register 3	SPCMD3	16	H'FFFFB016	16
IIC3	I^2C bus control register 1	ICCR1	8	H'FFFEE000	8
	I^2C bus control register 2	ICCR2	8	H'FFFEE001	8
	I^2C bus mode register	ICMR	8	H'FFFEE002	8
	I^2C bus interrupt enable register	ICIER	8	H'FFFEE003	8
	I^2C bus status register	ICSR	8	H'FFFEE004	8
	Slave address register	SAR	8	H'FFFEE005	8
	I^2C bus transmit data register	ICDRT	8	H'FFFEE006	8
	I^2C bus receive data register	ICDRR	8	H'FFFEE007	8
	NF2CYC register	NF2CYC	8	H'FFFEE008	8
ADC	A/D control register_0	ADCR_0	8	H'FFFFE800	8
	A/D status register_0	ADSR_0	8	H'FFFFE802	8
	A/D start trigger select register_0	ADSTRGR_0	8	H'FFFFE81C	8
	A/D analog input channel select register_0	ADANSR_0	8	H'FFFFE820	8
	A/D bypass control register_0	ADBYPSCR_0	8	H'FFFFE830	8
	A/D data register 0	ADDR0	16	H'FFFFE840	16
	A/D data register 1	ADDR1	16	H'FFFFE842	16
	A/D data register 2	ADDR2	16	H'FFFFE844	16
	A/D data register 3	ADDR3	16	H'FFFFE846	16
	A/D control register_1	ADCR_1	8	H'FFFFEC00	8
	A/D status register_1	ADSR_1	8	H'FFFFEC02	8
	A/D start trigger select register_1	ADSTRGR_1	8	H'FFFFEC1C	8

33.3 AC Characteristics

Signals input to this LSI are basically handled as signals in synchronization with a clock. The setup and hold times for input pins must be followed.

Table 33.4 Maximum Operating Frequency

Conditions: $V_{cc}Q = PLLV_{cc} = DrV_{cc} = 3.0$ to 3.6 V, $AV_{cc} = AVREF = 4.5$ to 5.5 V,
$V_{ss} = PLLV_{ss} = DrV_{ss} = AVREFVSS = AV_{ss} = 0$ V,
Ta = –40°C to +85°C (Industrial specifications)

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Operating frequency	CPU (Iϕ)	f	20	—	200	MHz	
	Internal bus, external bus (Bϕ)		20	—	50		
	Peripheral module (Pϕ)		20	—	50		
	MTU2S (Mϕ)		40	—	100		
	AD (Aϕ)		40	—	50		