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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, I²C, SCI, SPI, USB
Peripherals	DMA, PWM, WDT
Number of I/O	112
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f72166adfp-v1

Items	Specification
Data transfer controller (DTC)	• Data transfer activated by an on-chip peripheral module interrupt can be done independently of the CPU transfer. • Transfer mode selectable for each interrupt source (transfer mode is specified in memory) • Multiple data transfer enabled for one activation source • Various transfer modes Normal mode, repeat mode, or block transfer mode can be selected. • Data transfer size can be specified as byte, word, or longword • The interrupt that activated the DTC can be issued to the CPU. A CPU interrupt can be requested after one data transfer completion. • A CPU interrupt can be requested after all specified data transfer completion.
Clock pulse generator (CPG)	• Clock mode: Input clock can be selected from external input (EXTAL) or crystal resonator • Input clock can be multiplied by 16 by the internal PLL circuit • Five types of clocks generated: CPU clock: Maximum 200 MHz (SH7216A, SH7216B, SH7214A, and SH7214B) Maximum 100 MHz (SH7216G, SH7216H, SH7214G, and SH7214H) Bus clock: Maximum 50 MHz Peripheral clock: Maximum 50 MHz Timer clock: Maximum 100 MHz AD clock: Maximum 50 MHz
Watchdog timer (WDT)	• On-chip one-channel watchdog timer • A counter overflow can reset the LSI
Power-down modes	• Three power-down modes provided to reduce the current consumption in this LSI Sleep mode Software standby mode Module standby mode

PLL Multiplication Ratio	FRQCR/MCLKCR/ACLKCR Division Ratio Setting					Clock Ratio					Clock Frequency (MHz)*					
	Iϕ	Bϕ	Pϕ	Mϕ	Aϕ	Iϕ	Bϕ	Pϕ	Mϕ	Aϕ	Input Clock	Iϕ	Bϕ	Pϕ	Mϕ	Aϕ
×16	1/4	1/8	1/8	1/4	1/4	4	2	2	4	4	12.5	50	25	25	50	50
	1/4	1/4	1/8	1/4	1/4	4	4	2	4	4		50	50	25	50	50
	1/4	1/4	1/4	1/4	1/4	4	4	4	4	4		50	50	50	50	50
	1/2	1/8	1/8	1/4	1/4	8	2	2	4	4		100	25	25	50	50
	1/2	1/8	1/8	1/2	1/4	8	2	2	8	4		100	25	25	100	50
	1/2	1/4	1/8	1/4	1/4	8	4	2	4	4		100	50	25	50	50
	1/2	1/4	1/8	1/2	1/4	8	4	2	8	4		100	50	25	100	50
	1/2	1/4	1/4	1/4	1/4	8	4	4	4	4		100	50	50	50	50
	1/2	1/4	1/4	1/2	1/4	8	4	4	8	4		100	50	50	100	50
	1/1	1/8	1/8	1/4	1/4	16	2	2	4	4		200	25	25	50	50
	1/1	1/8	1/8	1/2	1/4	16	2	2	8	4		200	25	25	100	50
	1/1	1/4	1/8	1/4	1/4	16	4	2	4	4		200	50	25	50	50
	1/1	1/4	1/8	1/2	1/4	16	4	2	8	4		200	50	25	100	50
	1/1	1/4	1/4	1/4	1/4	16	4	4	4	4		200	50	50	50	50
	1/1	1/4	1/4	1/2	1/4	16	4	4	8	4		200	50	50	100	50

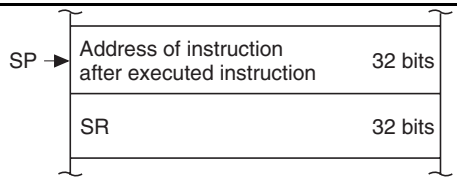
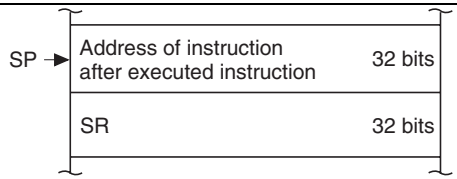
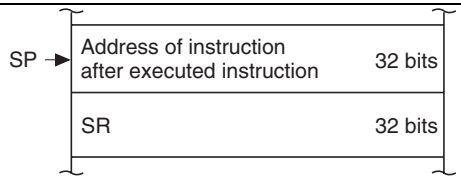
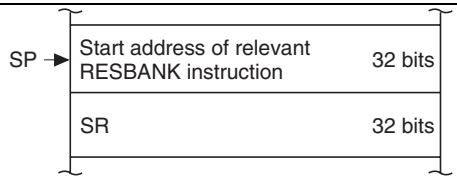
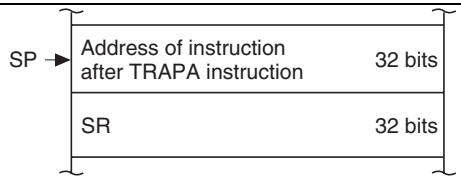
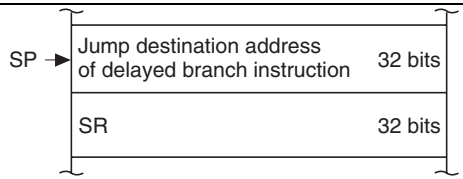
Notes: * Clock frequencies when the input clock frequency is assumed to be the shown value.

1. The PLL multiplication ratio is fixed at ×16. The division ratio can be selected from ×1, ×1/2, ×1/4, and ×1/8 for each clock by the setting in the frequency control register.
2. The output frequency of the PLL circuit is obtained by multiplication of the frequency of the input from the crystal resonator or EXTAL pin and the multiplication ratio (×16) of the PLL circuit. This output frequency must be 200 MHz or lower.
3. The input to the divider is always the output from the PLL circuit.
4. The internal clock (Iϕ) frequency is obtained by multiplication of the frequency of the input from the crystal resonator or EXTAL pin, the multiplication ratio (×16) of the PLL circuit, and the division ratio of the divider. The resultant frequency of the internal clock (Iϕ) must not exceed 200 MHz or 100 MHz (maximum operating frequency) or lower.
5. The bus clock (Bϕ) frequency is obtained by multiplication of the frequency of the input from the crystal resonator or EXTAL pin, the multiplication ratio (×16) of the PLL circuit, and the division ratio of the divider. The resultant frequency of the bus clock (Bϕ) must not exceed 50 MHz or the internal clock (Iϕ) frequency.
6. The peripheral clock (Pϕ) frequency is obtained by multiplication of the frequency of the input from the crystal resonator or EXTAL pin, the multiplication ratio (×16) of the PLL circuit, and the division ratio of the divider. The resultant frequency of the peripheral clock (Pϕ) must not exceed 50 MHz or the bus clock (Bϕ) frequency.

5.8 Stack Status after Exception Handling Ends

The status of the stack after exception handling ends is as shown in table 5.11.

Table 5.11 Stack Status After Exception Handling Ends

Exception Type	Stack Status
Address error	
Interrupt	
Register bank error (overflow) FPU exception	
Register bank error (underflow)	
Trap instruction	
Slot illegal instruction	

Bit	Bit Name	Initial Value	R/W	Description
0	ERR	0	R/(W)*	Transfer Stop Flag Indicates that a DTC address error or NMI interrupt has occurred. If a DTC address error or NMI interrupt occurs while the DTC is active, a DTC address error handling or NMI interrupt handling processing is executed after the DTC has released the bus mastership. The DTC halts after a data transfer or a transfer information writing state depending on the NMI input timing. Note that a writing state is not exact, when the DTC halts after a data transfer. When the data is transferred, set a transfer information once again (except that a read skip is performed). 0: No interrupt has occurred 1: An interrupt has occurred [Clearing condition] • When writing 0 after reading 1

Note: * Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

8.2.9 DTC Vector Base Register (DTCVBR)

DTCVBR is a 32-bit register that specifies the base address for vector table address calculation.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 12		All 0	R/W	Bits 11 to 0 are always read as 0. The write value should always be 0.
11 to 0	—	All 0	R	

Bit	Bit Name	Initial Value	R/W	Description
10 to 7	WR[3:0]	1010	R/W	Number of Access Wait Cycles Specify the number of cycles that are necessary for read/write access. 0000: No cycle 0001: 1 cycle 0010: 2 cycles 0011: 3 cycles 0100: 4 cycles 0101: 5 cycles 0110: 6 cycles 0111: 8 cycles 1000: 10 cycles 1001: 12 cycles 1010: 14 cycles 1011: 18 cycles 1100: 24 cycles 1101: Reserved (setting prohibited) 1110: Reserved (setting prohibited) 1111: Reserved (setting prohibited)
6	WM	0	R/W	External Wait Mask Specification Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access wait cycle is 0. 0: External wait input is valid 1: External wait input is ignored
5 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial value	R/W	Description
2 to 0	4VCOR[2:0]	000	R/W	These bits specify the TCIV_4 interrupt skipping count within the range from 0 to 7.* For details, see table 11.41.

Note: * When 0 is specified for the interrupt skipping count, no interrupt skipping will be performed. Before changing the interrupt skipping count, be sure to clear the T3AEN and T4VEN bits to 0 to clear the skipping counter (TICNT).

Table 11.40 Setting of Interrupt Skipping Count by Bits 3ACOR2 to 3ACOR0

Bit 6	Bit 5	Bit 4	
3ACOR2	3ACOR1	3ACOR0	Description
0	0	0	Does not skip TGIA_3 interrupts.
0	0	1	Sets the TGIA_3 interrupt skipping count to 1.
0	1	0	Sets the TGIA_3 interrupt skipping count to 2.
0	1	1	Sets the TGIA_3 interrupt skipping count to 3.
1	0	0	Sets the TGIA_3 interrupt skipping count to 4.
1	0	1	Sets the TGIA_3 interrupt skipping count to 5.
1	1	0	Sets the TGIA_3 interrupt skipping count to 6.
1	1	1	Sets the TGIA_3 interrupt skipping count to 7.

Table 11.41 Setting of Interrupt Skipping Count by Bits 4VCOR2 to 4VCOR0

Bit 2	Bit 1	Bit 0	
4VCOR2	4VCOR1	4VCOR0	Description
0	0	0	Does not skip TCIV_4 interrupts.
0	0	1	Sets the TCIV_4 interrupt skipping count to 1.
0	1	0	Sets the TCIV_4 interrupt skipping count to 2.
0	1	1	Sets the TCIV_4 interrupt skipping count to 3.
1	0	0	Sets the TCIV_4 interrupt skipping count to 4.
1	0	1	Sets the TCIV_4 interrupt skipping count to 5.
1	1	0	Sets the TCIV_4 interrupt skipping count to 6.
1	1	1	Sets the TCIV_4 interrupt skipping count to 7.

(c) Phase counting mode 3

Figure 11.32 shows an example of phase counting mode 3 operation, and table 11.50 summarizes the TCNT up/down-count conditions.

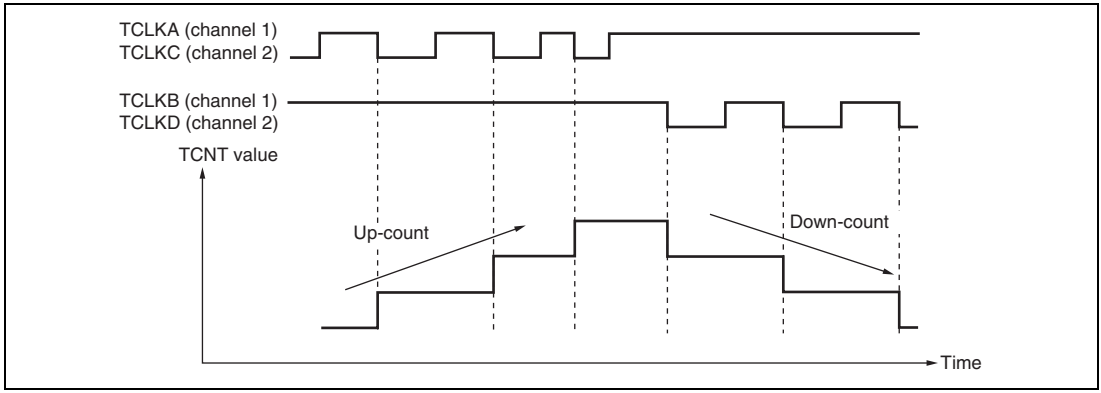


Figure 11.32 Example of Phase Counting Mode 3 Operation

Table 11.50 Up/Down-Count Conditions in Phase Counting Mode 3

TCLKA (Channel 1) TCLKC (Channel 2)	TCLKB (Channel 1) TCLKD (Channel 2)	Operation
High level	↑	Don't care
Low level	↓	Don't care
↑	Low level	Don't care
↓	High level	Up-count
High level	↓	Down-count
Low level	↑	Don't care
↑	High level	Don't care
↓	Low level	Don't care

[Legend]
↑: Rising edge
↓: Falling edge

11.5 Interrupt Sources

11.5.1 Interrupt Sources and Priorities

There are three kinds of MTU2 interrupt source; TGR input capture/compare match, TCNT overflow, and TCNT underflow. Each interrupt source has its own status flag and enable/disabled bit, allowing the generation of interrupt request signals to be enabled or disabled individually.

When an interrupt request is generated, the corresponding status flag in TSR is set to 1. If the corresponding enable/disable bit in TIER is set to 1 at this time, an interrupt is requested. The interrupt request is cleared by clearing the status flag to 0.

Relative channel priorities can be changed by the interrupt controller, however the priority order within a channel is fixed. For details, see section 6, Interrupt Controller (INTC).

Table 11.57 lists the MTU2 interrupt sources.

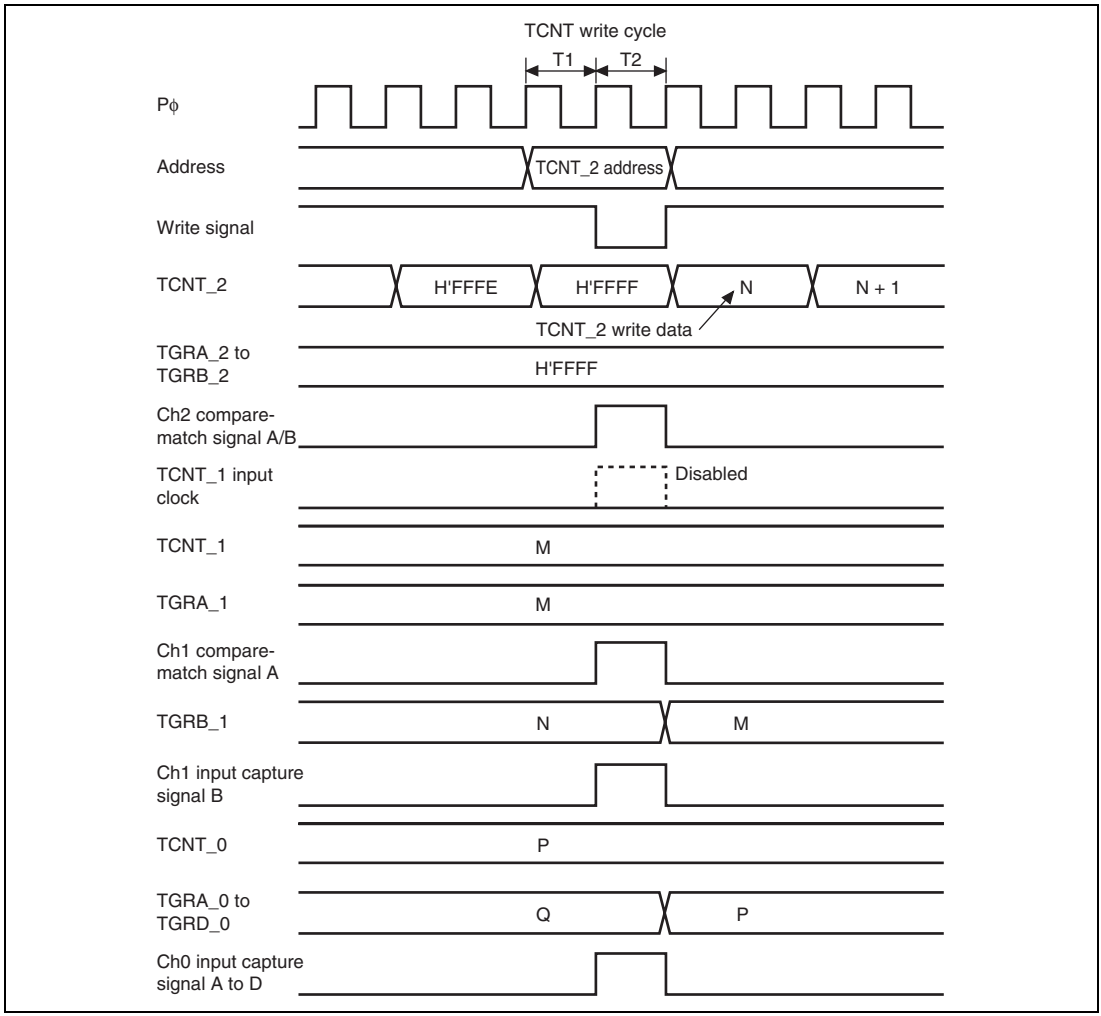


Figure 11.131 TCNT_2 Write and Overflow/Underflow Contention with Cascade Connection

Section 12 Multi-Function Timer Pulse Unit 2S (MTU2S)

This LSI has an on-chip multi-function timer pulse unit 2S (MTU2S) that comprises three 16-bit timer channels. The MTU2S includes channels 3 to 5 of the MTU2. For details, refer to section 11, Multi-Function Timer Pulse Unit 2 (MTU2). To distinguish from the MTU2, "S" is added to the end of the MTU2S input/output pin and register names. For example, TIOC3A is called TIOC3AS and TGRA_3 is called TGRA_3S in this section.

The MTU2S can operate at 100 MHz max. for complementary PWM output functions or at 50 MHz max. for the other functions.

Table 12.1 MTU2S Functions

Item		Channel 3	Channel 4	Channel 5
Count clock		Mϕ/1 Mϕ/4 Mϕ/16 Mϕ/64 Mϕ/256 Mϕ/1024	Mϕ/1 Mϕ/4 Mϕ/16 Mϕ/64 Mϕ/256 Mϕ/1024	Mϕ/1 Mϕ/4 Mϕ/16 Mϕ/64
General registers		TGRA_3S TGRB_3S	TGRA_4S TGRB_4S	TGRU_5S TGRV_5S TGRW_5S
General registers/ buffer registers		TGRC_3S TGRD_3S	TGRC_4S TGRD_4S	—
I/O pins		TIOC3AS TIOC3BS TIOC3CS TIOC3DS	TIOC4AS TIOC4BS TIOC4CS TIOC4DS	Input pins TIC5US TIC5VS TIC5WS
Counter clear function		TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture
Compare match output	0 output	√	√	—
	1 output	√	√	—
	Toggle output	√	√	—
Input capture function		√	√	√
Synchronous operation		√	√	—

14.4 Interrupts

14.4.1 Interrupt Sources and DTC/DMAC Transfer Requests

The CMT has channels and each of them to which a different vector address is allocated has a compare match interrupt. When both the interrupt request flag (CMF) and the interrupt enable bit (CMIE) are set to 1, the corresponding interrupt request is output. When the interrupt is used to activate a CPU interrupt, the priority of channels can be changed by the interrupt controller settings. For details, see section 6, Interrupt Controller (INTC).

Clear the CMF bit to 0 by the user exception handling routine. If this operation is not carried out, another interrupt will be generated. The direct memory access controller (DMAC) can be set to be activated when a compare match interrupt is requested. In this case, an interrupt is not issued to the CPU. If the setting to activate the DMAC has not been made, an interrupt request is sent to the CPU. The CMF bit is automatically cleared to 0 when data is transferred by the DMAC.

The data transfer controller (DTC) can be activated by an interrupt request. In this case, the priority between channels is fixed. For details, refer to section 8, Data Transfer Controller (DTC).

Table 14.2 Interrupt Sources

Channel	Interrupt Source	Interrupt Enable Bit	Interrupt Flag	DMAC/DTC Activation	Priority
0	CMI0	CMIE	CMF	Possible	High
1	CMI1	CMIE	CMF	Possible	Low

Bit	Bit Name	Initial Value	R/W	Description
0	DR	0	R/(W)*	Receive Data Ready Indicates that the quantity of data in the receive FIFO data register (SCFRDR) is less than the specified receive trigger number, and that the next data has not yet been received after the elapse of 15 ETU from the last stop bit in asynchronous mode. In clocked synchronous mode, this bit is not set to 1. 0: Receiving is in progress, or no receive data remains in SCFRDR after receiving ended normally [Clearing conditions] • DR is cleared to 0 when the chip undergoes a power-on reset • DR is cleared to 0 when all receive data are read after 1 is read from DR and then 0 is written. • DR is cleared to 0 when all receive data in SCFRDR are read by the DMAC/DTC. 1: Next receive data has not been received [Setting condition] • DR is set to 1 when SCFRDR contains less data than the specified receive trigger number, and the next data has not yet been received after the elapse of 15 ETU from the last stop bit.* Note: * This is equivalent to 1.5 frames with the 8-bit, 1-stop-bit format. (ETU: elementary time unit)

Note: * Only 0 can be written to clear the flag after 1 is read.

(1) Transmit/Receive Formats

The data length is fixed at eight bits. No parity bit can be added.

(2) Clock

An internal clock generated by the on-chip baud rate generator by the setting of the C/A bit in SCSMR and CKE[1:0] in SCSCR, or an external clock input from the SCK pin can be selected as the SCIF transmit/receive clock.

When the SCIF operates on an internal clock, it outputs the clock signal at the SCK pin. Eight clock pulses are output per transmitted or received character. When the SCIF is not transmitting or receiving, the clock signal remains in the high state. When only receiving, the clock signal outputs while the RE bit of SCSCR is 1 and the number of data in receive FIFO is more than the receive FIFO data trigger number.

(3) Transmitting and Receiving Data

- SCIF Initialization (Clocked Synchronous Mode)

Before transmitting, receiving, or changing the mode or communication format, the software must clear the TE and RE bits to 0 in the serial control register (SCSCR), then initialize the SCIF. Clearing TE to 0 initializes the transmit shift register (SCTSR). Clearing RE to 0, however, does not initialize the RDF, PER, FER, and ORER flags and receive data register (SCRDR), which retain their previous contents.

(3) LSB First Transfer (32-Bit Data)

Figure 18.14 shows the operation of the RSPI data register (SPDR) and the shift register when the RSPI performs a 32-bit data length LSB-first data transfer.

The CPU or the DTC/DMAC writes T31 to T00 to the transmit buffer of SPDR. If the SPTEF bit in the RSPI status register (SPSR) is 0 and the shift register is empty, the RSPI reverses the order of the bits of the data in the transmit buffer of SPDR, copies it to the shift register, and fully populates the shift register. When serial transfer starts, the RSPI outputs data from the MSB (bit 31) of the shift register, and shifts in the data from the LSB (bit 0) of the shift register. When the RSPCK cycle required for the serial transfer of 32 bits has passed, data R00 to R31 is stored in the shift register. In this state, the RSPI copies the data, in which the order of the bits is reversed, from the shift register to the receive buffer of SPDR, and empties the shift register.

If another serial transfer is started before the CPU or the DTC/DMAC writes to the transmit buffer of SPDR, received data R00 to R31 is shifted out from the shift register.

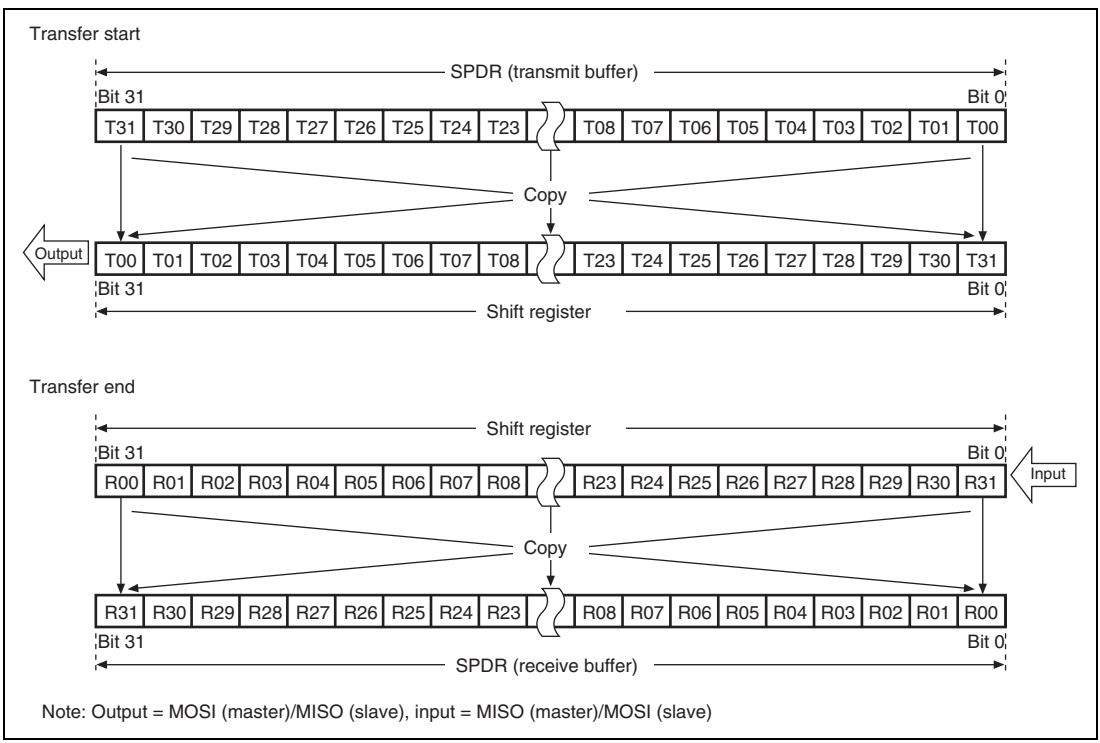
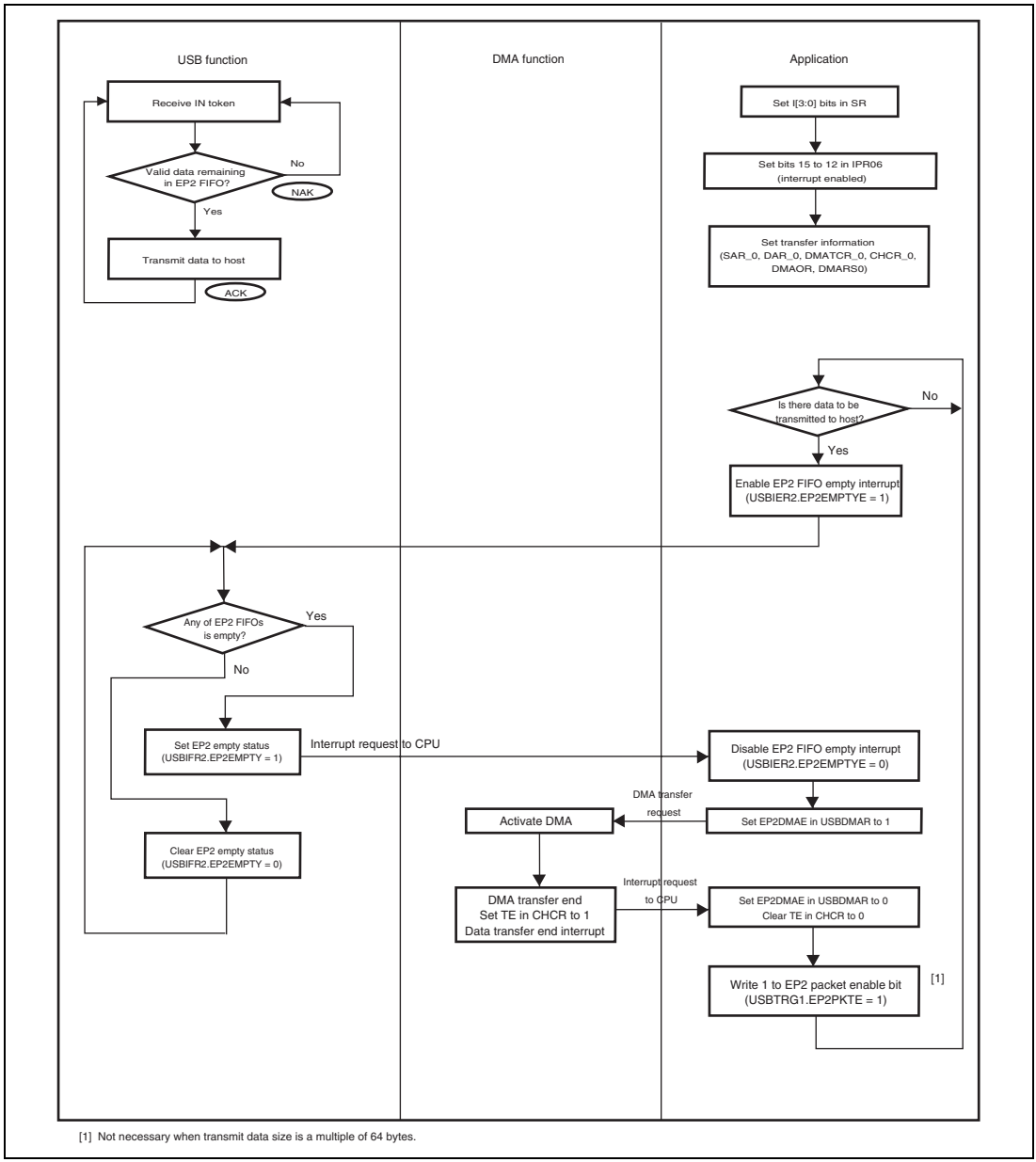


Figure 18.14 LSB First Transfer (32-Bit Data)

Bit	Bit Name	Initial Value	R/W	Description
5	EP8STLC	0	W	EP8 Stall Clear Writing 1 to this bit clears the EP8STLS bit to 0. This bit cannot be cleared to 0.
4	EP7STLC	0	W	EP7 Stall Clear Writing 1 to this bit clears the EP7STLS bit to 0. This bit cannot be cleared to 0.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	EP9STLS	0	R/W	EP9 Stall Setting Writing 1 to this bit places endpoint 9 in the stall state. This bit cannot be cleared to 0.
1	EP8STLS	0	R/W	EP8 Stall Setting Writing 1 to this bit places endpoint 8 in the stall state. This bit cannot be cleared to 0.
0	EP7STLS	0	R/W	EP7 Stall Setting Writing 1 to this bit places endpoint 7 in the stall state. This bit cannot be cleared to 0.



[1] Not necessary when transmit data size is a multiple of 64 bytes.

Figure 24.21 Example of DMA Transfer (Channel 0) for Bulk-IN Transfer (EP2) (When Transmit Data Size Cannot be Determined Before Receiving IN Token)

Command	H'3F	Size	Bit rate	Input frequency
	Clock type count	Multiplication ratio 1	Multiplication ratio 2	
	SUM			
Response	H'06			
Error response	H'BF	Error		
Confirmation	H'06			
Response	H'06			

[Legend]

Size (1 byte): Total number of bytes in the bit rate, input frequency, clock type count, and multiplication ratio fields

Bit rate (2 bytes): New bit rate (for example, H'00C0 indicates 19200 bps)

1/100 of the new bit rate value should be specified.

Input frequency (2 bytes): Clock frequency input to this LSI (for example, H'07D0 indicates 20.00 MHz)

This value should be calculated by multiplying the input frequency value to two decimal places by 100.

Clock type count (1 byte): Number of clock types (for example, H'02 indicates two clock types; that is, an internal clock and a peripheral clock)

Multiplication ratio 1 (1 byte): Multiplication/division ratio of the input frequency to obtain the internal clock

A positive value indicates a multiplication ratio (for example, H'04 = 4 = multiplication by 4)

A negative value indicates a division ratio (for example, HFE = -2 = division by 2)

Multiplication 2 (1 byte): Multiplication/division ratio of the input frequency to obtain the peripheral clock

This value is represented in the same format as multiplication ratio 1

SUM (1 byte): Checksum

To make sure that the FCU accepts a command, enter the mode in which the FCU can accept the target command, check the FRDY, ILGLERR, ERSERR, and PRGERR bit values in FSTATR0, and the FCUERR bit value in FSTATR1, and then issue the target FCU command. The CMDLK bit in FASTAT holds a value obtained by logical ORing the ILGLERR, ERSERR, and PRGERR bit values in FSTATR0 and the FCUERR bit value in the FSTATR1. Therefore the FCU's error occurrence state can be checked by reading the CMDLK bit. In table 27.13, the CMDLK bit is used as the bit to indicate the error occurrence state. The FRDY bit of FSTATR0 is 0 during the programming/erasure, programming/erasure suspension, and lock bit read 2 processes. While the FRDY bit is 0, the P/E suspend command can be accepted only when the SUSRDY bit in FSTATR0 is 1.

Table 27.13 includes 0 and 1 in single cells of the ERSSPD, PRGSPD, and FRDY bit rows for the sake of simplification. The ERSSPD bits 1 and 0 indicate the erasure suspension and programming suspension processes, respectively. The PRGSPD bits 1 and 0 indicate the programming suspension and erasure suspension processes, respectively. The FRDY bit value can be either 1 or 0, which is a value held by the bit prior to a transition to the command lock state.

33.3.3 Bus Timing

Table 33.7 Bus Timing

Conditions: $V_{cc}Q = PLLV_{cc} = DrV_{cc} = 3.0$ to 3.6 V, $AV_{cc} = AVREF = 4.5$ V to 5.5 V,
$V_{ss} = PLLV_{ss} = DrV_{ss} = AVREFVSS = AV_{ss} = 0$ V,
Ta = –40°C to +85°C (Industrial specifications)

		Bϕ = 50 MHz*[1]			
Item	**Symbol**	**Min.**	**Max.**	**Unit**	**Figure**
Address delay time 1	t_{AD1}	1	18	ns	Figures 33.10 to 33.34
Address delay time 2	t_{AD2}	$1/2t_{cyc} + 1$	$1/2t_{cyc} + 18$	ns	Figure 33.17
Address delay time 3	t_{AD3}	$1/2t_{cyc} + 1$	$1/2t_{cyc} + 18$	ns	Figures 33.35, 33.36
Address setup time	t_{AS}	0	—	ns	Figures 33.10 to 33.13, 33.17
Address hold time	t_{AH}	0	—	ns	Figures 33.10 to 33.13
$\overline{BS}$ delay time	t_{BSD}	—	18	ns	Figures 33.10 to 33.31, 33.35
$\overline{CS}$ delay time 1	t_{CSD1}	1	18	ns	Figures 33.10 to 33.34
$\overline{CS}$ delay time 2	t_{CSD2}	$1/2t_{cyc} + 1$	$1/2t_{cyc} + 18$	ns	Figures 33.35, 33.36
$\overline{CS}$ setup time	t_{CSS}	0	—	ns	Figures 33.10 to 33.13
$\overline{CS}$ hold time	t_{CSH}	0	—	ns	Figures 33.10 to 33.13
Read write delay time 1	t_{RWD1}	1	18	ns	Figures 33.10 to 33.34
Read write delay time 2	t_{RWD2}	$1/2t_{cyc} + 1$	$1/2t_{cyc} + 18$	ns	Figures 33.35, 33.36
Read strobe delay time	t_{RSD}	$1/2t_{cyc} + 1$	$1/2t_{cyc} + 18$	ns	Figures 33.10 to 33.14, 33.17
Read data setup time 1	t_{RDS1}	$1/2t_{cyc} + 14$	—	ns	Figures 33.10 to 33.14, 33.16
Read data setup time 2	t_{RDS2}	14	—	ns	Figures 33.18 to 33.21, 33.26 to 33.28
Read data setup time 3	t_{RDS3}	$1/2t_{cyc} + 14$	—	ns	Figure 33.17
Read data setup time 4	t_{RDS4}	$1/2t_{cyc} + 14$	—	ns	Figure 33.35