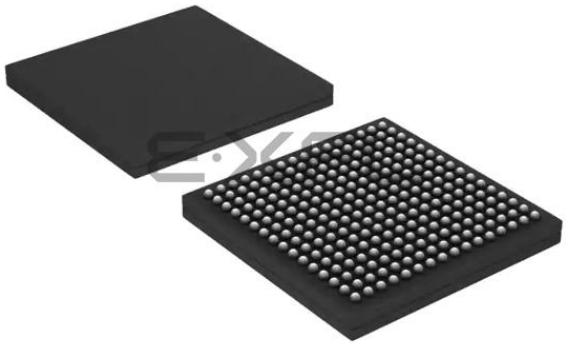

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Details	
Product Status	Active
Core Processor	Coldfire V4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	I²C, SPI, SSI, UART/USART, USB OTG
Peripherals	DMA, WDT
Number of I/O	132
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf54451cvm180

Table 3. Special-Case Default Signal Functionality (continued)

Pin	256 MAPBGA	360 TEPBGA
$\overline{\text{PCI\_GNT}}$[3:0]	GPIO	$\overline{\text{PCI\_GNT}}$[3:0]
$\overline{\text{PCI\_REQ}}$[3:0]	GPIO	$\overline{\text{PCI\_REQ}}$[3:0]
$\overline{\text{IRQ1}}$	GPIO	$\overline{\text{PCI\_INTA}}$ and configured as an agent.
ATA_RESET	GPIO	ATA reset

Table 4. MCF5445*x* Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
Reset								
$\overline{\text{RESET}}$	—	—	—	U	I	EVDD	L4	Y18
$\overline{\text{RSTOUT}}$	—	—	—	—	O	EVDD	M15	B17
Clock								
EXTAL/PCI_CLK	—	—	—	—	I	EVDD	M16	A16
XTAL	—	—	—	U[3]	O	EVDD	L16	A17
Mode Selection								
BOOTMOD[1:0]	—	—	—	—	I	EVDD	M5, M7	AB17, AB21
FlexBus								
FB_AD[31:24]	PFBADH[7:0][4]	FB_D[31:24]	—	—	I/O	EVDD	A14, A13, D12, C12, B12, A12, D11, C11	J2, K4, J1, K1–3, L1, L4
FB_AD[23:16]	PFBADMH[7:0][4]	FB_D[23:16]	—	—	I/O	EVDD	B11, A11, D10, C10, B10, A10, D9, C9	L2, L3, M1–4, N1–2
FB_AD[15:8]	PFBADML[7:0][4]	FB_D[15:8]	—	—	I/O	EVDD	B9, A9, D8, C8, B8, A8, D7, C7	P1–2, R1–3, P4, T1–2
FB_AD[7:0]	PFBADL[7:0][4]	FB_D[7:0]	—	—	I/O	EVDD	B7, A7, D6, C6, B6, A6, D5, C5	T3–4, U1–3, V1–2, W1
$\overline{\text{FB\_BE/BWE}}$[3:2]	PBE[3:2]	FB_TSIZ[1:0]	—	—	O	EVDD	B5, A5	Y1, W2
$\overline{\text{FB\_BE/BWE}}$[1:0]	PBE[1:0]	—	—	—	O	EVDD	B4, A4	W3, Y2
FB_CLK	—	—	—	—	O	EVDD	B13	J3
$\overline{\text{FB\_CS}}$[3:1]	PCS[3:1]	—	—	—	O	EVDD	C2, D4, C3	W5, AA4, AB3
$\overline{\text{FB\_CS0}}$	—	—	—	—	O	EVDD	C4	Y4
$\overline{\text{FB\_OE}}$	PFBCTL3	—	—	—	O	EVDD	A2	AA1
FB_R/$\overline{\text{W}}$	PFBCTL2	—	—	—	O	EVDD	B2	AA3
$\overline{\text{FB\_TA}}$	PFBCTL1	—	—	U	I	EVDD	B1	AB2

Table 4. MCF5445*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
FB_TS	PFBCTL0	FB_ALE	FB_TBST	—	O	EVDD	A3	Y3
PCI Controller[5]								
PCI_AD[31:0]	—	FB_A[31:0]	—	—	I/O	EVDD	—	C11, D11, A10, B10, J4, G2, G3, F1, D12, C12, B12, A11, B11, B9, D9, D10, A8, B8, A5, B5, A4, A3, B3, D4, D3, E3–E1, F3, C2, D2, C1
—	—	FB_A[23:0]	—	—	I/O	EVDD	K14–13, J15–13, H13–15, G15–13, F14–13, E15–13, D16, B16, C15, B15, C14, D15, C16, D14	—
PCI_CBE[3:0]	—	—	—	—	I/O	EVDD	—	G4, E4, D1, B1
PCI_DEVSEL	—	—	—	—	O	EVDD	—	F2
PCI_FRAME	—	—	—	—	I/O	EVDD	—	B2
PCI_GNT3	PPCI7	ATA_DMACK	—	—	O	EVDD	—	B7
PCI_GNT[2:1]	PPCI[6:5]	—	—	—	O	EVDD	—	C8, C9
PCI_GNT0/ PCI_EXTREQ	PPCI4	—	—	—	O	EVDD	—	A9
PCI_IDSEL	—	—	—	—	I	EVDD	—	D5
PCI_IRDY	—	—	—	—	I/O	EVDD	—	C3
PCI_PAR	—	—	—	—	I/O	EVDD	—	C4
PCI_PERR	—	—	—	—	I/O	EVDD	—	B4
PCI_REQ3	PPCI3	ATA_INTRQ	—	—	I	EVDD	—	C7
PCI_REQ[2:1]	PPCI[2:1]	—	—	—	I	EVDD	—	D7, C5
PCI_REQ0/ PCI_EXTGNT	PPCI0	—	—	—	I	EVDD	—	A2
PCI_RST	—	—	—	—	O	EVDD	—	B6
PCI_SERR	—	—	—	—	I/O	EVDD	—	A6
PCI_STOP	—	—	—	—	I/O	EVDD	—	A7
PCI_TRDY	—	—	—	—	I/O	EVDD	—	C10
SDRAM Controller								
SD_A[13:0]	—	—	—	—	O	SDVDD	R1, P1, N2, P2, R2, T2, M4, N3, P3, R3, T3, T4, R4, N4	V22, U20–22, T19–22, R20–22, N19, P20–21

Table 4. MCF5445*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
FEC0_TXCLK	PFEC0H7	FEC0_RMII_ REF_CLK	—	—	I	EVDD	H4	Y10
FEC0_TXD[3:2]	PFEC0L[7:6]	—	ULPI_DATA[3:2]	—	O	EVDD	J1, J2	W10, AB11
FEC0_TXD1	PFEC0L5	FEC0_RMII_TXD1	—	—	O	EVDD	J3	AA11
FEC0_TXD0	PFEC0H5	FEC0_RMII_TXD0	—	—	O	EVDD	J4	Y11
FEC0_TXEN	PFEC0H6	FEC0_RMII_TXEN	—	—	O	EVDD	K1	W11
FEC0_TXER	PFEC0L4	—	ULPI_DATA0	—	O	EVDD	K2	AB12
FEC1								
FEC1_MDC	PFECI2C5	—	$\overline{\text{ATA\_DIOR}}$	—	O	EVDD	—	W20
FEC1_MDIO	PFECI2C4	—	$\overline{\text{ATA\_DIOW}}$	—	I/O	EVDD	—	Y22
FEC1_COL	PFEC1H4	—	ATA_DATA7	—	I	EVDD	—	AB18
FEC1_CRS	PFEC1H0	—	ATA_DATA6	—	I	EVDD	—	AA18
FEC1_RXCLK	PFEC1H3	—	ATA_DATA5	—	I	EVDD	—	W14
FEC1_RXDV	PFEC1H2	FEC1_RMII_ CRS_DV	ATA_DATA15	—	I	EVDD	—	AB15
FEC1_RXD[3:2]	PFEC1L[3:2]	—	ATA_DATA[4:3]	—	I	EVDD	—	AA15, Y15
FEC1_RXD1	PFEC1L1	FEC1_RMII_RXD1	ATA_DATA14	—	I	EVDD	—	AA17
FEC1_RXD0	PFEC1H1	FEC1_RMII_RXD0	ATA_DATA13	—	I	EVDD	—	Y17
FEC1_RXER	PFEC1L0	FEC1_RMII_RXER	ATA_DATA12	—	I	EVDD	—	W17
FEC1_TXCLK	PFEC1H7	FEC1_RMII_ REF_CLK	ATA_DATA11	—	I	EVDD	—	AB19
FEC1_TXD[3:2]	PFEC1L[7:6]	—	ATA_DATA[2:1]	—	O	EVDD	—	Y19, W18
FEC1_TXD1	PFEC1L5	FEC1_RMII_TXD1	ATA_DATA10	—	O	EVDD	—	AA19
FEC1_TXD0	PFEC1H5	FEC1_RMII_TXD0	ATA_DATA9	—	O	EVDD	—	Y20
FEC1_TXEN	PFEC1H6	FEC1_RMII_TXEN	ATA_DATA8	—	O	EVDD	—	AA21
FEC1_TXER	PFEC1L4	—	ATA_DATA0	—	O	EVDD	—	AA22
USB On-the-Go								
USB_DM	—	—	—	—	O	USB VDD	F16	A14
USB_DP	—	—	—	—	O	USB VDD	E16	A15
USB_VBUS_EN	PUSB1	USB_PULLUP	ULPI_NXT	—	O	USB VDD	E5	AA2
USB_VBUS_OC	PUSB0	—	ULPI_STP	UD[7]	I	USB VDD	B3	V4

Table 4. MCF5445*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
DSPI_SIN	PDSPI1	SBF_DI	—	[8]	I	EVDD	P15	B19
DSPI_SOUT	PDSPI0	SBF_DO	—	—	O	EVDD	N13	C20
UARTs								
$\overline{\text{U1CTS}}$	PUART7	—	—	—	I	EVDD	—	V3
$\overline{\text{U1RTS}}$	PUART6	—	—	—	O	EVDD	—	U4
U1RXD	PUART5	—	—	—	I	EVDD	—	P3
U1TXD	PUART4	—	—	—	O	EVDD	—	N3
$\overline{\text{U0CTS}}$	PUART3	—	—	—	I	EVDD	M3	Y16
$\overline{\text{U0RTS}}$	PUART2	—	—	—	O	EVDD	M2	AA16
U0RXD	PUART1	—	—	—	I	EVDD	N1	AB16
U0TXD	PUART0	—	—	—	O	EVDD	M1	W15
Note: The UART1 and UART 2 signals are multiplexed on the DMA timers and I2C pins.								
DMA Timers								
DT3IN	PTIMER3	DT3OUT	U2RXD	—	I	EVDD	C13	H2
DT2IN	PTIMER2	DT2OUT	U2TXD	—	I	EVDD	D13	H1
DT1IN	PTIMER1	DT1OUT	$\overline{\text{U2CTS}}$	—	I	EVDD	B14	H3
DT0IN	PTIMER0	DT0OUT	$\overline{\text{U2RTS}}$	—	I	EVDD	A15	G1
BDM/JTAG[9]								
PSTDDATA[7:0]	—	—	—	—	O	EVDD	E2, D1, F4, E3, D2, C1, E4, D3	AA6, AB6, AB5, W6, Y6, AA5, AB4, Y5
JTAG_EN	—	—	—	D	I	EVDD	M11	C21
PSTCLK	—	TCLK	—	—	I	EVDD	P13	C22
DSI	—	TDI	—	U	I	EVDD	T15	C19
DSO	—	TDO	—	—	O	EVDD	T14	A21
$\overline{\text{BKPT}}$	—	TMS	—	U	I	EVDD	R14	B21
DSCLK	—	$\overline{\text{TRST}}$	—	U	I	EVDD	M13	B22
Test								
TEST	—	—	—	D	I	EVDD	M6	AB20
PLLTEST	—	—	—	—	O	EVDD	K16	D15

Table 4. MCF5445*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
Power Supplies								
IVDD	—	—	—	—	—	—	E6–12, F5, F12	D6, D8, D14, F4, H4, N4, R4, W4, W7, W8, W12, W16, W19
EVDD	—	—	—	—	—	—	G5, G12, H5, H12, J5, J12, K5, K12, L5–6, L12	D13, D19, G8, G11, G14, G16, J7, J16, L7, L16, N16, P7, R16, T8, T12, T14, T16
SD_VDD	—	—	—	—	—	—	L7–11, M9, M10	F19, H19, K19, M19, R19, U19
VDD_OSC	—	—	—	—	—	—	L14	B16
VDD_A_PLL	—	—	—	—	—	—	K15	C14
VDD_RTC	—	—	—	—	—	—	M12	C13
VSS	—	—	—	—	—	—	A1, A16, F6–11, G6–11, H6–11, J6–11, K6–11, T1, T16	A1, A22, B14, G7, G9–10, G12–13, G15, H7, H16, J9–14, K7, K9–14, K16, L9–14, M7, M9–M14, M16, N7, N9–14, P9–14, P16, R7, T7, T9–11, T13, T15, AB1, AB22
VSS_OSC	—	—	—	—	—	—	L15	C16

1 Pull-ups are generally only enabled on pins with their primary function, except as noted.

2 Refers to pin's primary function.

3 Enabled only in oscillator bypass mode (internal crystal oscillator is disabled).

4 Serial boot must select 0-bit boot port size to enable the GPIO mode on these pins.

5 When the PCI is enabled, all PCI bus pins come up configured as such. This includes the PCI_GNT and PCI_REQ lines, which have GPIO. The IRQ1/$\overline{\text{PCI\_INTA}}$ signal is a special case. It comes up as $\overline{\text{PCI\_INTA}}$ when booting as a PCI agent and as GPIO when booting as a PCI host.
For the 360 TEPBGA, booting with PCI disabled results in all dedicated PCI pins being safe-stated. The $\overline{\text{PCI\_GNT}}$ and $\overline{\text{PCI\_REQ}}$ lines and IRQ1/$\overline{\text{PCI\_INTA}}$ come up as GPIO.

6 GPIO functionality is determined by the edge port module. The pin multiplexing and control module is only responsible for assigning the alternate functions.

7 Depends on programmed polarity of the USB_VBUS_OC signal.

8 Pull-up when the serial boot facility (SBF) controls the pin

9 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The pin multiplexing and control module is not responsible for assigning these pins.

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

5.3 ESD Protection

Table 7. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 8. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Units
Internal logic supply voltage[1]	IV_{DD}	1.35	1.65	V
PLL analog operation voltage range [1]	PV_{DD}	1.35	1.65	V
External I/O pad supply voltage	EV_{DD}	3.0	3.6	V
Internal oscillator supply voltage	$OSCV_{DD}$	3.0	3.6	V
Real-time clock supply voltage	$RTCV_{DD}$	1.35	1.65	V
SDRAM I/O pad supply voltage — DDR mode	SDV_{DD}	2.25	2.75	V
SDRAM I/O pad supply voltage — DDR2 mode	SDV_{DD}	1.7	1.9	V
SDRAM I/O pad supply voltage — Mobile DDR mode	SDV_{DD}	1.7	1.9	V
SDRAM input reference voltage	SDV_{REF}	0.49 x SDV_{DD}	0.51 x SDV_{DD}	V
Input High Voltage	V_{IH}	0.7 x EV_{DD}	3.65	V
Input Low Voltage	V_{IL}	V_{SS} – 0.3	0.35 x EV_{DD}	V
Input Hysteresis	V_{HYS}	0.06 x EV_{DD}	—	mV
Input Leakage Current[2] V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–2.5	2.5	µA
Input Leakage Current[3] V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–5	5	µA
High Impedance (Off-State) Leakage Current[4] V_{in} = V_{DD} or V_{SS}, All input/output and output pins	I_{OZ}	–10.0	10.0	µA
Output High Voltage (All input/output and all output pins) I_{OH} = –5.0 mA	V_{OH}	0.85 × EV_{DD}	—	V
Output Low Voltage (All input/output and all output pins) I_{OL} = 5.0mA	V_{OL}	—	0.15 × EV_{DD}	V

Table 10. PLL Electrical Characteristics (continued)

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
11	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
12	Crystal capacitive load	C_L	See crystal spec		
13	Discrete load capacitance for XTAL Discrete load capacitance for EXTAL	C_{L_XTAL} C_{L_EXTAL}	—	$2 \times (C_L - C_{S\_XTAL} - C_{S\_EXTAL} - C_{S\_PCB})$[6]	pF
14	Frequency un-LOCK Range	f_{UL}	-4.0	4.0	% f_{sys}
15	Frequency LOCK Range	f_{LCK}	-2.0	2.0	% f_{sys}
17	CLKOUT Period Jitter, [3, 4, 7] Measured at f_{SYS} Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter	C_{jitter}	 — —	 10 TBD	 % FB_CLK % FB_CLK

1 The minimum system frequency is the minimum input clock divided by the maximum low-power divider (16 MHz ÷ 32,768). When the PLL is enabled, the minimum system frequency (f_{sys}) is 150 MHz.

2 This parameter is guaranteed by characterization before qualification rather than 100% tested. Applies to external clock reference only.

3 Proper PC board layout procedures must be followed to achieve specifications.

4 This parameter is guaranteed by design rather than 100% tested.

5 This specification is the PLL lock time only and does not include oscillator start-up time.

6 C_{S_PCB} is the measured PCB stray capacitance on EXTAL and XTAL.

7 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD}, EV_{DD}, and V_{SS} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

5.6 Reset Timing Specifications

Table 11 lists specifications for the reset timing parameters shown in Figure 8.

Table 11. Reset and Configuration Override Timing

Num	Characteristic	Min	Max	Unit
R1[1]	$\overline{\text{RESET}}$ valid to CLKIN (setup)	9	—	ns
R2	CLKIN to $\overline{\text{RESET}}$ invalid (hold)	1.5	—	ns
R3	$\overline{\text{RESET}}$ valid time[2]	5	—	CLKIN cycles
R4	CLKIN to $\overline{\text{RSTOUT}}$ valid	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Configuration Override inputs valid	0	—	ns
R6	Configuration Override inputs valid to $\overline{\text{RSTOUT}}$ invalid (setup)	20	—	CLKIN cycles
R7	Configuration Override inputs invalid after $\overline{\text{RSTOUT}}$ invalid (hold)	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override inputs High Impedance	—	1	CLKIN cycles

1 $\overline{\text{RESET}}$ and Configuration Override data lines are synchronized internally. Setup and hold times must be met only if recognition on a particular clock is required.

2 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

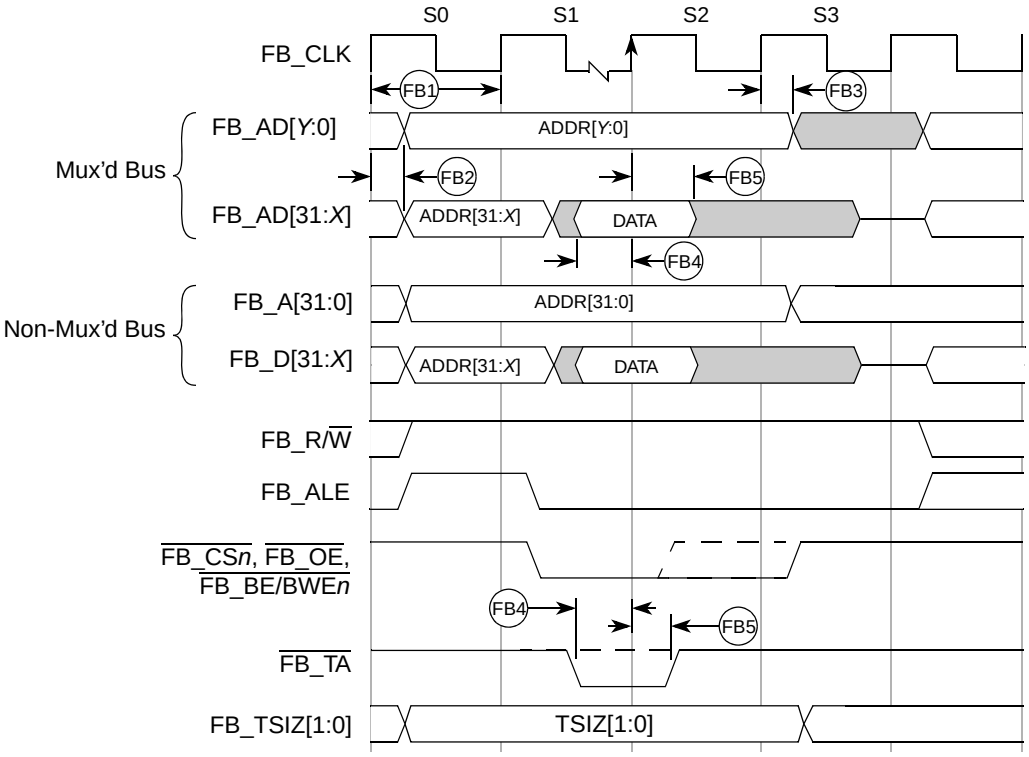

Figure 9. FlexBus Read Timing

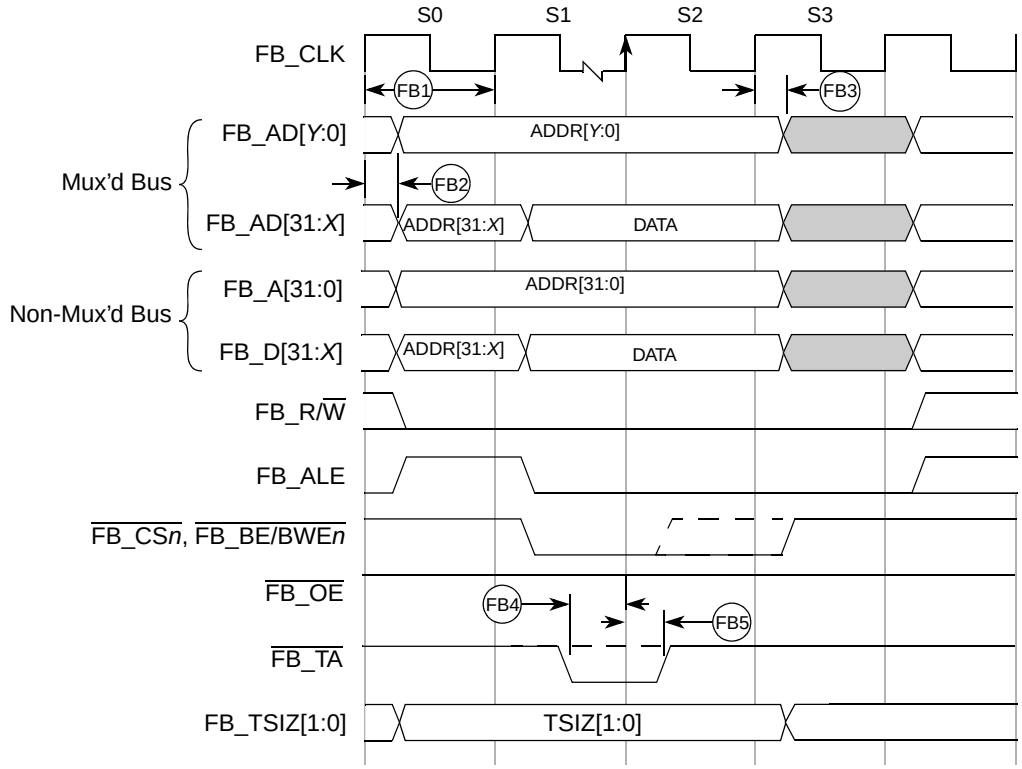

Figure 10. Flexbus Write Timing

Table 14. PCI Timing Specifications[1,2] (continued)

Num	Characteristic	33 MHz[3]		66 MHz[3]		
		Min	Max	Min	Max	Unit
P6	$\overline{\text{PCI\_REQ}}$[3:0]/$\overline{\text{PCI\_GNT}}$[3:0] — output valid	—	12.0	—	6.0	ns
P7	All PCI signals — output hold	2.0	—	1.0	—	ns

1 The PCI bus operates at the CLKIN frequency. All timings are relative to the input clock, CLKIN.

2 All PCI signals are bused signals except for PCI_GNT[3:0] and PCI_REQ[3:0]. These signals are defined as point-to-point signals by the PCI Specification.

3 The 66-MHz parameters are only guaranteed when the 66-MHz PCI pad slew rates are selected. Likewise, the 33-MHz parameters are only guaranteed when the 33-MHz PCI pad slew rates are selected.

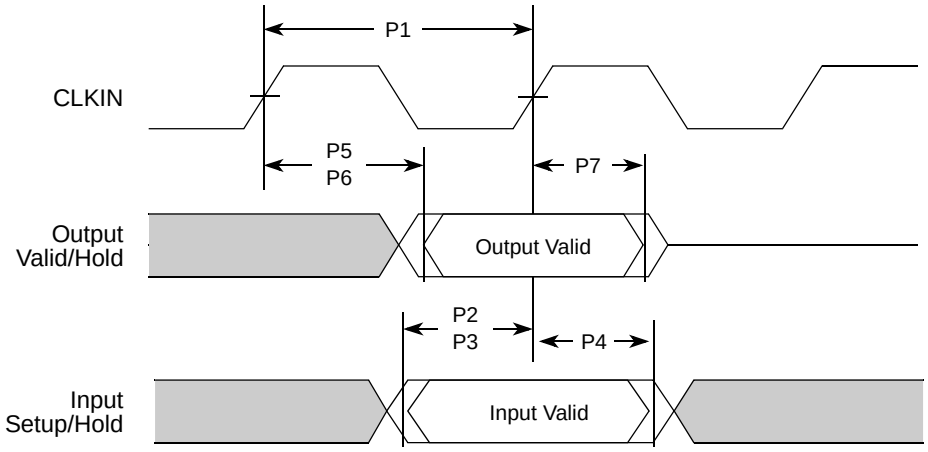

Figure 13. PCI Timing

5.9.1 Overshoot and Undershoot

Figure 14 shows the specification limits for overshoot and undershoot for PCI I/O. To guarantee long term reliability, the specification limits shown must be followed. Good transmission line design practices should be observed to guarantee the specification limits.

Table 17. SSI Timing—Slave Modes[1]

Num	Description	Symbol	Min	Max	Units	Notes
S11	SSI_BCLK cycle time	t_{BCLK}	$8 \times t_{SYS}$	—	ns	
S12	SSI_BCLK pulse width high / low		45%	55%	t_{BCLK}	
S13	SSI_FS input setup before SSI_BCLK		10	—	ns	
S14	SSI_FS input hold after SSI_BCLK		2	—	ns	
S15	SSI_BCLK to SSI_TXD / SSI_FS output valid		—	15	ns	
S16	SSI_BCLK to SSI_TXD / SSI_FS output invalid / high impedence		0	—	ns	
S17	SSI_RXD setup before SSI_BCLK		10	—	ns	
S18	SSI_RXD hold after SSI_BCLK		2	—	ns	

1 All timings specified with a capactive load of 25pF.

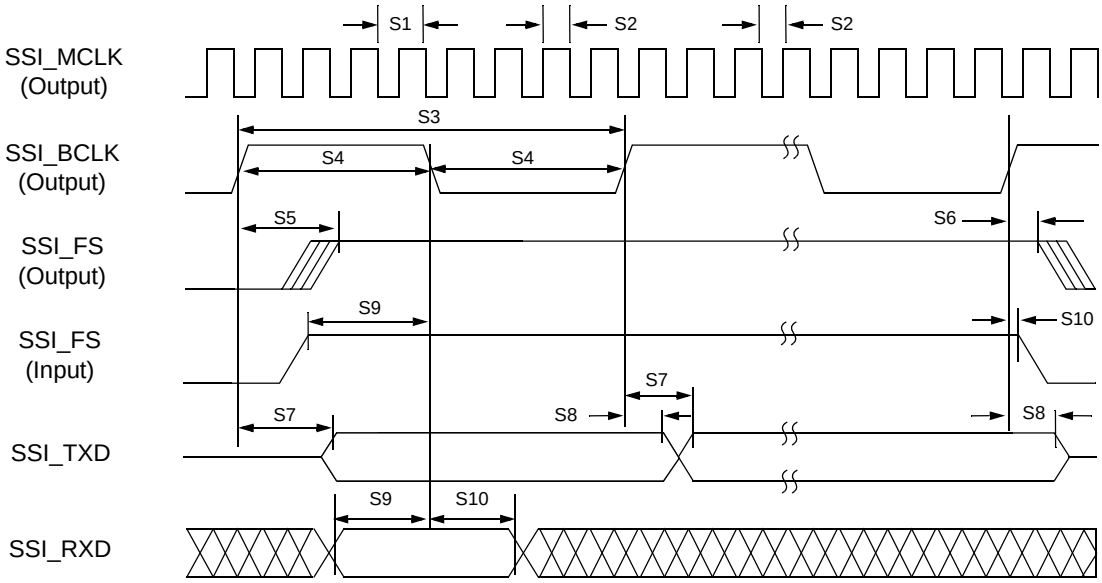

Figure 16. SSI Timing—Master Modes

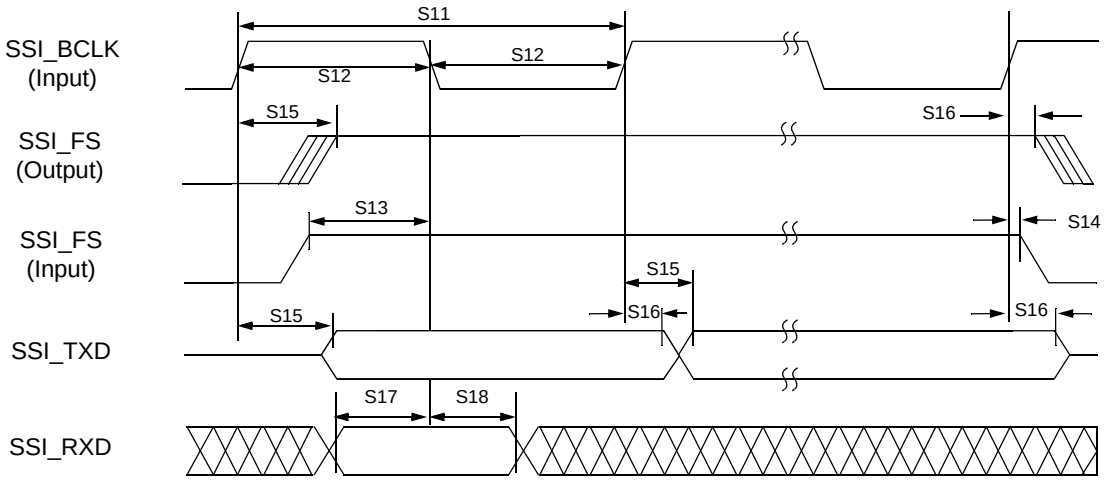

Figure 17. SSI Timing—Slave Modes

5.12 I²C Timing Specifications

Table 18 lists specifications for the I²C input timing parameters shown in Figure 18.

Table 18. I²C Input Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	t_{SYS}
I2	Clock low period	8	—	t_{SYS}
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4	—	t_{SYS}
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	t_{SYS}
I9	Stop condition setup time	2	—	t_{SYS}

Table 19 lists specifications for the I²C output timing parameters shown in Figure 18.

Table 19. I²C Output Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	6	—	t_{SYS}
I2[1]	Clock low period	10	—	t_{SYS}
I3[2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4[1]	Data hold time	7	—	t_{SYS}
I5[3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns

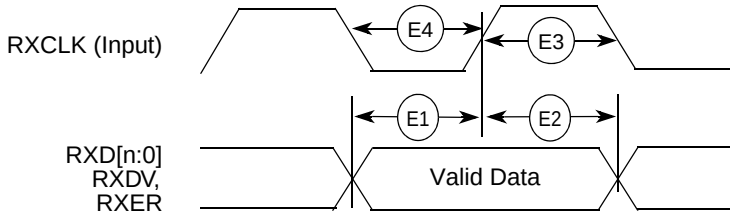

Figure 19. MII Receive Signal Timing Diagram

5.13.2 Transmit Signal Timing Specifications

Table 21. Transmit Signal Timing

Num	Characteristic	MII Mode		RMII Mode		Unit
		Min	Max	Min	Max	
—	TXCLK frequency	—	25	—	50	MHz
E5	TXCLK to TXD[n:0], TXEN, TXER invalid[1]	5	—	5	—	ns
E6	TXCLK to TXD[n:0], TXEN, TXER valid[1]	—	25	—	14	ns
E7	TXCLK pulse width high	35%	65%	35%	65%	t_{TXCLK}
E8	TXCLK pulse width low	35%	65%	35%	65%	t_{TXCLK}

1 In MII mode, n = 3; In RMII mode, n = 1

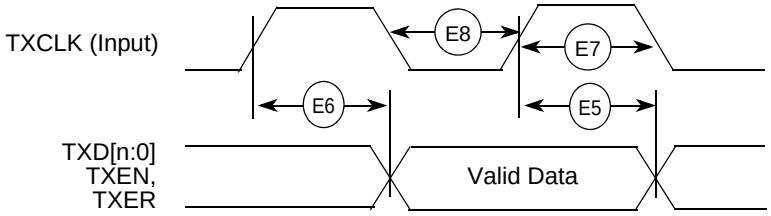

Figure 20. MII Transmit Signal Timing Diagram

5.13.3 Asynchronous Input Signal Timing Specifications

Table 22. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
E9	CRS, COL minimum pulse width	1.5	—	TXCLK period

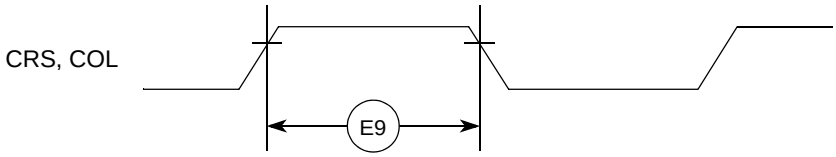

Figure 21. MII Async Inputs Timing Diagram

5.13.4 MII Serial Management Timing Specifications

Table 23. MII Serial Management Channel Signal Timing

Num	Characteristic	Symbol	Min	Max	Unit
E10	MDC cycle time	t_{MDC}	400	—	ns
E11	MDC pulse width		40	60	% t_{MDC}
E12	MDC to MDIO output valid		—	375	ns
E13	MDC to MDIO output invalid		25	—	ns
E14	MDIO input to MDC setup		10	—	ns
E15	MDIO input to MDC hold		0	—	ns

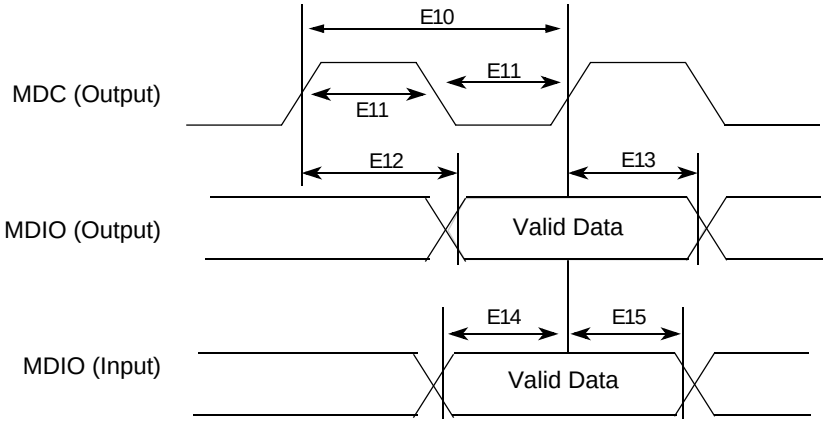

Figure 22. MII Serial Management Channel TIming Diagram

5.14 32-Bit Timer Module Timing Specifications

Table 24 lists timer module AC timings.

Table 24. Timer Module AC Timing Specifications

Name	Characteristic	Min	Max	Unit
T1	DT*n*IN cycle time (*n* = 0:3)	3	—	$t_{sys/2}$
T2	DT*n*IN pulse width (*n* = 0:3)	1	—	$t_{sys/2}$

5.15 ATA Interface Timing Specifications

The ATA controller is compatible with the ATA/ATAPI-6 industry standard. Refer to the *ATA/ATAPI-6 Specficiation* and the ATA controller chapter of the *MCF54455 Reference Manual* for timing diagrams of the various modes of operation.

The timings of the various ATA data transfer modes are determined by a set of timing equations described in the ATA section of the *MCF54455 Reference Manual*. These timing equations must be fulfilled for the ATA host to meet timing. Table 25 provides implementation specific timing parameters necessary to complete the timing equations.

Table 25. ATA Interface Timing Specifications[1,2]

Name	Characteristic	Symbol	Min	Max	Unit	Notes
A1	Setup time — ATA_IORDY to SYSCLK falling	t_{SUI}	4.0	—	ns	
A2	Hold time — ATA_IORDY from SYSCLK falling	t_{HI}	3.0	—	ns	
A3	Setup time — ATA_DATA[15:0] to SYSCLK rising	t_{SU}	4.0	—	ns	
A4	Propagation delay — SYSCLK rising to all outputs	t_{CO}	—	7.0	ns	3
A5	Output skew	t_{SKEW1}	—	1.5	ns	3
A6	Setup time — ATA_DATA[15:0] valid to ATA_IORDY	t_{I_DS}	2.0	—	ns	4
A7	Hold time — ATA_IORDY to ATA_DATA[15:0] invalid	t_{I_DH}	3.5	—	ns	4

1 These parameters are guaranteed by design and not testable.

2 All timings specified with a capacitive load of 40pF.

3 Applies to $\overline{\text{ATA\_CS}}$[1:0], ATA_DA[2:0], ATA_DIOR, ATA_DIOW, ATA_DMACK, ATA_DATA[15:0]

4 Applies to Ultra DMA data-in burst only

5.16 DSPI Timing Specifications

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. Table 26 provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the *MCF54455 Reference Manual* for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 26. DSPI Module AC Timing Specifications[1]

Name	Characteristic	Symbol	Min	Max	Unit	Notes
DS1	DSPI_SCK Cycle Time	t_{SCK}	4 x t_{SYS}	—	ns	2
DS2	DSPI_SCK Duty Cycle	—	(t_{sck} ÷ 2) - 2.0	(t_{sck} ÷ 2) + 2.0	ns	3
Master Mode						
DS3	DSPI_PCS*n* to DSPI_SCK delay	t_{CSC}	(2 × t_{SYS}) - 1.5	—	ns	4
DS4	DSPI_SCK to DSPI_PCS*n* delay	t_{ASC}	(2 × t_{SYS}) - 3.0	—	ns	5
DS5	DSPI_SCK to DSPI_SOUT valid	—	—	5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	—	-5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	—	9	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	—	0	—	ns	
Slave Mode						
DS9	DSPI_SCK to DSPI_SOUT valid	—	—	10	ns	

5.19 JTAG and Boundary Scan Timing

Table 29. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Min	Max	Unit
J1	TCLK Frequency of Operation	DC	20	MHz
J2	TCLK Cycle Period	50	—	ns
J3	TCLK Clock Pulse Width	20	30	ns
J4	TCLK Rise and Fall Times	—	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	5	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	20	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	—	33	ns
J8	TCLK Low to Boundary Scan Output High Z	—	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	10	—	ns
J11	TCLK Low to TDO Data Valid	—	11	ns
J12	TCLK Low to TDO High Z	—	11	ns
J13	$\overline{\text{TRST}}$ Assert Time	50	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

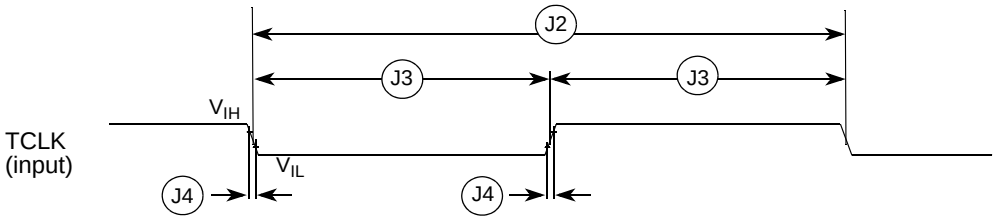

Figure 27. Test Clock Input Timing

5.20 Debug AC Timing Specifications

Table 30 lists specifications for the debug AC timing parameters shown in Figure 31 and Table 32.

Table 30. Debug AC Timing Specification

Num	Characteristic	Min	Max	Units
D0	PSTCLK cycle time	1	1	t_{SYS}
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	1.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4[1]	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

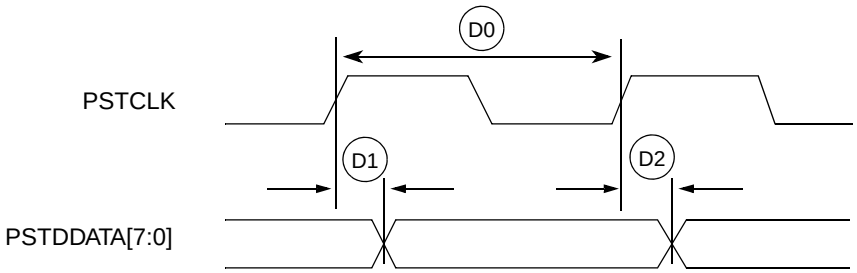

Figure 31. Real-Time Trace AC Timing

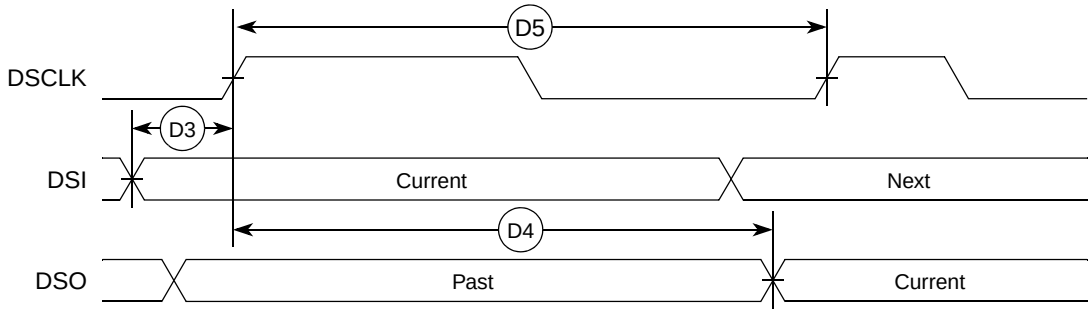

Figure 32. BDM Serial Port AC Timing

6 Power Consumption

All power consumption data is lab data measured on an M54455EVB running the Freescale Linux BSP.

Table 31. MCF4455 Application Power Consumption[1]

Core Freq.		Idle	MP3 Playback	TFTP Download	USB HS File Copy	Units
266 MHz	IV_{DD}	215.6	288.8	274.4	263.7	mA
	EV_{DD}	27.6	33.6	32.6	32.4	
	SDV_{DD}	142.9	158.2	161.1	158.0	
	Total Power	**672**	**829**	**809**	**787**	**mW**
200 MHz	IV_{DD}	163.8	228.0	213.8	207.9	mA
	EV_{DD}	29.9	34.7	34.3	33.8	
	SDV_{DD}	142.2	158.5	160.0	153.4	
	Total Power	**601**	**742**	**722**	**699**	**mW**

1 All voltage rails at nominal values: IV_{DD} = 1.5 V, EV_{DD} = 3.3 V, and SDV_{DD} = 1.8 V.

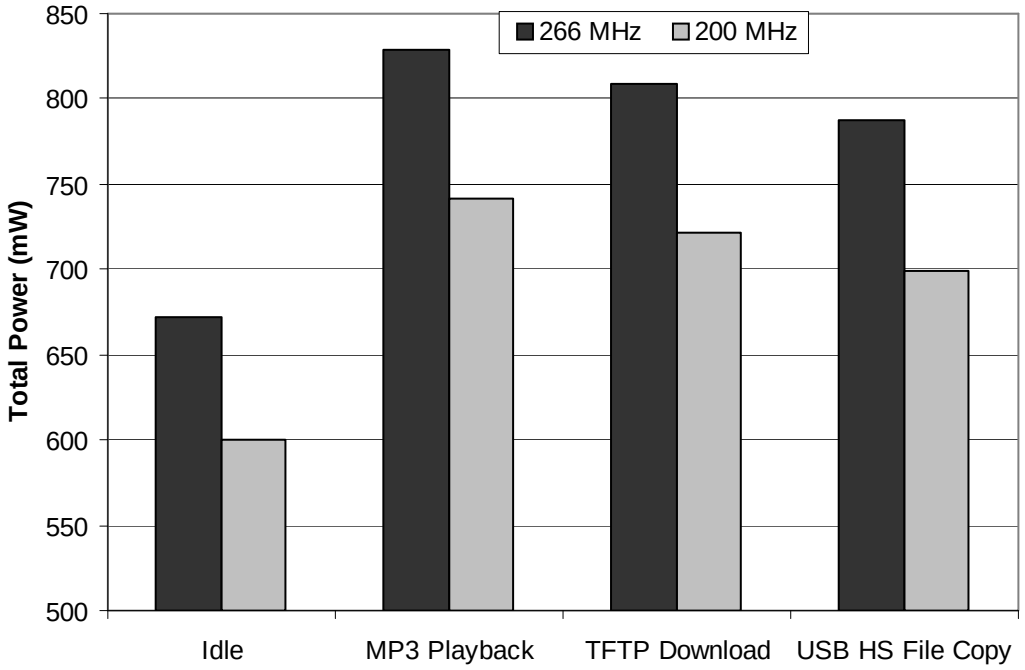

Figure 33. Power Consumption in Various Applications

All current consumption data is lab data measured on a single device using an evaluation board. Table 32 shows the typical power consumption in low-power modes. These current measurements are taken after executing a STOP instruction.

Table 32. Current Consumption in Low-Power Modes[1,2]

Mode	Voltage Supply	System Frequency				
		166 (Typ)[3]	200 (Typ)[3]	233 (Typ)[3]	266 (Typ)[3]	266 (Peak)[4]
RUN	IV_{DD} (mA)	93.4	110.9	128.2	145.4	202.1
	Power (mW)	140.1	166.3	192.4	218.1	303.2
WAIT/DOZE	IV_{DD} (mA)	28.0	32.7	37.5	41.1	100.2
	Power (mW)	42.0	49.1	56.2	61.7	150.3
STOP 0	IV_{DD} (mA)	17.1	19.8	22.5	25.2	25.2
	Power (mW)	25.7	29.7	33.7	37.8	37.8
STOP 1	IV_{DD} (mA)	17.9	19.8	22.4	25.1	25.1
	Power (mW)	26.8	29.6	33.6	37.6	37.6
STOP 2	IV_{DD} (mA)	5.7	5.7	5.7	5.7	5.7
	Power (mW)	8.6	8.6	8.6	8.6	8.6
STOP 3	IV_{DD} (mA)	1.8	1.8	1.8	1.8	1.8
	Power (mW)	2.6	2.6	2.6	2.6	2.6

1 All values are measured on an M54455EVB with 1.5V IV_{DD} power supply. Tests performed at room temperature.

2 Refer to the Power Management chapter in the *MCF54455 Reference Manual* for more information on low-power modes.

3 All peripheral clocks are off except UART0, INTC0, IACK, edge port, reset controller, CCM, PLL, and FlexBus prior to entering low-power mode.

4 All peripheral clocks on prior to entering low-power mode.

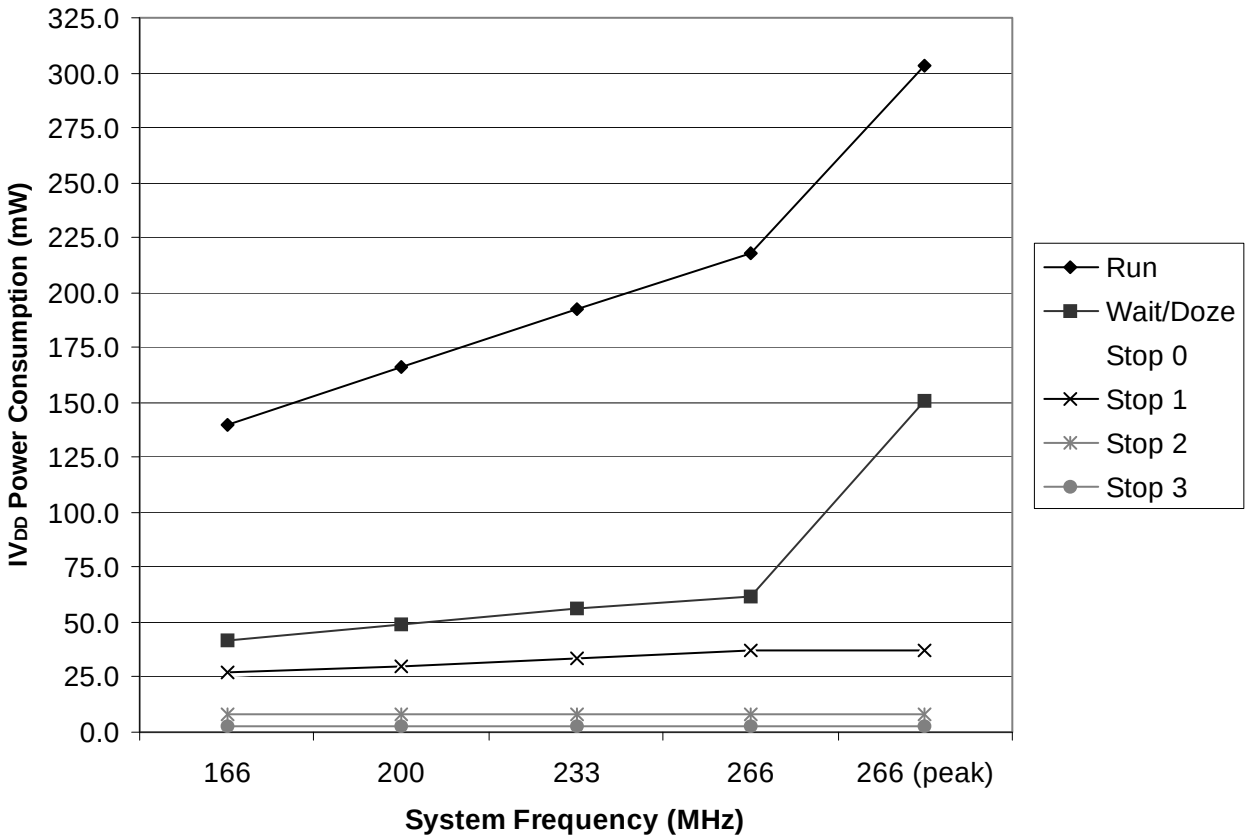

Figure 34. IV_{DD} Power Consumption in Low-Power Modes

7 Package Information

The latest package outline drawings are available on the product summary pages on http://www.freescale.com/coldfire. Table 33 lists the case outline numbers per device. Use these numbers in the web page's keyword search engine to find the latest package outline drawings.

Table 33. Package Information

Device	Package Type	Case Outline Numbers
MCF54450	256 MAPBGA	98ARH98219A
MCF54451		
MCF54452	360 TEPBGA	98ARE10605D
MCF54453		
MCF54454		
MCF54455		

8 Product Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com/coldfire.

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