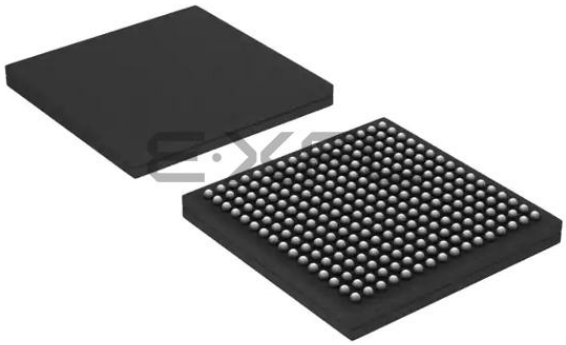

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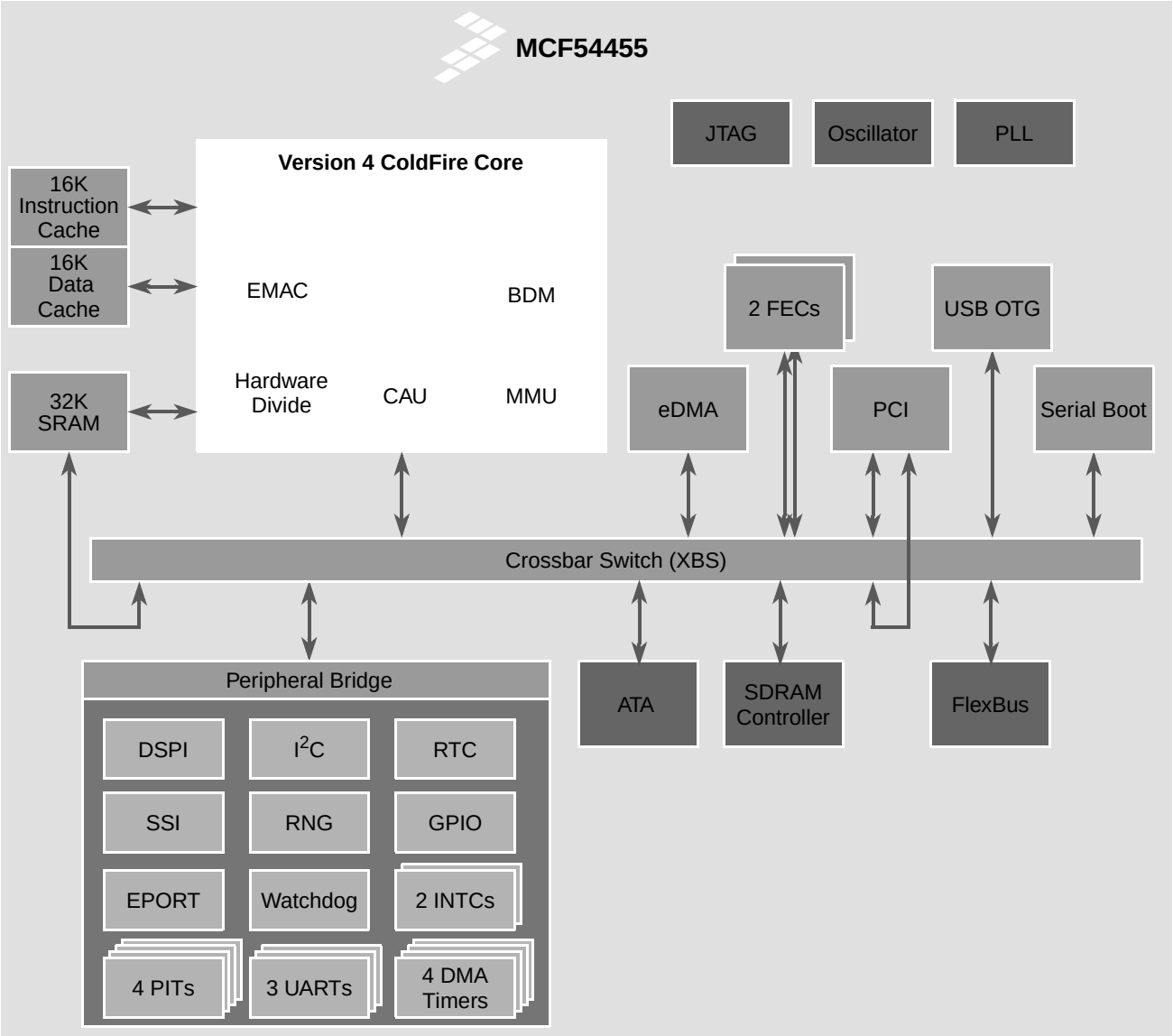
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V4
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	I²C, SPI, SSI, UART/USART, USB OTG
Peripherals	DMA, WDT
Number of I/O	132
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf54451vm240j



LEGEND

ATA	– Advanced Technology Attachment Controller	**INTC**	– Interrupt controller
BDM	– Background debug module	**JTAG**	– Joint Test Action Group interface
CAU	– Cryptography acceleration unit	**MMU**	– Memory management unit
DSPI	– DMA serial peripheral interface	**PCI**	– Peripheral Component Interconnect
eDMA	– Enhanced direct memory access	**PIT**	– Programmable interrupt timers
EMAC	– Enchance multiply-accumulate unit	**PLL**	– Phase locked loop module
EPORT	– Edge port module	**RNG**	– Random Number Generator
FEC	– Fast Ethernet controller	**RTC**	– Real time clock
GPIO	– General Purpose Input/Output	**SSI**	– Synchronous Serial Interface
I^{2}C	– Inter-Intergrated Circuit	**USB OTG**	– Universal Serial Bus On-the-Go controller

Figure 1. MCF54455 Block Diagram

Table 3. Special-Case Default Signal Functionality (continued)

Pin	256 MAPBGA	360 TEPBGA
$\overline{\text{PCI\_GNT}}$[3:0]	GPIO	$\overline{\text{PCI\_GNT}}$[3:0]
$\overline{\text{PCI\_REQ}}$[3:0]	GPIO	$\overline{\text{PCI\_REQ}}$[3:0]
$\overline{\text{IRQ1}}$	GPIO	$\overline{\text{PCI\_INTA}}$ and configured as an agent.
ATA_RESET	GPIO	ATA reset

Table 4. MCF5445*x* Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
Reset								
$\overline{\text{RESET}}$	—	—	—	U	I	EVDD	L4	Y18
$\overline{\text{RSTOUT}}$	—	—	—	—	O	EVDD	M15	B17
Clock								
EXTAL/PCI_CLK	—	—	—	—	I	EVDD	M16	A16
XTAL	—	—	—	U[3]	O	EVDD	L16	A17
Mode Selection								
BOOTMOD[1:0]	—	—	—	—	I	EVDD	M5, M7	AB17, AB21
FlexBus								
FB_AD[31:24]	PFBADH[7:0][4]	FB_D[31:24]	—	—	I/O	EVDD	A14, A13, D12, C12, B12, A12, D11, C11	J2, K4, J1, K1–3, L1, L4
FB_AD[23:16]	PFBADMH[7:0][4]	FB_D[23:16]	—	—	I/O	EVDD	B11, A11, D10, C10, B10, A10, D9, C9	L2, L3, M1–4, N1–2
FB_AD[15:8]	PFBADML[7:0][4]	FB_D[15:8]	—	—	I/O	EVDD	B9, A9, D8, C8, B8, A8, D7, C7	P1–2, R1–3, P4, T1–2
FB_AD[7:0]	PFBADL[7:0][4]	FB_D[7:0]	—	—	I/O	EVDD	B7, A7, D6, C6, B6, A6, D5, C5	T3–4, U1–3, V1–2, W1
$\overline{\text{FB\_BE/BWE}}$[3:2]	PBE[3:2]	FB_TSIZ[1:0]	—	—	O	EVDD	B5, A5	Y1, W2
$\overline{\text{FB\_BE/BWE}}$[1:0]	PBE[1:0]	—	—	—	O	EVDD	B4, A4	W3, Y2
FB_CLK	—	—	—	—	O	EVDD	B13	J3
$\overline{\text{FB\_CS}}$[3:1]	PCS[3:1]	—	—	—	O	EVDD	C2, D4, C3	W5, AA4, AB3
$\overline{\text{FB\_CS0}}$	—	—	—	—	O	EVDD	C4	Y4
$\overline{\text{FB\_OE}}$	PFBCTL3	—	—	—	O	EVDD	A2	AA1
FB_R/$\overline{\text{W}}$	PFBCTL2	—	—	—	O	EVDD	B2	AA3
$\overline{\text{FB\_TA}}$	PFBCTL1	—	—	U	I	EVDD	B1	AB2

Table 4. MCF5445*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
DSPI_SIN	PDSPI1	SBF_DI	—	[8]	I	EVDD	P15	B19
DSPI_SOUT	PDSPI0	SBF_DO	—	—	O	EVDD	N13	C20
UARTs								
$\overline{\text{U1CTS}}$	PUART7	—	—	—	I	EVDD	—	V3
$\overline{\text{U1RTS}}$	PUART6	—	—	—	O	EVDD	—	U4
U1RXD	PUART5	—	—	—	I	EVDD	—	P3
U1TXD	PUART4	—	—	—	O	EVDD	—	N3
$\overline{\text{U0CTS}}$	PUART3	—	—	—	I	EVDD	M3	Y16
$\overline{\text{U0RTS}}$	PUART2	—	—	—	O	EVDD	M2	AA16
U0RXD	PUART1	—	—	—	I	EVDD	N1	AB16
U0TXD	PUART0	—	—	—	O	EVDD	M1	W15
Note: The UART1 and UART 2 signals are multiplexed on the DMA timers and I2C pins.								
DMA Timers								
DT3IN	PTIMER3	DT3OUT	U2RXD	—	I	EVDD	C13	H2
DT2IN	PTIMER2	DT2OUT	U2TXD	—	I	EVDD	D13	H1
DT1IN	PTIMER1	DT1OUT	$\overline{\text{U2CTS}}$	—	I	EVDD	B14	H3
DT0IN	PTIMER0	DT0OUT	$\overline{\text{U2RTS}}$	—	I	EVDD	A15	G1
BDM/JTAG[9]								
PSTDDATA[7:0]	—	—	—	—	O	EVDD	E2, D1, F4, E3, D2, C1, E4, D3	AA6, AB6, AB5, W6, Y6, AA5, AB4, Y5
JTAG_EN	—	—	—	D	I	EVDD	M11	C21
PSTCLK	—	TCLK	—	—	I	EVDD	P13	C22
DSI	—	TDI	—	U	I	EVDD	T15	C19
DSO	—	TDO	—	—	O	EVDD	T14	A21
$\overline{\text{BKPT}}$	—	TMS	—	U	I	EVDD	R14	B21
DSCLK	—	$\overline{\text{TRST}}$	—	U	I	EVDD	M13	B22
Test								
TEST	—	—	—	D	I	EVDD	M6	AB20
PLLTEST	—	—	—	—	O	EVDD	K16	D15

4.3 Pinout—360 TEPBGA

The pinout for the MCF54452, MCF54453, MCF54454, and MCF54455 packages are shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A		PCI_REQ0	PCI_AD10	PCI_AD11	PCI_AD13	PCI_SERR	PCI_STOP	PCI_AD15	PCI_GNT0	PCI_AD29	PCI_AD20	XTAL 32K	EXTAL 32K	USB_DM	USB_DP	EXTAL	XTAL	DACK0	DSPI_PCS2	DSPI_SCK	TDO		A
B	PCI_CBE0	PCI_FRAME	PCI_AD9	PCI_PERR	PCI_AD12	PCI_RST	PCI_GNT3	PCI_AD14	PCI_AD18	PCI_AD28	PCI_AD19	PCI_AD21	NC		NC	VDD_OSC	RSTOUT	DREQ0	DSPI_SIN	DSPI_PCS1	TMS	TRST	B
C	PCI_AD0	PCI_AD2	PCI_IRDY	PCI_PAR	PCI_REQ1	IRQ1	PCI_REQ3	PCI_GNT2	PCI_GNT1	PCI_TRDY	PCI_AD31	PCI_AD22	VDD_RTC	VDD_A_PLL	NC	VSS_OSC	DACK1	DREQ1	TDI	DSPI_SOUT	JTAG_EN	TCLK	C
D	PCI_CBE1	PCI_AD1	PCI_AD7	PCI_AD8	PCI_IDSEL	IVDD	PCI_REQ2	IVDD	PCI_AD17	PCI_AD16	PCI_AD30	PCI_AD23	EVDD	IVDD	PLL TEST	NC	DSPI_PCS0	DSPI_PCS5	EVDD	SSI_MCLK	SSI_RXD	SSI_TXD	D
E	PCI_AD4	PCI_AD5	PCI_AD6	PCI_CBE2															SSI_BCLK	SSI_FS	SD_DM2	SD_DQS2	E
F	PCI_AD24	PCI_DEVSEL	PCI_AD3	IVDD																SD_D16	SD_D17	SD_D18	F
G	T0IN	PCI_AD26	PCI_AD25	PCI_CBE3				EVDD			EVDD			EVDD		EVDD			SD_D19	SD_D20	SD_D21	SD_D22	G
H	T2IN	T3IN	T1IN	IVDD																SD_D23	SD_DM3	SD_DQS3	H
J	FB_AD29	FB_AD31	FB_CLK	PCI_AD27				EVDD								EVDD			SD_D26	SD_D27	SD_D25	SD_D24	J
K	FB_AD28	FB_AD27	FB_AD26	FB_AD30																SD_D28	SD_D29	SD_D30	K
L	FB_AD25	FB_AD23	FB_AD22	FB_AD24				EVDD								EVDD			SD_CAS	SD_CS1	SD_D31	SD_CLK	L
M	FB_AD21	FB_AD20	FB_AD19	FB_AD18																SD_CS0	SD_VREF	SD_CLK	M
N	FB_AD17	FB_AD16	U1TXD	IVDD												EVDD			SD_A2	SD_WE	SD_RAS	SD_CKE	N
P	FB_AD15	FB_AD14	U1RXD	FB_AD10				EVDD											SD_BA0	SD_A1	SD_A0	SD_BA1	P
R	FB_AD13	FB_AD12	FB_AD11	IVDD												EVDD				SD_A5	SD_A4	SD_A3	R
T	FB_AD9	FB_AD8	FB_AD7	FB_AD6				EVDD			EVDD			EVDD		EVDD			SD_A9	SD_A8	SD_A7	SD_A6	T
U	FB_AD5	FB_AD4	FB_AD3	U1RTS																SD_A12	SD_A11	SD_A10	U
V	FB_AD2	FB_AD1	U1CTS	USB_VBUS_OC															ATA_DA2	ATA_DA1	ATA_DA0	SD_A13	V
W	FB_AD0	FB_BE/BWE2	FB_BE/BWE1	IVDD	FB_CS3	PST DDATA4	IVDD	IVDD	FEC0_RXD1	FEC0_TXD3	FEC0_TXEN	IVDD	ATA_RESET	FEC1_RXCLK	U0TXD	IVDD	FEC1_RXER	FEC1_TXD2	IVDD	FEC1_MDC	ATA_CS1	ATA_CS0	W
Y	FB_BE/BWE3	FB_BE/BWE0	FB_TS	FB_CS0	PST DDATA0	PST DDATA3	FEC0_MDIO	FEC0_RXDV	FEC0_RXD2	FEC0_TXCLK	FEC0_TXD0	I2C_SDA	ATA_BUFFER_EN	ATA_IORDY	FEC1_RXD2	U0CTS	FEC1_RXD0	RESET	FEC1_TXD3	FEC1_TXD0	NC	FEC1_MDIO	Y
AA	FB_OE	USB_VBUS_EN	FB_R/W	FB_CS2	PST DDATA2	PST DDATA7	FEC0_CRS	FEC0_RXCLK	NC	FEC0_RXER	FEC0_TXD1	I2C_SCL	IRQ4	ATA_DMARQ	FEC1_RXD3	U0RTS	FEC1_RXD1	FEC1_CRS	FEC1_TXD1	NC	FEC1_TXEN	FEC1_TXER	AA
AB		FB_TA	FB_CS1	PST DDATA1	PST DDATA5	PST DDATA6	FEC0_COL	FEC0_MDC	FEC0_RXD3	FEC0_RXD0	FEC0_TXD2	FEC0_TXER	IRQ7	IRQ3	FEC1_RXDV	U0RXD	BOOT MOD1	FEC1_COL	FEC1_TXCLK	TEST	BOOT MOD0		AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure 6. MCF54452, MCF54453, MCF54454, and MCF54455 Pinout (360 TEPBGA)

5 Electrical Characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF54455 microprocessor. This section contains detailed information on DC/AC electrical characteristics and AC timing specifications.

The electrical specifications are preliminary and from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. However, for production silicon, these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this MCU document supersede any values found in the module specifications.

5.1 Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Pin Name	Value	Units
External I/O pad supply voltage	EV_{DD}	EVDD	-0.3 to +4.0	V
Internal oscillator supply voltage	$OSCV_{DD}$	VDD_OSC	-0.3 to +4.0	V
Real-time clock supply voltage	$RTCV_{DD}$	VDD_RTC	-0.5 to +2.0	V
Internal logic supply voltage	IV_{DD}	IVDD	-0.5 to +2.0	V
SDRAM I/O pad supply voltage	SDV_{DD}	SD_VDD	-0.3 to +4.0	V
PLL supply voltage	PV_{DD}	VDD_A_PLL	-0.5 to +2.0	V
Digital input voltage[3]	V_{IN}	—	-0.3 to +3.6	V
Instantaneous maximum current Single pin limit (applies to all pins) [3, 4, 5]	I_{DD}	—	25	mA
Operating temperature range (packaged)	T_A (T_L - T_H)	—	-40 to +85	°C
Storage temperature range	T_{stg}	—	-55 to +150	°C

1 Functional operating conditions are given in Table 8. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., V_{SS} or EV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, and then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and EV_{DD}.

5 Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > EV_{DD}) is greater than I_{DD}, the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Ensure the external EV_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MPU is not consuming power (ex; no clock). The power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

5.2 Thermal Characteristics

Table 6. Thermal Characteristics

Characteristic		Symbol	256 MAPBGA	360 TEPBGA	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	29[1,2]	24[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	25[1,2]	21[1,2]	°C/W
Junction to board		θ_{JB}	18[3]	15[3]	°C/W
Junction to case		θ_{JC}	10[4]	11[4]	°C/W
Junction to top of package		Ψ_{jt}	2[1,5]	2[1,5]	°C/W
Maximum operating junction temperature		T_j	105	105	°C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C
Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = P_{INT} + $P_{I/O}$
P_{INT} = $I_{DD} \times IV_{DD}$, Watts - Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273°C)} \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

5.3 ESD Protection

Table 7. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 8. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Units
Internal logic supply voltage[1]	IV_{DD}	1.35	1.65	V
PLL analog operation voltage range [1]	PV_{DD}	1.35	1.65	V
External I/O pad supply voltage	EV_{DD}	3.0	3.6	V
Internal oscillator supply voltage	$OSCV_{DD}$	3.0	3.6	V
Real-time clock supply voltage	$RTCV_{DD}$	1.35	1.65	V
SDRAM I/O pad supply voltage — DDR mode	SDV_{DD}	2.25	2.75	V
SDRAM I/O pad supply voltage — DDR2 mode	SDV_{DD}	1.7	1.9	V
SDRAM I/O pad supply voltage — Mobile DDR mode	SDV_{DD}	1.7	1.9	V
SDRAM input reference voltage	SDV_{REF}	0.49 x SDV_{DD}	0.51 x SDV_{DD}	V
Input High Voltage	V_{IH}	0.7 x EV_{DD}	3.65	V
Input Low Voltage	V_{IL}	V_{SS} – 0.3	0.35 x EV_{DD}	V
Input Hysteresis	V_{HYS}	0.06 x EV_{DD}	—	mV
Input Leakage Current[2] V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–2.5	2.5	µA
Input Leakage Current[3] V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–5	5	µA
High Impedance (Off-State) Leakage Current[4] V_{in} = V_{DD} or V_{SS}, All input/output and output pins	I_{OZ}	–10.0	10.0	µA
Output High Voltage (All input/output and all output pins) I_{OH} = –5.0 mA	V_{OH}	0.85 × EV_{DD}	—	V
Output Low Voltage (All input/output and all output pins) I_{OL} = 5.0mA	V_{OL}	—	0.15 × EV_{DD}	V

Table 8. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Units
Weak Internal Pull Up Device Current, tested at V_{IL} Max.[5]	I_{APU}	–10	–130	µA
Input Capacitance [6] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF
Load Capacitance Low drive strength High drive strength	C_L		 25 50	pF
DC Injection Current [3, 7, 8, 9] $V_{NEGCLAMP}$ =V_{SS}– 0.3 V, $V_{POSCLAMP}$ = V_{DD} + 0.3 Single Pin Limit Total MCU Limit, Includes sum of all stressed pins	I_{IC}	 -1.0 -10	 1.0 10	mA

1 IV_{DD} and PV_{DD} should be at the same voltage. PV_{DD} should have a filtered input. Please see the PLL section of this specification for an example circuit. There are three PV_{DD} inputs, one for each PLL. A filter circuit should used on each PV_{DD} input.

2 Valid for all parts, EXCEPT the MCF54452YVR200.

3 Valid just the MCF54452YVR200 part number.

4 Worst-case tristate leakage current with only one I/O pin high. Since all I/Os share power when high, the leakage current is distributed among them. With all I/Os high, this spec reduces to ±2 µA min/max.

5 Refer to the *MCF54455 Reference Manual* signals description chapter for pins having weak internal pull-up devices.

6 This parameter is characterized before qualification rather than 100% tested.

7 All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD}.

8 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

9 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure the external V_{DD} load shunts current greater than the maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, at power-up, the system clock is not present during the power-up sequence until the PLL has attained lock.

5.5 Clock Timing Specifications

The clock module configures the device for one of several clocking methods. Clocking modes include internal phase-locked loop (PLL) clocking with an external clock reference or an external crystal reference supported by an internal crystal amplifier. The PLL can also be disabled, and an external oscillator can directly clock the device.

The specifications in Table 9 are for the CLKIN input pin (EXTAL input driven by an external clock reference). The duty cycle specification is based on an acceptable tolerance for the PLL, which yields 50% duty-cycle internal clocks to all on-chip peripherals. The MCF5445*x* devices use the input clock signal as its synchronous bus clock for PCI. A poor duty cycle on the input clock, may affect the overall timing margin to external devices. If negative edge logic is used to interface to PCI, providing a 50% duty-cycle input clock aids in simplifying overall system design.

Table 10. PLL Electrical Characteristics (continued)

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
11	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
12	Crystal capacitive load	C_L	See crystal spec		
13	Discrete load capacitance for XTAL Discrete load capacitance for EXTAL	C_{L_XTAL} C_{L_EXTAL}	—	$2 \times (C_L - C_{S\_XTAL} - C_{S\_EXTAL} - C_{S\_PCB})$[6]	pF
14	Frequency un-LOCK Range	f_{UL}	-4.0	4.0	% f_{sys}
15	Frequency LOCK Range	f_{LCK}	-2.0	2.0	% f_{sys}
17	CLKOUT Period Jitter, [3, 4, 7] Measured at f_{SYS} Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter	C_{jitter}	 — —	 10 TBD	 % FB_CLK % FB_CLK

1 The minimum system frequency is the minimum input clock divided by the maximum low-power divider (16 MHz ÷ 32,768). When the PLL is enabled, the minimum system frequency (f_{sys}) is 150 MHz.

2 This parameter is guaranteed by characterization before qualification rather than 100% tested. Applies to external clock reference only.

3 Proper PC board layout procedures must be followed to achieve specifications.

4 This parameter is guaranteed by design rather than 100% tested.

5 This specification is the PLL lock time only and does not include oscillator start-up time.

6 C_{S_PCB} is the measured PCB stray capacitance on EXTAL and XTAL.

7 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD}, EV_{DD}, and V_{SS} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

5.6 Reset Timing Specifications

Table 11 lists specifications for the reset timing parameters shown in Figure 8.

Table 11. Reset and Configuration Override Timing

Num	Characteristic	Min	Max	Unit
R1[1]	$\overline{\text{RESET}}$ valid to CLKIN (setup)	9	—	ns
R2	CLKIN to $\overline{\text{RESET}}$ invalid (hold)	1.5	—	ns
R3	$\overline{\text{RESET}}$ valid time[2]	5	—	CLKIN cycles
R4	CLKIN to $\overline{\text{RSTOUT}}$ valid	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Configuration Override inputs valid	0	—	ns
R6	Configuration Override inputs valid to $\overline{\text{RSTOUT}}$ invalid (setup)	20	—	CLKIN cycles
R7	Configuration Override inputs invalid after $\overline{\text{RSTOUT}}$ invalid (hold)	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override inputs High Impedance	—	1	CLKIN cycles

1 $\overline{\text{RESET}}$ and Configuration Override data lines are synchronized internally. Setup and hold times must be met only if recognition on a particular clock is required.

2 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

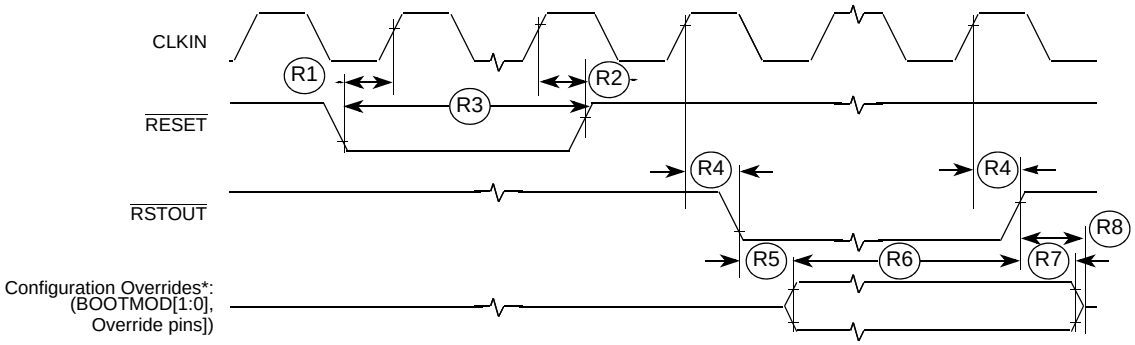


Figure 8. $\overline{\text{RESET}}$ and Configuration Override Timing

5.7 FlexBus Timing Specifications

A multi-function external bus interface called FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 66MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices, a simple chip-select based interface can be used.

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 12. FlexBus AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	25	66.66	MHz	
FB1	Clock Period	15	40	ns	
FB2	Output Valid	—	7.0	ns	[1]
FB3	Output Hold	1.0	—	ns	1
FB4	Input Setup	3.0	—	ns	[2]
FB5	Input Hold	0	—	ns	2

[1] Specification is valid for all FB_AD[31:0], $\overline{\text{FB\_BS}}$[3:0], $\overline{\text{FB\_CS}}$[3:0], $\overline{\text{FB\_OE}}$, FB_R/$\overline{\text{W}}$, $\overline{\text{FB\_TBST}}$, FB_TSIZ[1:0], and $\overline{\text{FB\_TS}}$.

[2] Specification is valid for all FB_AD[31:0] and $\overline{\text{FB\_TA}}$.

NOTE

The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial.

The address and data busses are muxed between the FlexBus and PCI controller. At the end of the read and write bus cycles the address signals are indeterminate.

5.8 SDRAM AC Timing Characteristics

The following timing numbers must be followed to properly latch or drive data onto the SDRAM memory bus. All timing numbers are relative to the four DQS byte lanes.

Table 13. SDRAM Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of Operation		60	133.33	MHz	1
DD1	Clock Period	t_{SDCK}	7.5	16.67	ns	
DD2	Pulse Width High	t_{SDCKH}	0.45	0.55	t_{SDCK}	2
DD3	Pulse Width Low	t_{SDCKL}	0.45	0.55	t_{SDCK}	3
DD4	Address, SD_CKE, $\overline{SD\_CAS}$, $\overline{SD\_RAS}$, $\overline{SD\_WE}$, $\overline{SD\_CS}$[1:0] — Output Valid	t_{CMV}	—	(0.5 x t_{SDCK}) + 1.0ns	ns	3
DD5	Address, SD_CKE, $\overline{SD\_CAS}$, $\overline{SD\_RAS}$, $\overline{SD\_WE}$, $\overline{SD\_CS}$[1:0] — Output Hold	t_{CMH}	2.0	—	ns	
DD6	Write Command to first DQS Latching Transition	t_{DQSS}	(1.0 x t_{SDCK}) - 0.6ns	(1.0 x t_{SDCK}) + 0.6ns	ns	
DD7	Data and Data Mask Output Setup (DQ-->DQS) Relative to DQS (DDR Write Mode)	t_{QS}	1.0	—	ns	4 5
DD8	Data and Data Mask Output Hold (DQS-->DQ) Relative to DQS (DDR Write Mode)	t_{QH}	1.0	—	ns	6
DD9	Input Data Skew Relative to DQS (Input Setup)	t_{IS}	—	1.0	ns	7
DD10	Input Data Hold Relative to DQS.	t_{IH}	(0.25 x t_{SDCK}) + 0.5ns	—	ns	8

1 The SDRAM interface operates at the same frequency as the internal system bus.

2 Pulse width high plus pulse width low cannot exceed min and max clock period.

3 Command output valid should be 1/2 the memory bus clock (t_{SDCK}) plus some minor adjustments for process, temperature, and voltage variations.

4 This specification relates to the required input setup time of DDR memories. The microprocessor's output setup should be larger than the input setup of the DDR memories. If it is not larger, then the input setup on the memory is in violation.
SD_D[31:24] is relative to SD_DQS[3]; SD_D[23:16] is relative to SD_DQS[2]

5 The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.

6 This specification relates to the required hold time of DDR memories.
SD_D[31:24] is relative to SD_DQS[3]; SD_D[23:16] is relative to SD_DQS[2]

7 Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

8 Data input hold is derived from each DQS clock edge. It begins with a DQS transition and ends when the first data line becomes invalid.

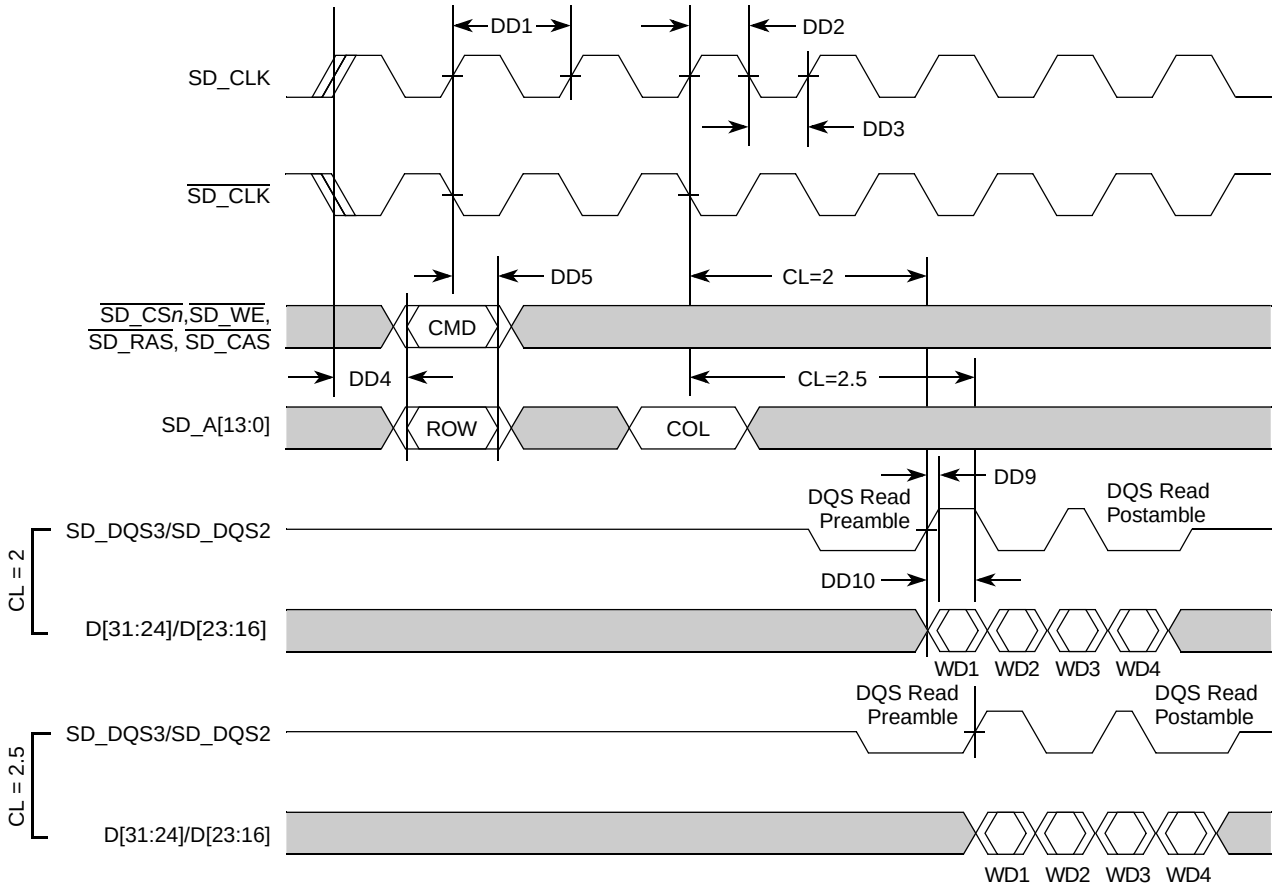


Figure 12. DDR Read Timing

5.9 PCI Bus Timing Specifications

The PCI bus on the device is PCI 2.2 compliant. The following timing numbers are mostly from the PCI 2.2 spec. Refer to the PCI 2.2 spec for a more detailed timing analysis.

Table 14. PCI Timing Specifications[1,2]

Num	Characteristic	33 MHz[3]		66 MHz[3]		
		Min	Max	Min	Max	Unit
	Frequency of Operation	—	33.33	33.33	66.66	MHz
P1	Clock Period	30	—	15	30	ns
P2	Bused PCI signals — input setup	7.0	—	3.0	—	ns
P3	$\overline{\text{PCI\_GNT}}$[3:0]/$\overline{\text{PCI\_REQ}}$[3:0] — input setup	10.0	—	5.0	—	ns
P4	All PCI signals — input hold	0	—	0	—	ns
P5	Bused PCI signals — output valid	—	11.0	—	6.0	ns

Table 14. PCI Timing Specifications[1,2] (continued)

Num	Characteristic	33 MHz[3]		66 MHz[3]		
		Min	Max	Min	Max	Unit
P6	$\overline{\text{PCI\_REQ}}$[3:0]/$\overline{\text{PCI\_GNT}}$[3:0] — output valid	—	12.0	—	6.0	ns
P7	All PCI signals — output hold	2.0	—	1.0	—	ns

1 The PCI bus operates at the CLKIN frequency. All timings are relative to the input clock, CLKIN.

2 All PCI signals are bused signals except for PCI_GNT[3:0] and PCI_REQ[3:0]. These signals are defined as point-to-point signals by the PCI Specification.

3 The 66-MHz parameters are only guaranteed when the 66-MHz PCI pad slew rates are selected. Likewise, the 33-MHz parameters are only guaranteed when the 33-MHz PCI pad slew rates are selected.

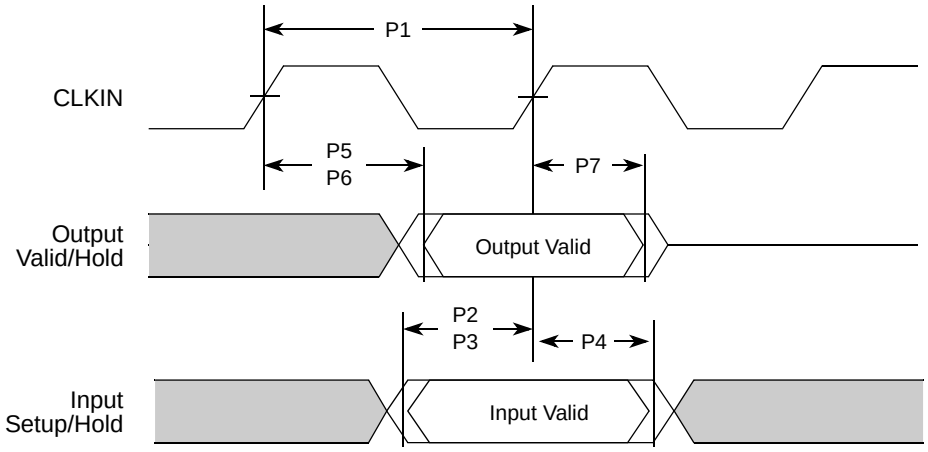


Figure 13. PCI Timing

5.9.1 Overshoot and Undershoot

Figure 14 shows the specification limits for overshoot and undershoot for PCI I/O. To guarantee long term reliability, the specification limits shown must be followed. Good transmission line design practices should be observed to guarantee the specification limits.

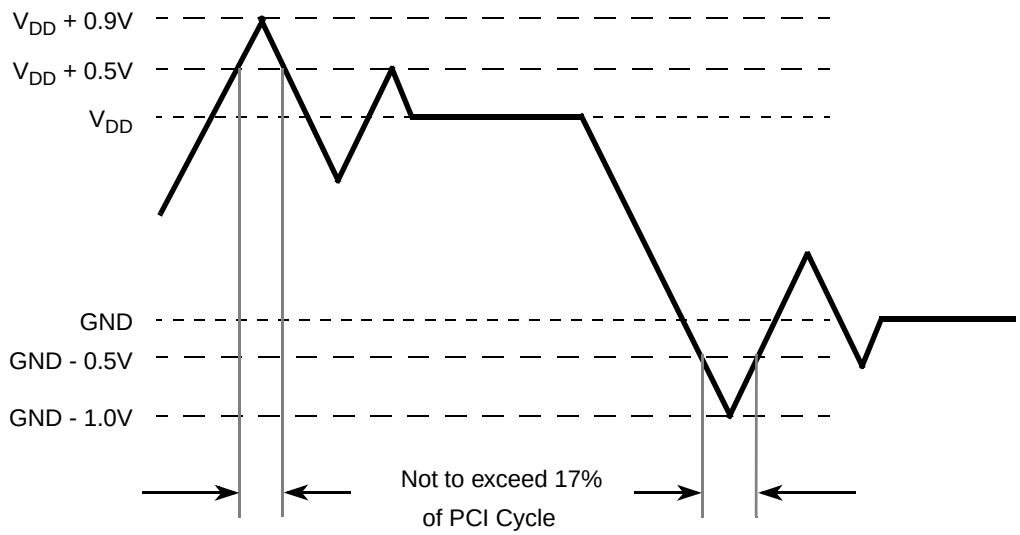


Figure 14. Overshoot and Undershoot Limits

5.10 ULPI Timing Specifications

The ULPI interface is fully compliant with the industry standard UTMI+ Low Pin Interface. Control and data timing requirements for the ULPI pins are given in Table 15. These timings apply to synchronous mode only. All timings are measured with respect to the clock as seen at the USB_CLKIN pin on the MCF5445*x*. The ULPI PHY is the source of the 60MHz clock.

NOTE

The USB controller requires a 60-MHz clock, even if using the on-chip FS/LS transceiver instead of the ULPI interface. In this case, the 60-MHz clock can be generated by the PLL or input on the USB_CLKIN pin.

Table 15. ULPI Interface Timing

Num	Characteristic	Min	Nominal	Max	Units
	USB_CLKIN operating frequency	—	60	—	MHz
	USB_CLKIN duty cycle	—	50	—	%
U1	USB_CLKIN clock period	—	16.67	—	ns
U2	Input Setup (control and data)	5.0	—	—	ns
U3	Input Hold (control and data)	1.0	—	—	ns
U4	Output Valid (control and data)	—	—	9.5	ns
U5	Output Hold (control and data)	1.0	—	—	

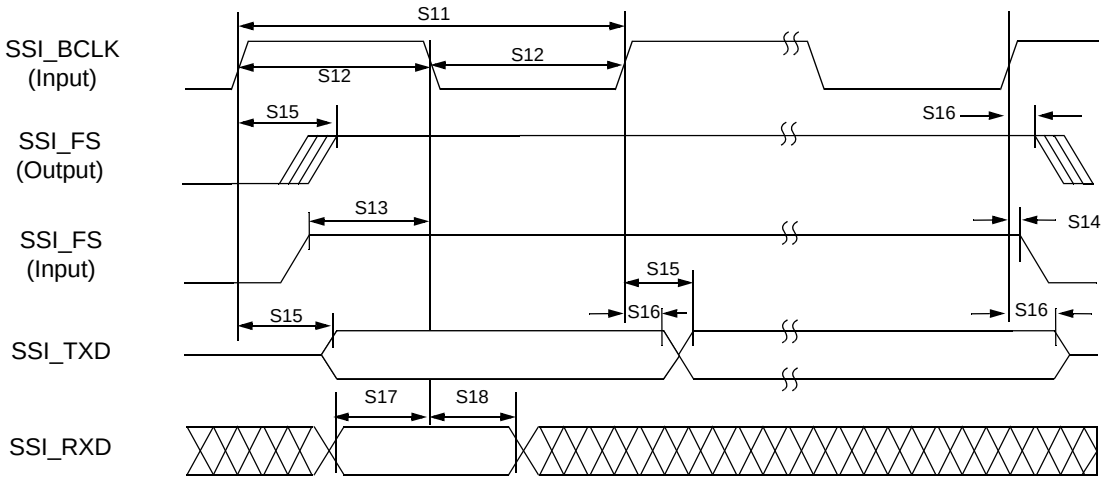


Figure 17. SSI Timing—Slave Modes

5.12 I²C Timing Specifications

Table 18 lists specifications for the I²C input timing parameters shown in Figure 18.

Table 18. I²C Input Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	t_{SYS}
I2	Clock low period	8	—	t_{SYS}
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4	—	t_{SYS}
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	t_{SYS}
I9	Stop condition setup time	2	—	t_{SYS}

Table 19 lists specifications for the I²C output timing parameters shown in Figure 18.

Table 19. I²C Output Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	6	—	t_{SYS}
I2[1]	Clock low period	10	—	t_{SYS}
I3[2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4[1]	Data hold time	7	—	t_{SYS}
I5[3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns

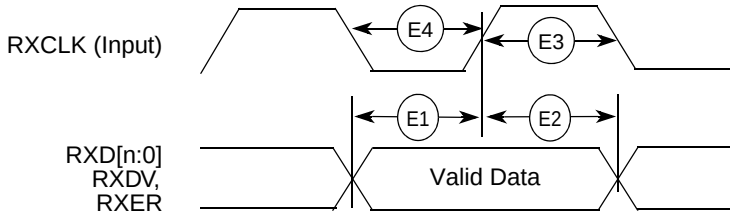


Figure 19. MII Receive Signal Timing Diagram

5.13.2 Transmit Signal Timing Specifications

Table 21. Transmit Signal Timing

Num	Characteristic	MII Mode		RMII Mode		Unit
		Min	Max	Min	Max	
—	TXCLK frequency	—	25	—	50	MHz
E5	TXCLK to TXD[n:0], TXEN, TXER invalid[1]	5	—	5	—	ns
E6	TXCLK to TXD[n:0], TXEN, TXER valid[1]	—	25	—	14	ns
E7	TXCLK pulse width high	35%	65%	35%	65%	t_{TXCLK}
E8	TXCLK pulse width low	35%	65%	35%	65%	t_{TXCLK}

1 In MII mode, n = 3; In RMII mode, n = 1

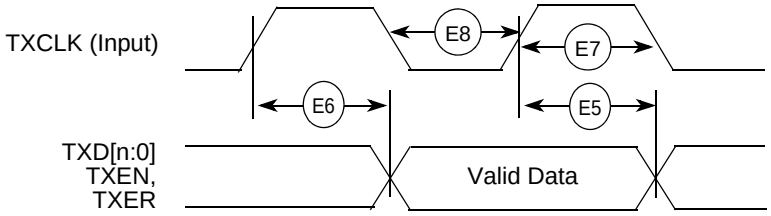


Figure 20. MII Transmit Signal Timing Diagram

5.13.3 Asynchronous Input Signal Timing Specifications

Table 22. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
E9	CRS, COL minimum pulse width	1.5	—	TXCLK period

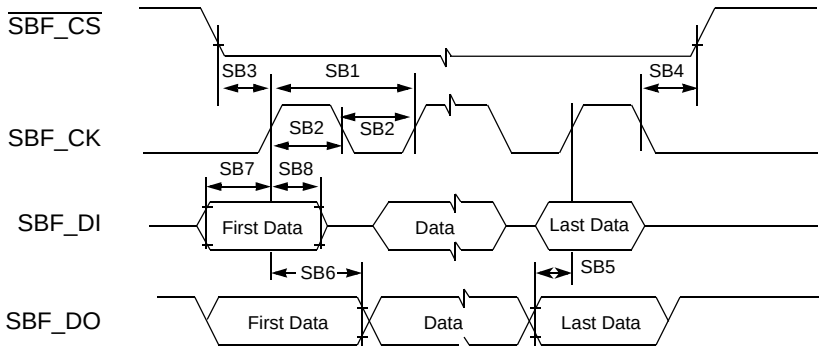


Figure 25. SBF Timing

5.18 General Purpose I/O Timing Specifications

Table 28. GPIO Timing[1]

Num	Characteristic	Min	Max	Unit
G1	FB_CLK High to GPIO Output Valid	—	9	ns
G2	FB_CLK High to GPIO Output Invalid	1.5	—	ns
G3	GPIO Input Valid to FB_CLK High	9	—	ns
G4	FB_CLK High to GPIO Input Invalid	1.5	—	ns

1 These general purpose specifications apply to the following signals: $\overline{\text{IRQ}}n$, all UART signals, all timer signals, $\overline{\text{DACK}}n$ and $\overline{\text{DREQ}}n$, and all signals configured as GPIO.

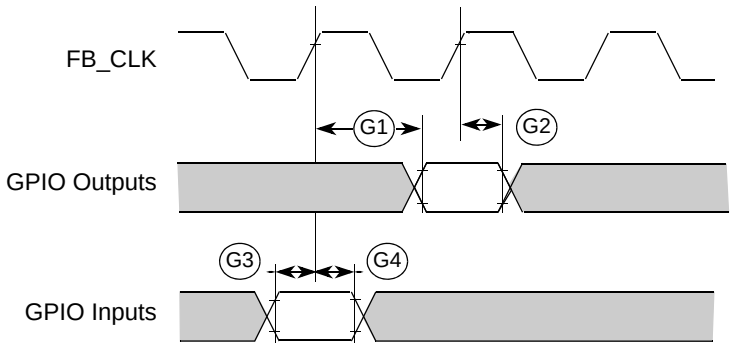


Figure 26. GPIO Timing

5.19 JTAG and Boundary Scan Timing

Table 29. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Min	Max	Unit
J1	TCLK Frequency of Operation	DC	20	MHz
J2	TCLK Cycle Period	50	—	ns
J3	TCLK Clock Pulse Width	20	30	ns
J4	TCLK Rise and Fall Times	—	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	5	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	20	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	—	33	ns
J8	TCLK Low to Boundary Scan Output High Z	—	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	10	—	ns
J11	TCLK Low to TDO Data Valid	—	11	ns
J12	TCLK Low to TDO High Z	—	11	ns
J13	$\overline{\text{TRST}}$ Assert Time	50	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

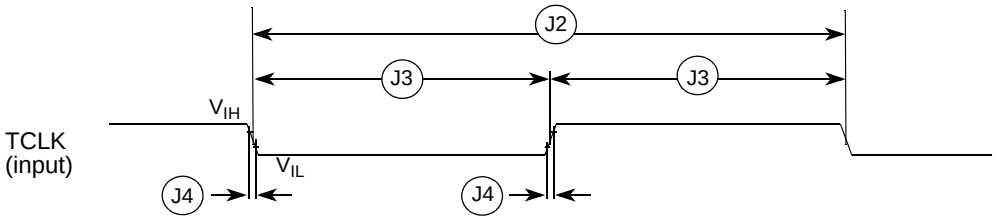


Figure 27. Test Clock Input Timing

All current consumption data is lab data measured on a single device using an evaluation board. Table 32 shows the typical power consumption in low-power modes. These current measurements are taken after executing a STOP instruction.

Table 32. Current Consumption in Low-Power Modes[1,2]

Mode	Voltage Supply	System Frequency				
		166 (Typ)[3]	200 (Typ)[3]	233 (Typ)[3]	266 (Typ)[3]	266 (Peak)[4]
RUN	IV_{DD} (mA)	93.4	110.9	128.2	145.4	202.1
	Power (mW)	140.1	166.3	192.4	218.1	303.2
WAIT/DOZE	IV_{DD} (mA)	28.0	32.7	37.5	41.1	100.2
	Power (mW)	42.0	49.1	56.2	61.7	150.3
STOP 0	IV_{DD} (mA)	17.1	19.8	22.5	25.2	25.2
	Power (mW)	25.7	29.7	33.7	37.8	37.8
STOP 1	IV_{DD} (mA)	17.9	19.8	22.4	25.1	25.1
	Power (mW)	26.8	29.6	33.6	37.6	37.6
STOP 2	IV_{DD} (mA)	5.7	5.7	5.7	5.7	5.7
	Power (mW)	8.6	8.6	8.6	8.6	8.6
STOP 3	IV_{DD} (mA)	1.8	1.8	1.8	1.8	1.8
	Power (mW)	2.6	2.6	2.6	2.6	2.6

1 All values are measured on an M54455EVB with 1.5V IV_{DD} power supply. Tests performed at room temperature.

2 Refer to the Power Management chapter in the *MCF54455 Reference Manual* for more information on low-power modes.

3 All peripheral clocks are off except UART0, INTC0, IACK, edge port, reset controller, CCM, PLL, and FlexBus prior to entering low-power mode.

4 All peripheral clocks on prior to entering low-power mode.

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