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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V4
Core Size	32-Bit Single-Core
Speed	266MHz
Connectivity	I²C, SPI, SSI, UART/USART, USB OTG
Peripherals	DMA, WDT
Number of I/O	132
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	360-BBGA
Supplier Device Package	360-TEPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf54452vr266

1 MCF5445*x* Family Comparison

The following table compares the various device derivatives available within the MCF5445*x* family.

Table 1. MCF5445*x* Family Configurations

Module	MCF54450	MCF54451	MCF54452	MCF54453	MCF54454	MCF54455
ColdFire Version 4 Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•	•	•	•	•
Core (System) Clock	up to 240 MHz		up to 266 MHz			
Peripheral Bus Clock (Core clock ÷ 2)	up to 120 MHz		up to 133 MHz			
External Bus Clock (Core clock ÷ 4)	up to 60 MHz		up to 66 MHz			
Performance (Dhrystone/2.1 MIPS)	up to 370		up to 410			
Independent Data/Instruction Cache	16 Kbytes each					
Static RAM (SRAM)	32 Kbytes					
PCI Controller	—	—	•	•	•	•
Cryptography Acceleration Unit (CAU)	—	•	—	•	—	•
ATA Controller	—	—	—	—	•	•
DDR SDRAM Controller	•	•	•	•	•	•
FlexBus External Interface	•	•	•	•	•	•
USB 2.0 On-the-Go	•	•	•	•	•	•
UTMI+ Low Pin Interface (ULPI)	•	•	•	•	•	•
Synchronous Serial Interface (SSI)	•	•	•	•	•	•
Fast Ethernet Controller (FEC)	1	1	2	2	2	2
UARTs	3	3	3	3	3	3
I^2C	•	•	•	•	•	•
DSPI	•	•	•	•	•	•
Real Time Clock	•	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4	4
Watchdog Timer (WDT)	•	•	•	•	•	•
Periodic Interrupt Timers (PIT)	4	4	4	4	4	4
Edge Port Module (EPORT)	•	•	•	•	•	•
Interrupt Controllers (INTC)	2	2	2	2	2	2
16-channel Direct Memory Access (DMA)	•	•	•	•	•	•
General Purpose I/O (GPIO)	•	•	•	•	•	•
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•	•	•
Package	256 MAPBGA		360 TEPBGA			

3.3.1 Power-Up Sequence

If EV_{DD}/SDV_{DD} are powered up with the IV_{DD} at 0 V, the sense circuits in the I/O pads cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must power up. The rise times on the power supplies should be slower than 50 V/millisecond to avoid turning on the internal ESD protection clamp diodes.

3.3.2 Power-Down Sequence

If IV_{DD}/PV_{DD} are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and PV_{DD} power down before EV_{DD} or SDV_{DD} must power down. There are no requirements for the fall times of the power supplies.

4 Pin Assignments and Reset States

4.1 Signal Multiplexing

The following table lists all the MCF5445*x* pins grouped by function. The Dir column is the direction for the primary function of the pin only. Refer to Section 4, “Pin Assignments and Reset States,” for package diagrams. For a more detailed discussion of the MCF5445*x* signals, consult the *MCF54455 Reference Manual* (MCF54455RM).

NOTE

In this table and throughout this document, a single signal within a group is designated without square brackets (i.e., FB_AD23), while designations for multiple signals within a group use brackets (i.e., FB_AD[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Most pins that are muxed with GPIO default to their GPIO functionality. See Table 3 for a list of the exceptions.

Table 3. Special-Case Default Signal Functionality

Pin	256 MAPBGA	360 TEPBGA
FB_AD[31:0]	FB_AD[31:0] except when serial boot selects 0-bit boot port size.	
$\overline{\text{FB\_BE/BWE}}$[3:0]	$\overline{\text{FB\_BE/BWE}}$[3:0]	
$\overline{\text{FB\_CS}}$[3:1]	$\overline{\text{FB\_CS}}$[3:1]	
$\overline{\text{FB\_OE}}$	$\overline{\text{FB\_OE}}$	
FB_R/$\overline{\text{W}}$	FB_R/$\overline{\text{W}}$	
$\overline{\text{FB\_TA}}$	$\overline{\text{FB\_TA}}$	
$\overline{\text{FB\_TS}}$	$\overline{\text{FB\_TS}}$	

Table 4. MCF5445*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
FB_TS	PFBCTL0	FB_ALE	FB_TBST	—	O	EVDD	A3	Y3
PCI Controller[5]								
PCI_AD[31:0]	—	FB_A[31:0]	—	—	I/O	EVDD	—	C11, D11, A10, B10, J4, G2, G3, F1, D12, C12, B12, A11, B11, B9, D9, D10, A8, B8, A5, B5, A4, A3, B3, D4, D3, E3–E1, F3, C2, D2, C1
—	—	FB_A[23:0]	—	—	I/O	EVDD	K14–13, J15–13, H13–15, G15–13, F14–13, E15–13, D16, B16, C15, B15, C14, D15, C16, D14	—
PCI_CBE[3:0]	—	—	—	—	I/O	EVDD	—	G4, E4, D1, B1
PCI_DEVSEL	—	—	—	—	O	EVDD	—	F2
PCI_FRAME	—	—	—	—	I/O	EVDD	—	B2
PCI_GNT3	PPCI7	ATA_DMACK	—	—	O	EVDD	—	B7
PCI_GNT[2:1]	PPCI[6:5]	—	—	—	O	EVDD	—	C8, C9
PCI_GNT0/ PCI_EXTREQ	PPCI4	—	—	—	O	EVDD	—	A9
PCI_IDSEL	—	—	—	—	I	EVDD	—	D5
PCI_IRDY	—	—	—	—	I/O	EVDD	—	C3
PCI_PAR	—	—	—	—	I/O	EVDD	—	C4
PCI_PERR	—	—	—	—	I/O	EVDD	—	B4
PCI_REQ3	PPCI3	ATA_INTRQ	—	—	I	EVDD	—	C7
PCI_REQ[2:1]	PPCI[2:1]	—	—	—	I	EVDD	—	D7, C5
PCI_REQ0/ PCI_EXTGNT	PPCI0	—	—	—	I	EVDD	—	A2
PCI_RST	—	—	—	—	O	EVDD	—	B6
PCI_SERR	—	—	—	—	I/O	EVDD	—	A6
PCI_STOP	—	—	—	—	I/O	EVDD	—	A7
PCI_TRDY	—	—	—	—	I/O	EVDD	—	C10
SDRAM Controller								
SD_A[13:0]	—	—	—	—	O	SDVDD	R1, P1, N2, P2, R2, T2, M4, N3, P3, R3, T3, T4, R4, N4	V22, U20–22, T19–22, R20–22, N19, P20–21

Table 4. MCF5445*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
ATA								
ATA_BUFFER_EN	PATAH5	—	—	—	O	EVDD	—	Y13
$\overline{\text{ATA\_CS}}$[1:0]	PATAH[4:3]	—	—	—	O	EVDD	—	W21, W22
ATA_DA[2:0]	PATAH[2:0]	—	—	—	O	EVDD	—	V19–21
$\overline{\text{ATA\_RESET}}$	PATAL2	—	—	—	O	EVDD	—	W13
ATA_DMARQ	PATAL1	—	—	—	I	EVDD	—	AA14
ATA_IORDY	PATAL0	—	—	—	I	EVDD	—	Y14
Real Time Clock								
EXTAL32K	—	—	—	—	I	EVDD	J16	A13
XTAL32K	—	—	—	—	O	EVDD	H16	A12
SSI								
SSI_MCLK	PSSI4	—	—	—	O	EVDD	T13	D20
SSI_BCLK	PSSI3	$\overline{\text{U1CTS}}$	—	—	I/O	EVDD	R13	E19
SSI_FS	PSSI2	$\overline{\text{U1RTS}}$	—	—	I/O	EVDD	P12	E20
SSI_RXD	PSSI1	U1RXD	—	UD	I	EVDD	T12	D21
SSI_TXD	PSSI0	U1TXD	—	UD	O	EVDD	R12	D22
I^2C								
I2C_SCL	PFECI2C1	—	U2TXD	U	I/O	EVDD	K3	AA12
I2C_SDA	PFECI2C0	—	U2RXD	U	I/O	EVDD	K4	Y12
DMA								
$\overline{\text{DACK1}}$	PDMA3	—	ULPI_DIR	—	O	EVDD	M14	C17
$\overline{\text{DREQ1}}$	PDMA2	—	USB_CLKIN	U	I	EVDD	P16	C18
$\overline{\text{DACK0}}$	PDMA1	DSPI_PCS3	—	—	O	EVDD	N15	A18
$\overline{\text{DREQ0}}$	PDMA0	—	—	U	I	EVDD	N16	B18
DSPI								
DSPI_PCS5/$\overline{\text{PCSS}}$	PDSPI6	—	—	—	O	EVDD	N14	D18
DSPI_PCS2	PDSPI5	—	—	—	O	EVDD	L13	A19
DSPI_PCS1	PDSPI4	$\overline{\text{SBF\_CS}}$	—	—	O	EVDD	P14	B20
DSPI_PCS0/$\overline{\text{SS}}$	PDSPI3	—	—	U	I/O	EVDD	R16	D17
DSPI_SCK	PDSPI2	SBF_CK	—	—	I/O	EVDD	R15	A20

Table 4. MCF5445*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
Power Supplies								
IVDD	—	—	—	—	—	—	E6–12, F5, F12	D6, D8, D14, F4, H4, N4, R4, W4, W7, W8, W12, W16, W19
EVDD	—	—	—	—	—	—	G5, G12, H5, H12, J5, J12, K5, K12, L5–6, L12	D13, D19, G8, G11, G14, G16, J7, J16, L7, L16, N16, P7, R16, T8, T12, T14, T16
SD_VDD	—	—	—	—	—	—	L7–11, M9, M10	F19, H19, K19, M19, R19, U19
VDD_OSC	—	—	—	—	—	—	L14	B16
VDD_A_PLL	—	—	—	—	—	—	K15	C14
VDD_RTC	—	—	—	—	—	—	M12	C13
VSS	—	—	—	—	—	—	A1, A16, F6–11, G6–11, H6–11, J6–11, K6–11, T1, T16	A1, A22, B14, G7, G9–10, G12–13, G15, H7, H16, J9–14, K7, K9–14, K16, L9–14, M7, M9–M14, M16, N7, N9–14, P9–14, P16, R7, T7, T9–11, T13, T15, AB1, AB22
VSS_OSC	—	—	—	—	—	—	L15	C16

1 Pull-ups are generally only enabled on pins with their primary function, except as noted.

2 Refers to pin's primary function.

3 Enabled only in oscillator bypass mode (internal crystal oscillator is disabled).

4 Serial boot must select 0-bit boot port size to enable the GPIO mode on these pins.

5 When the PCI is enabled, all PCI bus pins come up configured as such. This includes the PCI_GNT and PCI_REQ lines, which have GPIO. The IRQ1/$\overline{\text{PCI\_INTA}}$ signal is a special case. It comes up as $\overline{\text{PCI\_INTA}}$ when booting as a PCI agent and as GPIO when booting as a PCI host.
For the 360 TEPBGA, booting with PCI disabled results in all dedicated PCI pins being safe-stated. The $\overline{\text{PCI\_GNT}}$ and $\overline{\text{PCI\_REQ}}$ lines and IRQ1/$\overline{\text{PCI\_INTA}}$ come up as GPIO.

6 GPIO functionality is determined by the edge port module. The pin multiplexing and control module is only responsible for assigning the alternate functions.

7 Depends on programmed polarity of the USB_VBUS_OC signal.

8 Pull-up when the serial boot facility (SBF) controls the pin

9 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The pin multiplexing and control module is not responsible for assigning these pins.

4.3 Pinout—360 TEPBGA

The pinout for the MCF54452, MCF54453, MCF54454, and MCF54455 packages are shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A		PCI_REQ0	PCI_AD10	PCI_AD11	PCI_AD13	PCI_SERR	PCI_STOP	PCI_AD15	PCI_GNT0	PCI_AD29	PCI_AD20	XTAL 32K	EXTAL 32K	USB_DM	USB_DP	EXTAL	XTAL	DACK0	DSPI_PCS2	DSPI_SCK	TDO		A
B	PCI_CBE0	PCI_FRAME	PCI_AD9	PCI_PERR	PCI_AD12	PCI_RST	PCI_GNT3	PCI_AD14	PCI_AD18	PCI_AD28	PCI_AD19	PCI_AD21	NC		NC	VDD_OSC	RSTOUT	DREQ0	DSPI_SIN	DSPI_PCS1	TMS	TRST	B
C	PCI_AD0	PCI_AD2	PCI_IRDY	PCI_PAR	PCI_REQ1	IRQ1	PCI_REQ3	PCI_GNT2	PCI_GNT1	PCI_TRDY	PCI_AD31	PCI_AD22	VDD_RTC	VDD_A_PLL	NC	VSS_OSC	DACK1	DREQ1	TDI	DSPI_SOUT	JTAG_EN	TCLK	C
D	PCI_CBE1	PCI_AD1	PCI_AD7	PCI_AD8	PCI_IDSEL	IVDD	PCI_REQ2	IVDD	PCI_AD17	PCI_AD16	PCI_AD30	PCI_AD23	EVDD	IVDD	PLL TEST	NC	DSPI_PCS0	DSPI_PCS5	EVDD	SSI_MCLK	SSI_RXD	SSI_TXD	D
E	PCI_AD4	PCI_AD5	PCI_AD6	PCI_CBE2															SSI_BCLK	SSI_FS	SD_DM2	SD_DQS2	E
F	PCI_AD24	PCI_DEVSEL	PCI_AD3	IVDD																SD_D16	SD_D17	SD_D18	F
G	T0IN	PCI_AD26	PCI_AD25	PCI_CBE3				EVDD			EVDD			EVDD		EVDD			SD_D19	SD_D20	SD_D21	SD_D22	G
H	T2IN	T3IN	T1IN	IVDD																SD_D23	SD_DM3	SD_DQS3	H
J	FB_AD29	FB_AD31	FB_CLK	PCI_AD27				EVDD								EVDD			SD_D26	SD_D27	SD_D25	SD_D24	J
K	FB_AD28	FB_AD27	FB_AD26	FB_AD30																SD_D28	SD_D29	SD_D30	K
L	FB_AD25	FB_AD23	FB_AD22	FB_AD24				EVDD								EVDD			SD_CAS	SD_CS1	SD_D31	SD_CLK	L
M	FB_AD21	FB_AD20	FB_AD19	FB_AD18																SD_CS0	SD_VREF	SD_CLK	M
N	FB_AD17	FB_AD16	U1TXD	IVDD												EVDD			SD_A2	SD_WE	SD_RAS	SD_CKE	N
P	FB_AD15	FB_AD14	U1RXD	FB_AD10				EVDD											SD_BA0	SD_A1	SD_A0	SD_BA1	P
R	FB_AD13	FB_AD12	FB_AD11	IVDD												EVDD				SD_A5	SD_A4	SD_A3	R
T	FB_AD9	FB_AD8	FB_AD7	FB_AD6				EVDD			EVDD			EVDD		EVDD			SD_A9	SD_A8	SD_A7	SD_A6	T
U	FB_AD5	FB_AD4	FB_AD3	U1RTS																SD_A12	SD_A11	SD_A10	U
V	FB_AD2	FB_AD1	U1CTS	USB_VBUS_OC															ATA_DA2	ATA_DA1	ATA_DA0	SD_A13	V
W	FB_AD0	FB_BE/BWE2	FB_BE/BWE1	IVDD	FB_CS3	PST DDATA4	IVDD	IVDD	FEC0_RXD1	FEC0_TXD3	FEC0_TXEN	IVDD	ATA_RESET	FEC1_RXCLK	U0TXD	IVDD	FEC1_RXER	FEC1_TXD2	IVDD	FEC1_MDC	ATA_CS1	ATA_CS0	W
Y	FB_BE/BWE3	FB_BE/BWE0	FB_TS	FB_CS0	PST DDATA0	PST DDATA3	FEC0_MDIO	FEC0_RXDV	FEC0_RXD2	FEC0_TXCLK	FEC0_TXD0	I2C_SDA	ATA_BUFFER_EN	ATA_IORDY	FEC1_RXD2	U0CTS	FEC1_RXD0	RESET	FEC1_TXD3	FEC1_TXD0	NC	FEC1_MDIO	Y
AA	FB_OE	USB_VBUS_EN	FB_R/W	FB_CS2	PST DDATA2	PST DDATA7	FEC0_CRS	FEC0_RXCLK	NC	FEC0_RXER	FEC0_TXD1	I2C_SCL	IRQ4	ATA_DMARQ	FEC1_RXD3	U0RTS	FEC1_RXD1	FEC1_CRS	FEC1_TXD1	NC	FEC1_TXEN	FEC1_TXER	AA
AB		FB_TA	FB_CS1	PST DDATA1	PST DDATA5	PST DDATA6	FEC0_COL	FEC0_MDC	FEC0_RXD3	FEC0_RXD0	FEC0_TXD2	FEC0_TXER	IRQ7	IRQ3	FEC1_RXDV	U0RXD	BOOT MOD1	FEC1_COL	FEC1_TXCLK	TEST	BOOT MOD0		AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure 6. MCF54452, MCF54453, MCF54454, and MCF54455 Pinout (360 TEPBGA)

5.2 Thermal Characteristics

Table 6. Thermal Characteristics

Characteristic		Symbol	256 MAPBGA	360 TEPBGA	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	29[1,2]	24[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	25[1,2]	21[1,2]	°C/W
Junction to board		θ_{JB}	18[3]	15[3]	°C/W
Junction to case		θ_{JC}	10[4]	11[4]	°C/W
Junction to top of package		Ψ_{jt}	2[1,5]	2[1,5]	°C/W
Maximum operating junction temperature		T_j	105	105	°C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C
Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = P_{INT} + $P_{I/O}$
P_{INT} = $I_{DD} \times IV_{DD}$, Watts - Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273°C)} \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

Table 9. Input Clock Timing Requirements

Item	Specification	Min	Max	Unit
C1	Cycle time	15	40	ns
1 / C1	Frequency	25	66.66	MHz
C2	Rise time (20% of vdd to 80% of vdd)	-	2	ns
C3	Fall time (80% of vdd to 20% of vdd)	-	2	ns
C4	Duty cycle (at 50% of vdd)	40	60	%

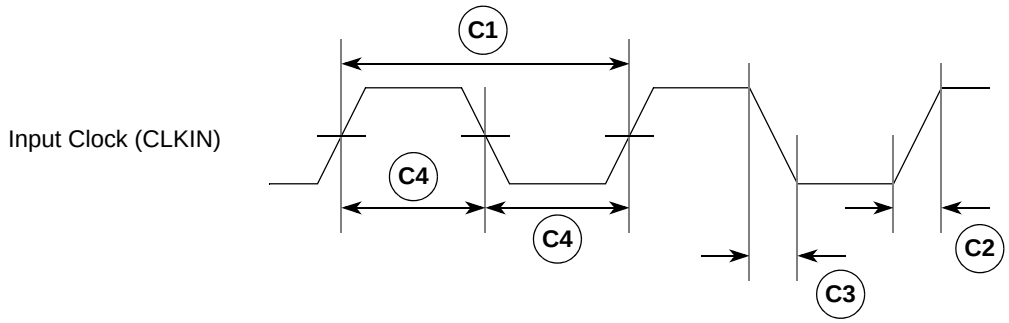

Figure 7. Input Clock Timing Diagram

Table 10. PLL Electrical Characteristics

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	PLL Reference Frequency Range Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 16 16	 40 66.66	 MHz MHz
2	Core/System Frequency	f_{sys}	512 Hz[1]	266.67 MHz	—
	Core/System Clock Period	t_{sys}	—	$1/f_{sys}$	ns
19	VCO Frequency ($f_{vco} = f_{ref} \times PFDR$)	f_{vco}	300	540	MHz
3	Crystal Start-up Time[2, 3]	t_{cst}	—	10	ms
4	EXTAL Input High Voltage Crystal Mode[4] All other modes (External, Limp)	 V_{IHEXT} V_{IHEXT}	 V_{XTAL} + 0.4 $E_{VDD}/2$ + 0.4	 — —	 V V
5	EXTAL Input Low Voltage Crystal Mode[4] All other modes (External, Limp)	 V_{ILEXT} V_{ILEXT}	 — —	 V_{XTAL} - 0.4 $E_{VDD}/2$ - 0.4	 V V
6	EXTAL Input Rise & Fall Time (20% to 80% E_{VDD}) (External, Limp)		1	2	ns
7	PLL Lock Time [3, 5]	t_{lpll}	—	50000	CLKIN
8	Duty Cycle of reference [3] (External, Limp)	t_{dc}	40	60	%
9	XTAL Current	I_{XTAL}	1	3	mA
10	Total on-chip stray capacitance on XTAL	C_{S_XTAL}	—	1.5	pF

Table 10. PLL Electrical Characteristics (continued)

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
11	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
12	Crystal capacitive load	C_L	See crystal spec		
13	Discrete load capacitance for XTAL Discrete load capacitance for EXTAL	C_{L_XTAL} C_{L_EXTAL}	—	$2 \times (C_L - C_{S\_XTAL} - C_{S\_EXTAL} - C_{S\_PCB})$[6]	pF
14	Frequency un-LOCK Range	f_{UL}	-4.0	4.0	% f_{sys}
15	Frequency LOCK Range	f_{LCK}	-2.0	2.0	% f_{sys}
17	CLKOUT Period Jitter, [3, 4, 7] Measured at f_{SYS} Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter	C_{jitter}	 — —	 10 TBD	 % FB_CLK % FB_CLK

1 The minimum system frequency is the minimum input clock divided by the maximum low-power divider (16 MHz ÷ 32,768). When the PLL is enabled, the minimum system frequency (f_{sys}) is 150 MHz.

2 This parameter is guaranteed by characterization before qualification rather than 100% tested. Applies to external clock reference only.

3 Proper PC board layout procedures must be followed to achieve specifications.

4 This parameter is guaranteed by design rather than 100% tested.

5 This specification is the PLL lock time only and does not include oscillator start-up time.

6 C_{S_PCB} is the measured PCB stray capacitance on EXTAL and XTAL.

7 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD}, EV_{DD}, and V_{SS} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

5.6 Reset Timing Specifications

Table 11 lists specifications for the reset timing parameters shown in Figure 8.

Table 11. Reset and Configuration Override Timing

Num	Characteristic	Min	Max	Unit
R1[1]	$\overline{\text{RESET}}$ valid to CLKIN (setup)	9	—	ns
R2	CLKIN to $\overline{\text{RESET}}$ invalid (hold)	1.5	—	ns
R3	$\overline{\text{RESET}}$ valid time[2]	5	—	CLKIN cycles
R4	CLKIN to $\overline{\text{RSTOUT}}$ valid	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Configuration Override inputs valid	0	—	ns
R6	Configuration Override inputs valid to $\overline{\text{RSTOUT}}$ invalid (setup)	20	—	CLKIN cycles
R7	Configuration Override inputs invalid after $\overline{\text{RSTOUT}}$ invalid (hold)	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override inputs High Impedance	—	1	CLKIN cycles

1 $\overline{\text{RESET}}$ and Configuration Override data lines are synchronized internally. Setup and hold times must be met only if recognition on a particular clock is required.

2 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

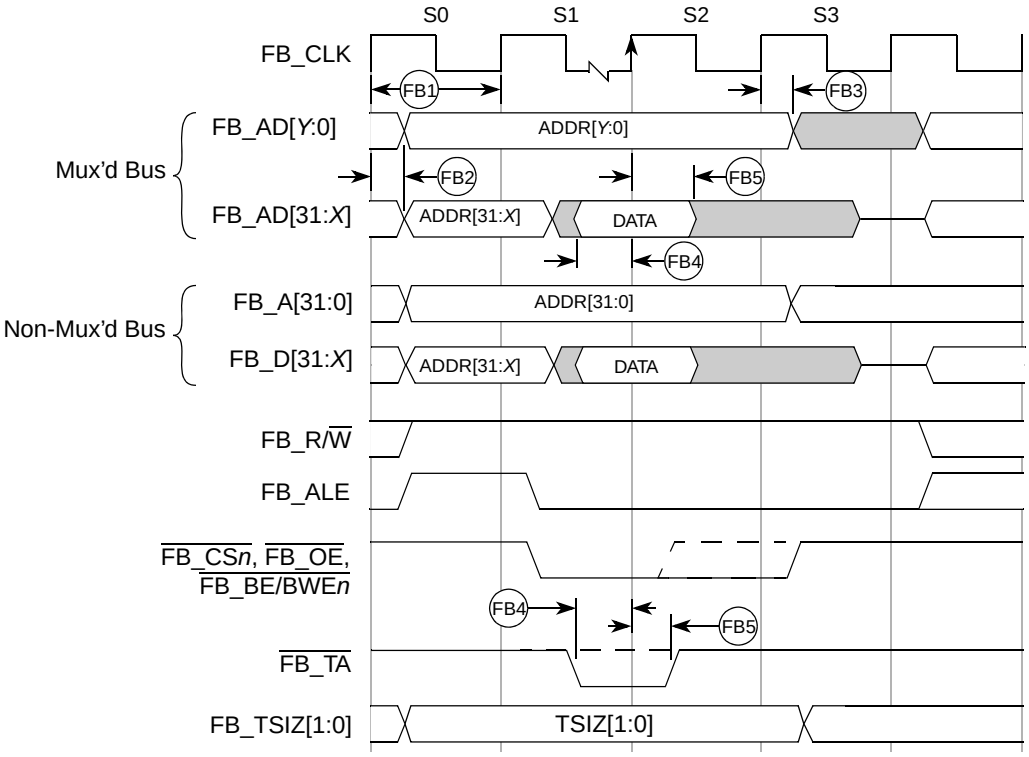

Figure 9. FlexBus Read Timing

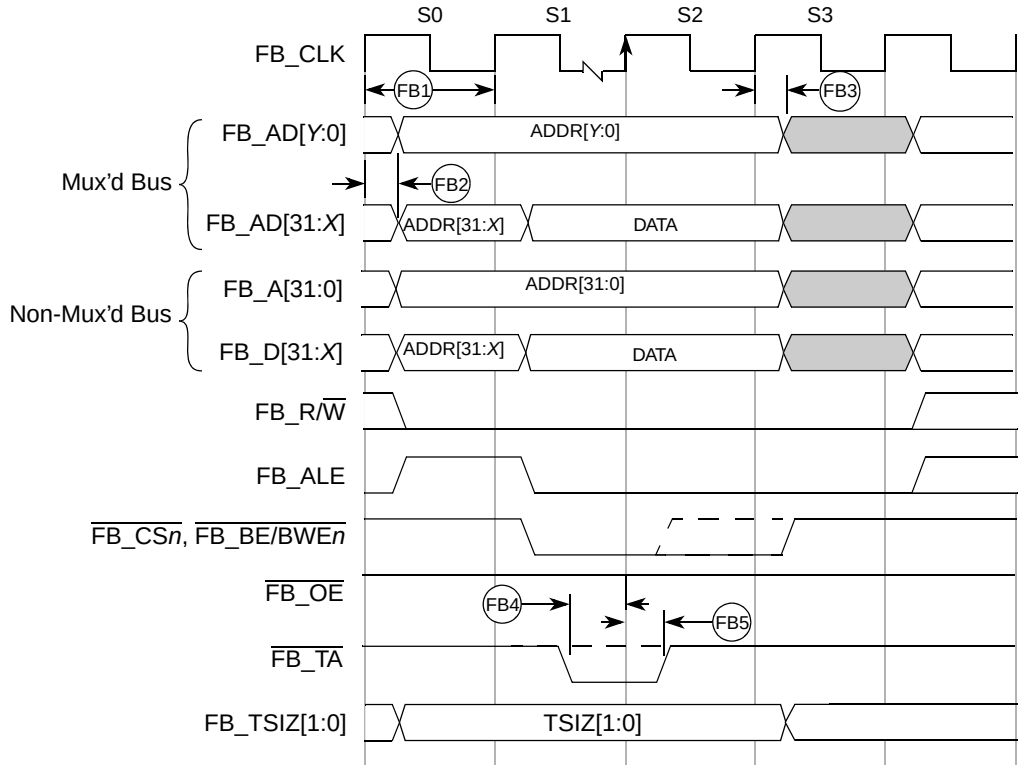

Figure 10. Flexbus Write Timing

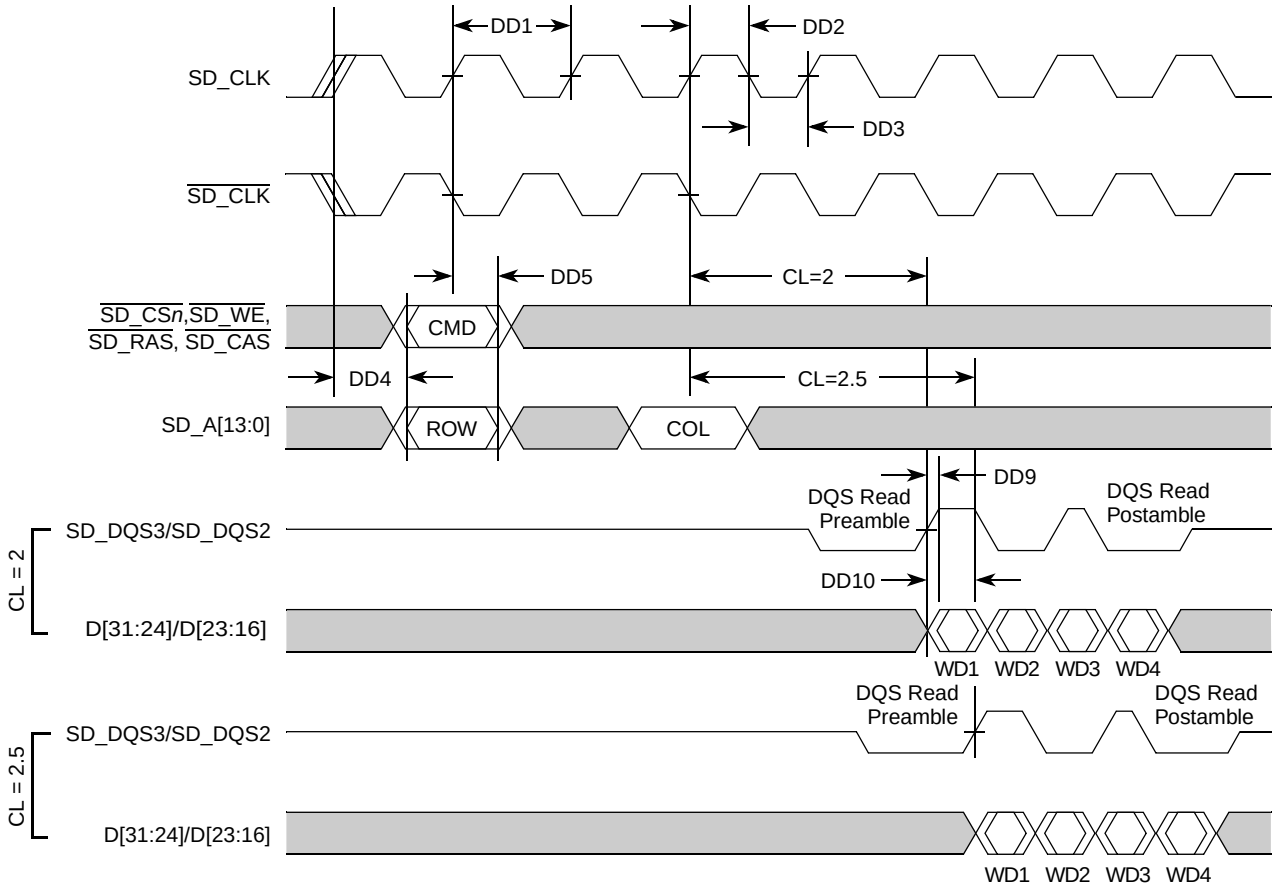

Figure 12. DDR Read Timing

5.9 PCI Bus Timing Specifications

The PCI bus on the device is PCI 2.2 compliant. The following timing numbers are mostly from the PCI 2.2 spec. Refer to the PCI 2.2 spec for a more detailed timing analysis.

Table 14. PCI Timing Specifications[1,2]

Num	Characteristic	33 MHz[3]		66 MHz[3]		
		Min	Max	Min	Max	Unit
	Frequency of Operation	—	33.33	33.33	66.66	MHz
P1	Clock Period	30	—	15	30	ns
P2	Bused PCI signals — input setup	7.0	—	3.0	—	ns
P3	$\overline{\text{PCI\_GNT}}$[3:0]/$\overline{\text{PCI\_REQ}}$[3:0] — input setup	10.0	—	5.0	—	ns
P4	All PCI signals — input hold	0	—	0	—	ns
P5	Bused PCI signals — output valid	—	11.0	—	6.0	ns

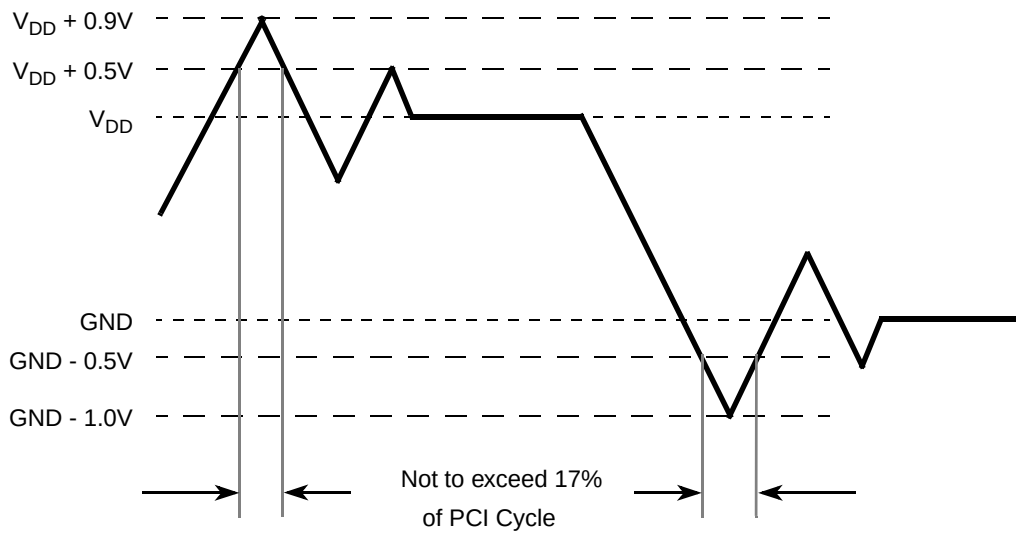

Figure 14. Overshoot and Undershoot Limits

5.10 ULPI Timing Specifications

The ULPI interface is fully compliant with the industry standard UTMI+ Low Pin Interface. Control and data timing requirements for the ULPI pins are given in Table 15. These timings apply to synchronous mode only. All timings are measured with respect to the clock as seen at the USB_CLKIN pin on the MCF5445*x*. The ULPI PHY is the source of the 60MHz clock.

NOTE

The USB controller requires a 60-MHz clock, even if using the on-chip FS/LS transceiver instead of the ULPI interface. In this case, the 60-MHz clock can be generated by the PLL or input on the USB_CLKIN pin.

Table 15. ULPI Interface Timing

Num	Characteristic	Min	Nominal	Max	Units
	USB_CLKIN operating frequency	—	60	—	MHz
	USB_CLKIN duty cycle	—	50	—	%
U1	USB_CLKIN clock period	—	16.67	—	ns
U2	Input Setup (control and data)	5.0	—	—	ns
U3	Input Hold (control and data)	1.0	—	—	ns
U4	Output Valid (control and data)	—	—	9.5	ns
U5	Output Hold (control and data)	1.0	—	—	

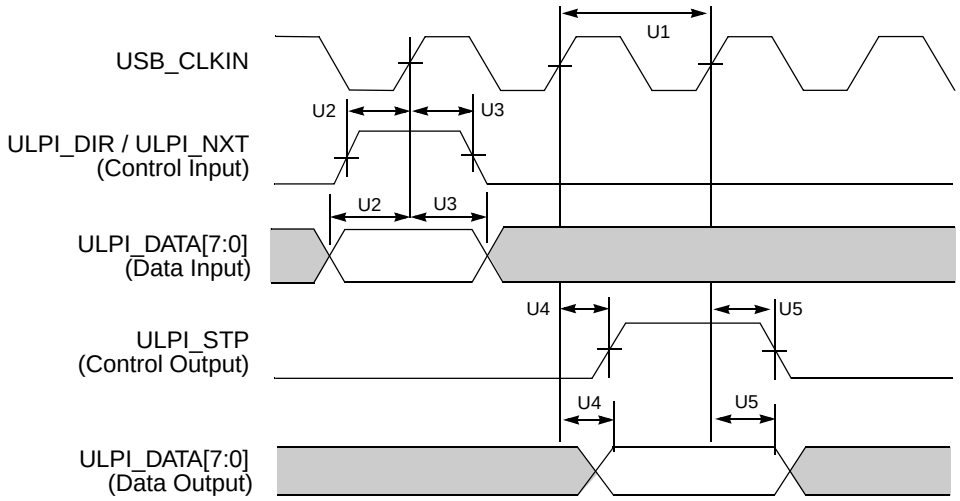

Figure 15. ULPI Timing Diagram

5.11 SSI Timing Specifications

This section provides the AC timings for the SSI in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (SSI_TCR[TSCKP] = 0, SSI_RCR[RSCKP] = 0) and a non-inverted frame sync (SSI_TCR[TFSI] = 0, SSI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SSI_BCLK) and/or the frame sync (SSI_FS) shown in the figures below.

Table 16. SSI Timing — Master Modes[1]

Num	Description	Symbol	Min	Max	Units	Notes
S1	SSI_MCLK cycle time	t_{MCLK}	$2 \times t_{SYS}$	—	ns	2
S2	SSI_MCLK pulse width high / low		45%	55%	t_{MCLK}	
S3	SSI_BCLK cycle time	t_{BCLK}	$8 \times t_{SYS}$	—	ns	3
S4	SSI_BCLK pulse width		45%	55%	t_{BCLK}	
S5	SSI_BCLK to SSI_FS output valid		—	15	ns	
S6	SSI_BCLK to SSI_FS output invalid		0	—	ns	
S7	SSI_BCLK to SSI_TXD valid		—	15	ns	
S8	SSI_BCLK to SSI_TXD invalid / high impedence		-2	—	ns	
S9	SSI_RXD / SSI_FS input setup before SSI_BCLK		10	—	ns	
S10	SSI_RXD / SSI_FS input hold after SSI_BCLK		0	—	ns	

1 All timings specified with a capactive load of 25pF.

2 SSI_MCLK can be generated from SSI_CLKIN or a divided version of the internal system clock (f_{sys}).

3 SSI_BCLK can be derived from SSI_CLKIN or a divided version of the internal system clock (f_{sys}).

Table 17. SSI Timing—Slave Modes[1]

Num	Description	Symbol	Min	Max	Units	Notes
S11	SSI_BCLK cycle time	t_{BCLK}	$8 \times t_{SYS}$	—	ns	
S12	SSI_BCLK pulse width high / low		45%	55%	t_{BCLK}	
S13	SSI_FS input setup before SSI_BCLK		10	—	ns	
S14	SSI_FS input hold after SSI_BCLK		2	—	ns	
S15	SSI_BCLK to SSI_TXD / SSI_FS output valid		—	15	ns	
S16	SSI_BCLK to SSI_TXD / SSI_FS output invalid / high impedence		0	—	ns	
S17	SSI_RXD setup before SSI_BCLK		10	—	ns	
S18	SSI_RXD hold after SSI_BCLK		2	—	ns	

1 All timings specified with a capactive load of 25pF.

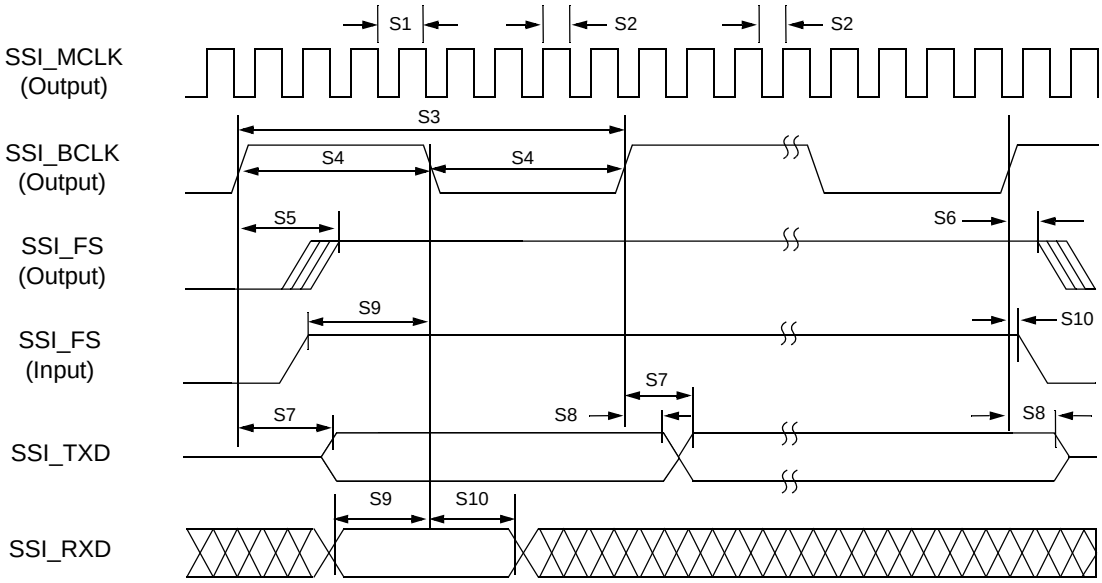

Figure 16. SSI Timing—Master Modes

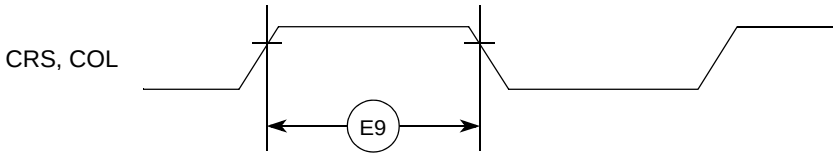

Figure 21. MII Async Inputs Timing Diagram

5.13.4 MII Serial Management Timing Specifications

Table 23. MII Serial Management Channel Signal Timing

Num	Characteristic	Symbol	Min	Max	Unit
E10	MDC cycle time	t_{MDC}	400	—	ns
E11	MDC pulse width		40	60	% t_{MDC}
E12	MDC to MDIO output valid		—	375	ns
E13	MDC to MDIO output invalid		25	—	ns
E14	MDIO input to MDC setup		10	—	ns
E15	MDIO input to MDC hold		0	—	ns

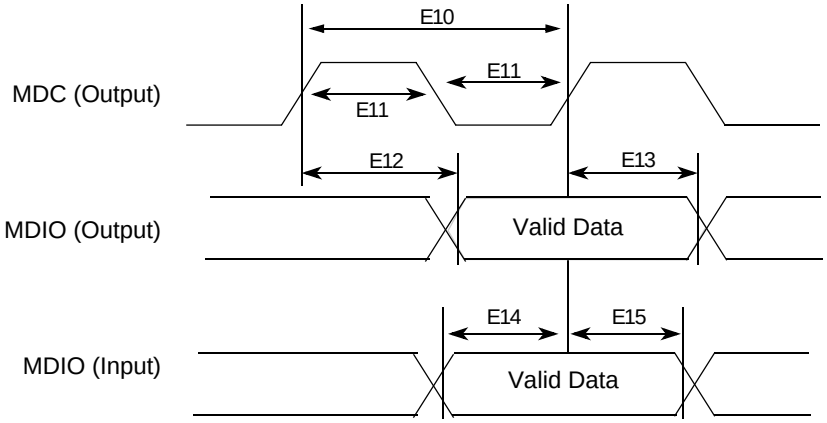

Figure 22. MII Serial Management Channel TIming Diagram

5.14 32-Bit Timer Module Timing Specifications

Table 24 lists timer module AC timings.

Table 24. Timer Module AC Timing Specifications

Name	Characteristic	Min	Max	Unit
T1	DT*n*IN cycle time (*n* = 0:3)	3	—	$t_{sys/2}$
T2	DT*n*IN pulse width (*n* = 0:3)	1	—	$t_{sys/2}$

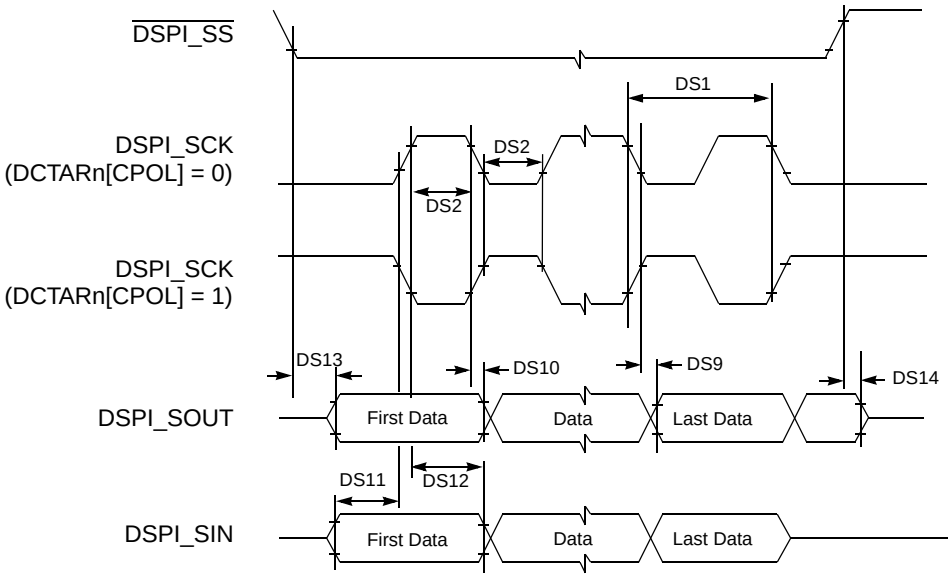

Figure 24. DSPI Classic SPI Timing—Slave Mode

5.17 SBF Timing Specifications

The Serial Boot Facility (SBF) provides a means to read configuration information and system boot code from a broad array of SPI-compatible EEPROMs, flashes, FRAMs, nVSRAMs, etc. Table 27 provides the AC timing specifications for the SBF.

Table 27. SBF AC Timing Specifications

Name	Characteristic	Symbol	Min	Max	Unit	Notes
SB1	SBF_CK Cycle Time	t_{SBFCK}	40	—	ns	[1]
SB2	SBF_CK High/Low Time	—	30%	—	t_{SBFCK}	
SB3	$\overline{\text{SBF\_CS}}$ to SBF_CK delay	—	t_{SBFCK} - 2.0	—	ns	
SB4	SBF_CK to $\overline{\text{SBF\_CS}}$ delay	—	t_{SBFCK} - 2.0	—	ns	
SB5	SBF_CK to SBF_DO valid	—	-5	—	ns	
SB6	SBF_CK to SBF_DO invalid	—	5	—	ns	
SB7	SBF_DI to SBF_SCK input setup	—	10	—	ns	
SB8	SBF_CK to SBF_DI input hold	—	0	—	ns	

[1] At reset, the SBF_CK cycle time is $t_{REF} \times 67$. The first byte of data read from the serial memory contains a divider value that is used to set the SBF_CK cycle time for the duration of the serial boot process.

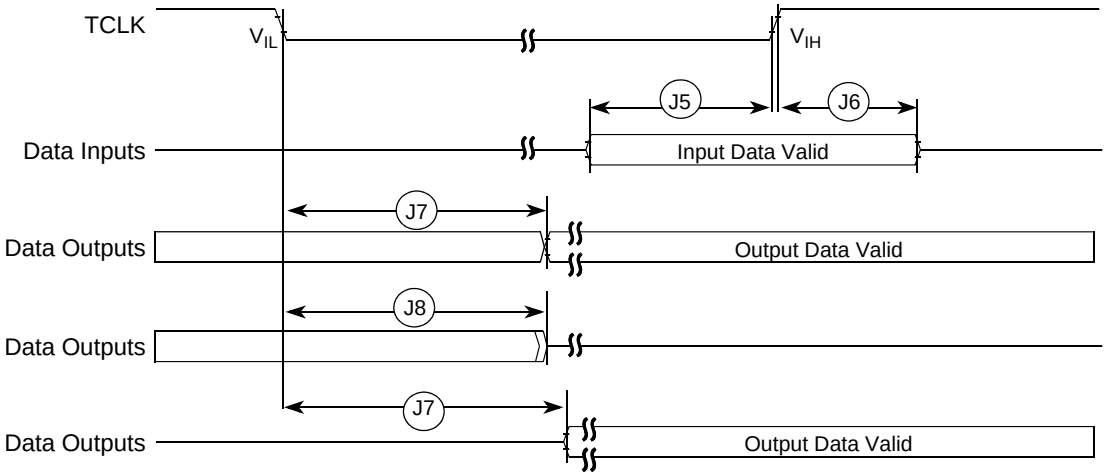

Figure 28. Boundary Scan (JTAG) Timing

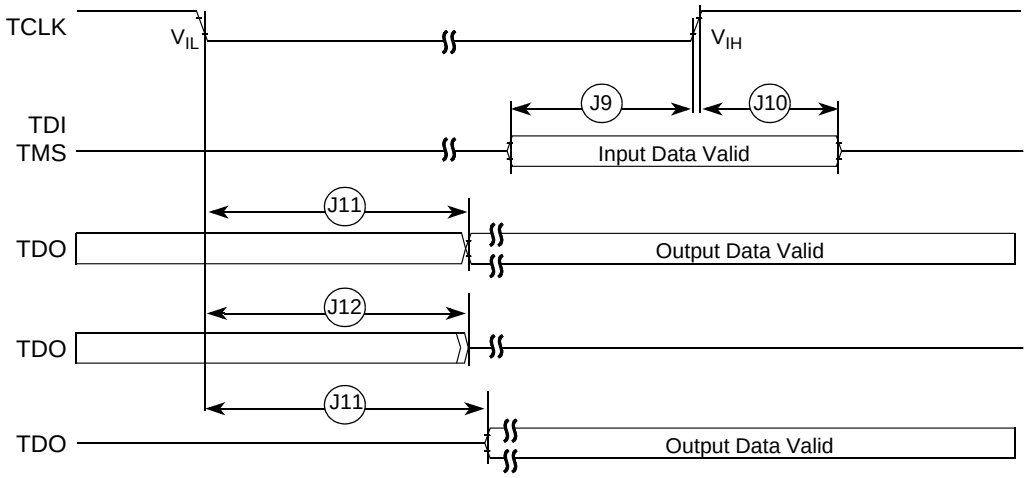

Figure 29. Test Access Port Timing

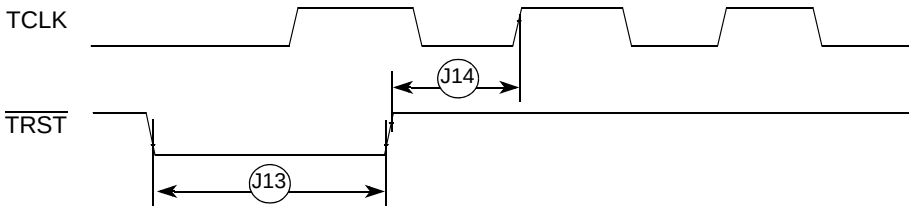

Figure 30. $\overline{\text{TRST}}$ Timing

5.20 Debug AC Timing Specifications

Table 30 lists specifications for the debug AC timing parameters shown in Figure 31 and Table 32.

Table 30. Debug AC Timing Specification

Num	Characteristic	Min	Max	Units
D0	PSTCLK cycle time	1	1	t_{SYS}
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	1.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4[1]	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

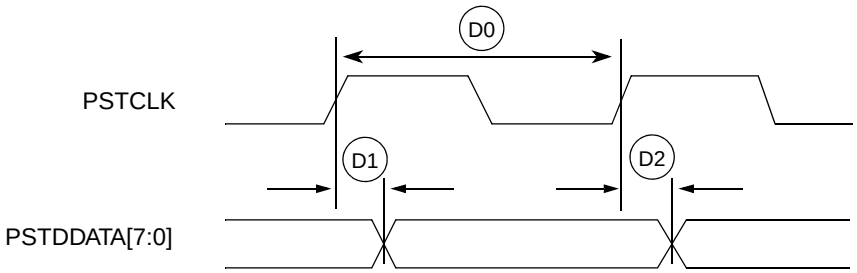

Figure 31. Real-Time Trace AC Timing

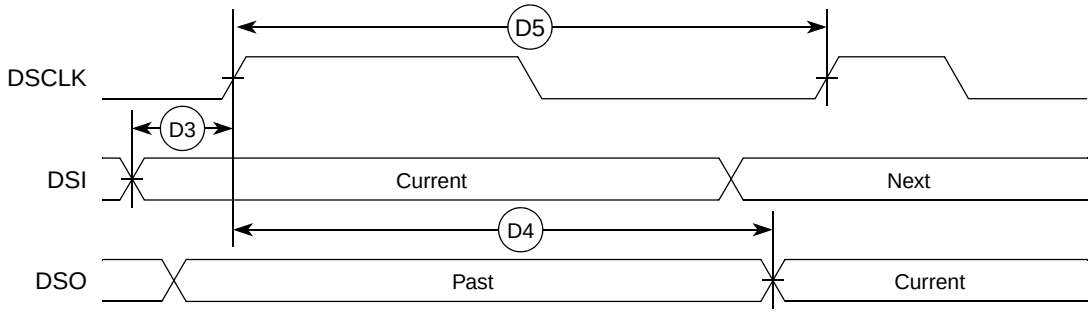

Figure 32. BDM Serial Port AC Timing

All current consumption data is lab data measured on a single device using an evaluation board. Table 32 shows the typical power consumption in low-power modes. These current measurements are taken after executing a STOP instruction.

Table 32. Current Consumption in Low-Power Modes[1,2]

Mode	Voltage Supply	System Frequency				
		166 (Typ)[3]	200 (Typ)[3]	233 (Typ)[3]	266 (Typ)[3]	266 (Peak)[4]
RUN	IV_{DD} (mA)	93.4	110.9	128.2	145.4	202.1
	Power (mW)	140.1	166.3	192.4	218.1	303.2
WAIT/DOZE	IV_{DD} (mA)	28.0	32.7	37.5	41.1	100.2
	Power (mW)	42.0	49.1	56.2	61.7	150.3
STOP 0	IV_{DD} (mA)	17.1	19.8	22.5	25.2	25.2
	Power (mW)	25.7	29.7	33.7	37.8	37.8
STOP 1	IV_{DD} (mA)	17.9	19.8	22.4	25.1	25.1
	Power (mW)	26.8	29.6	33.6	37.6	37.6
STOP 2	IV_{DD} (mA)	5.7	5.7	5.7	5.7	5.7
	Power (mW)	8.6	8.6	8.6	8.6	8.6
STOP 3	IV_{DD} (mA)	1.8	1.8	1.8	1.8	1.8
	Power (mW)	2.6	2.6	2.6	2.6	2.6

1 All values are measured on an M54455EVB with 1.5V IV_{DD} power supply. Tests performed at room temperature.

2 Refer to the Power Management chapter in the *MCF54455 Reference Manual* for more information on low-power modes.

3 All peripheral clocks are off except UART0, INTC0, IACK, edge port, reset controller, CCM, PLL, and FlexBus prior to entering low-power mode.

4 All peripheral clocks on prior to entering low-power mode.

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