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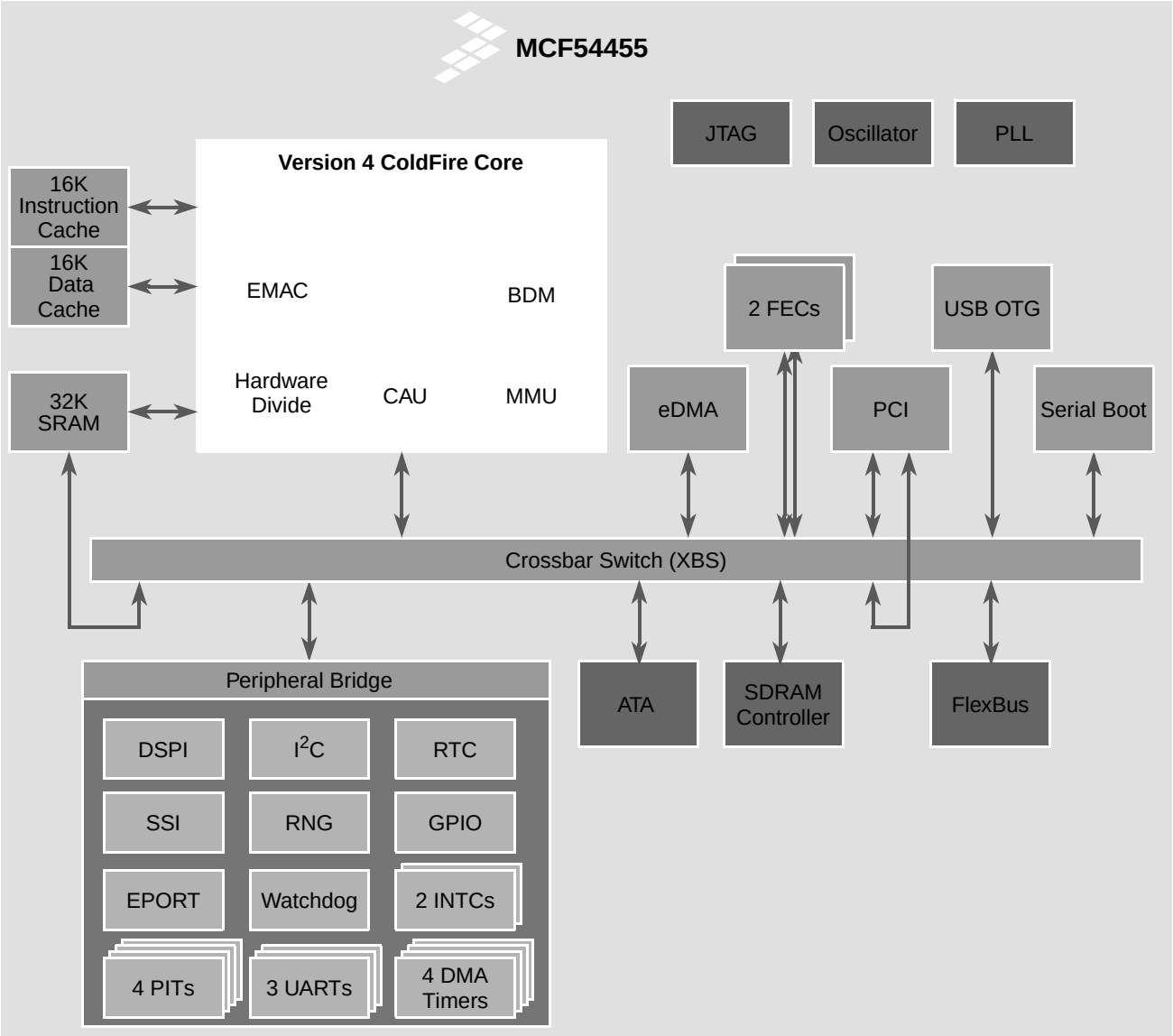
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V4
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	I²C, SPI, SSI, UART/USART, USB OTG
Peripherals	DMA, WDT
Number of I/O	132
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	360-BBGA
Supplier Device Package	360-TEPBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf54454cvr200



LEGEND

ATA	– Advanced Technology Attachment Controller	**INTC**	– Interrupt controller
BDM	– Background debug module	**JTAG**	– Joint Test Action Group interface
CAU	– Cryptography acceleration unit	**MMU**	– Memory management unit
DSPI	– DMA serial peripheral interface	**PCI**	– Peripheral Component Interconnect
eDMA	– Enhanced direct memory access	**PIT**	– Programmable interrupt timers
EMAC	– Enchance multiply-accumulate unit	**PLL**	– Phase locked loop module
EPORT	– Edge port module	**RNG**	– Random Number Generator
FEC	– Fast Ethernet controller	**RTC**	– Real time clock
GPIO	– General Purpose Input/Output	**SSI**	– Synchronous Serial Interface
I^{2}C	– Inter-Intergrated Circuit	**USB OTG**	– Universal Serial Bus On-the-Go controller

Figure 1. MCF54455 Block Diagram

1 MCF5445*x* Family Comparison

The following table compares the various device derivatives available within the MCF5445*x* family.

Table 1. MCF5445*x* Family Configurations

Module	MCF54450	MCF54451	MCF54452	MCF54453	MCF54454	MCF54455
ColdFire Version 4 Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•	•	•	•	•
Core (System) Clock	up to 240 MHz		up to 266 MHz			
Peripheral Bus Clock (Core clock ÷ 2)	up to 120 MHz		up to 133 MHz			
External Bus Clock (Core clock ÷ 4)	up to 60 MHz		up to 66 MHz			
Performance (Dhrystone/2.1 MIPS)	up to 370		up to 410			
Independent Data/Instruction Cache	16 Kbytes each					
Static RAM (SRAM)	32 Kbytes					
PCI Controller	—	—	•	•	•	•
Cryptography Acceleration Unit (CAU)	—	•	—	•	—	•
ATA Controller	—	—	—	—	•	•
DDR SDRAM Controller	•	•	•	•	•	•
FlexBus External Interface	•	•	•	•	•	•
USB 2.0 On-the-Go	•	•	•	•	•	•
UTMI+ Low Pin Interface (ULPI)	•	•	•	•	•	•
Synchronous Serial Interface (SSI)	•	•	•	•	•	•
Fast Ethernet Controller (FEC)	1	1	2	2	2	2
UARTs	3	3	3	3	3	3
I^2C	•	•	•	•	•	•
DSPI	•	•	•	•	•	•
Real Time Clock	•	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4	4
Watchdog Timer (WDT)	•	•	•	•	•	•
Periodic Interrupt Timers (PIT)	4	4	4	4	4	4
Edge Port Module (EPORT)	•	•	•	•	•	•
Interrupt Controllers (INTC)	2	2	2	2	2	2
16-channel Direct Memory Access (DMA)	•	•	•	•	•	•
General Purpose I/O (GPIO)	•	•	•	•	•	•
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•	•	•
Package	256 MAPBGA		360 TEPBGA			

2 Ordering Information

Table 2. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Temperature
MCF54450CVM180	MCF54450 Microprocessor	256 MAPBGA	180 MHz	–40° to +85° C
MCF54450VM240			240 MHz	0° to +70° C
MCF54451CVM180	MCF54451 Microprocessor		180 MHz	–40° to +85° C
MCF54451VM240			240 MHz	0° to +70° C
MCF54452CVR200	MCF54452 Microprocessor	360 TEPBGA	200 MHz	–40° to +85° C
MCF54452YVR200			200 MHz	–40° to +105° C
MCF54452VR266			266 MHz	0° to +70° C
MCF54453CVR200	MCF54453 Microprocessor		200 MHz	–40° to +85° C
MCF54453VR266			266 MHz	0° to +70° C
MCF54454CVR200	MCF54454 Microprocessor		200 MHz	–40° to +85° C
MCF54454VR266			266 MHz	0° to +70° C
MCF54455CVR200	MCF54455 Microprocessor		200 MHz	–40° to +85° C
MCF54455VR266			266 MHz	0° to +70° C

3 Hardware Design Considerations

3.1 Analog Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for the analog V_{DD} pins (VDD_A_PLL, VDD_RTC). The filter shown in Figure 2 should be connected between the board IV_{DD} and the analog pins. The resistor and capacitors should be placed as close to the dedicated analog V_{DD} pin as possible. The 10-Ω resistor in the given filter is required. Do not implement the filter circuit using only capacitors. The analog power pins draw very little current. Concerns regarding voltage loss across the 10-ohm resistor are not valid.

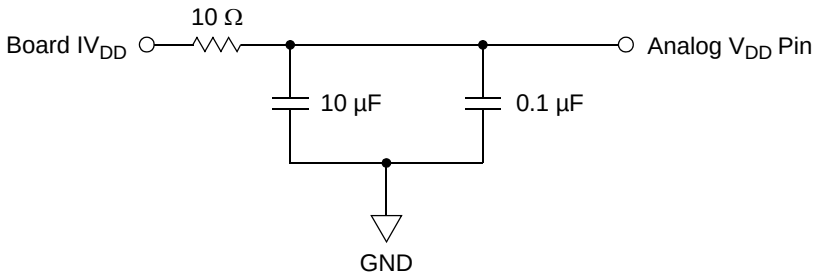


Figure 2. System Analog V_{DD} Power Filter

3.2 Oscillator Power Filtering

Figure 3 shows an example for isolating the oscillator power supply from the I/O supply (EVDD) and ground.

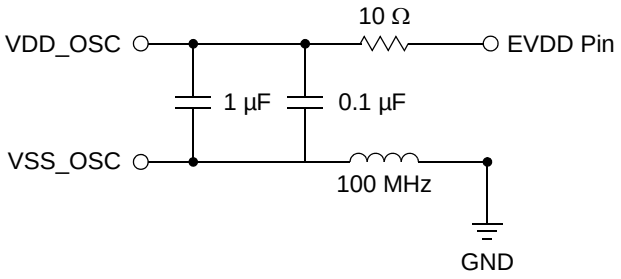
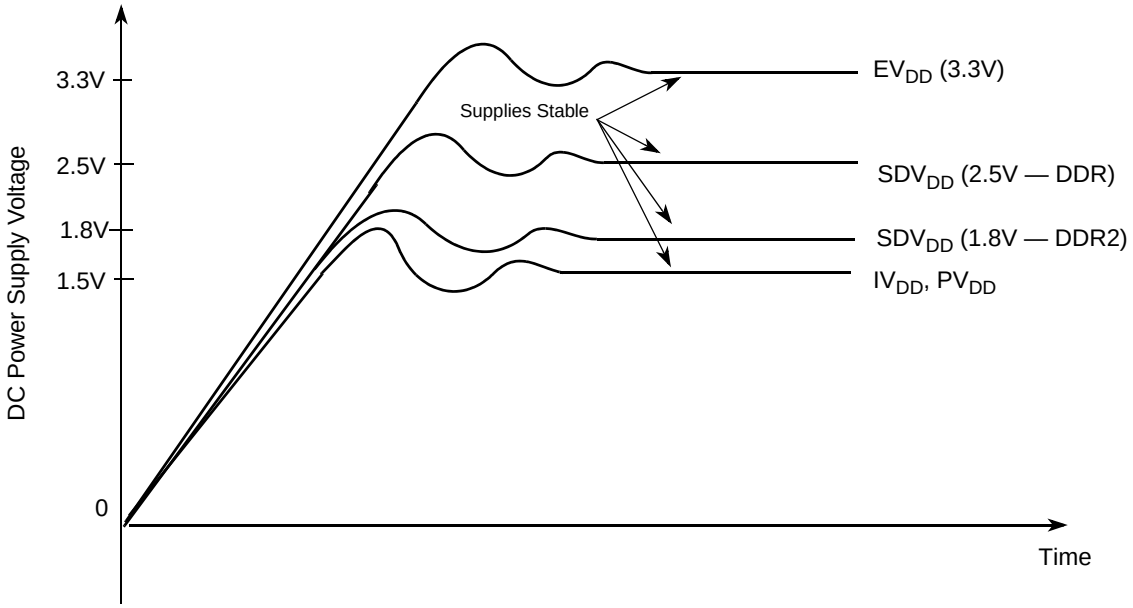


Figure 3. Oscillator Power Filter

3.3 Supply Voltage Sequencing

Figure 4 shows situations in sequencing the I/O V_{DD} (EV_{DD}), SDRAM V_{DD} (SDV_{DD}), PLL V_{DD} (PV_{DD}), and internal logic/core V_{DD} (IV_{DD}).



Notes:
1. Input voltage must not be greater than the supply voltage (EV_{DD}, SDV_{DD}, IV_{DD}, or PV_{DD}) by more than 0.5V at any time, including during power-up.
2. Use 50 V/millisecond or slower rise time for all supplies.

Figure 4. Supply Voltage Sequencing and Separation Cautions

The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. SDV_{DD} (2.5V or 1.8V) and EV_{DD} are specified relative to IV_{DD}.

3.3.1 Power-Up Sequence

If EV_{DD}/SDV_{DD} are powered up with the IV_{DD} at 0 V, the sense circuits in the I/O pads cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must power up. The rise times on the power supplies should be slower than 50 V/millisecond to avoid turning on the internal ESD protection clamp diodes.

3.3.2 Power-Down Sequence

If IV_{DD}/PV_{DD} are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and PV_{DD} power down before EV_{DD} or SDV_{DD} must power down. There are no requirements for the fall times of the power supplies.

4 Pin Assignments and Reset States

4.1 Signal Multiplexing

The following table lists all the MCF5445*x* pins grouped by function. The Dir column is the direction for the primary function of the pin only. Refer to Section 4, “Pin Assignments and Reset States,” for package diagrams. For a more detailed discussion of the MCF5445*x* signals, consult the *MCF54455 Reference Manual* (MCF54455RM).

NOTE

In this table and throughout this document, a single signal within a group is designated without square brackets (i.e., FB_AD23), while designations for multiple signals within a group use brackets (i.e., FB_AD[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Most pins that are muxed with GPIO default to their GPIO functionality. See Table 3 for a list of the exceptions.

Table 3. Special-Case Default Signal Functionality

Pin	256 MAPBGA	360 TEPBGA
FB_AD[31:0]	FB_AD[31:0] except when serial boot selects 0-bit boot port size.	
$\overline{\text{FB\_BE/BWE}}$[3:0]	$\overline{\text{FB\_BE/BWE}}$[3:0]	
$\overline{\text{FB\_CS}}$[3:1]	$\overline{\text{FB\_CS}}$[3:1]	
$\overline{\text{FB\_OE}}$	$\overline{\text{FB\_OE}}$	
FB_R/$\overline{\text{W}}$	FB_R/$\overline{\text{W}}$	
$\overline{\text{FB\_TA}}$	$\overline{\text{FB\_TA}}$	
$\overline{\text{FB\_TS}}$	$\overline{\text{FB\_TS}}$	

Table 4. MCF5445*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
SD_BA[1:0]	—	—	—	—	O	SDVDD	P4, T5	P22, P19
$\overline{\text{SD\_CAS}}$	—	—	—	—	O	SDVDD	T6	L19
SD_CKE	—	—	—	—	O	SDVDD	N5	N22
SD_CLK	—	—	—	—	O	SDVDD	T9	L22
$\overline{\text{SD\_CLK}}$	—	—	—	—	O	SDVDD	T8	M22
$\overline{\text{SD\_CS}}$[1:0]	—	—	—	—	O	SDVDD	P6, R6	L20, M20
SD_D[31:16]	—	—	—	—	I/O	SDVDD	N6, T7, N7, P7, R7, R8, P8, N8, N9, T10, R10, P10, N10, T11, R11, P11	L21, K22, K21, K20, J20, J19, J21, J22, H20, G22, G21, G20, G19, F22, F21, F20
SD_DM[3:2]	—	—	—	—	O	SDVDD	P9, N12	H21, E21
SD_DQS[3:2]	—	—	—	—	O	SDVDD	R9, N11	H22, E22
$\overline{\text{SD\_RAS}}$	—	—	—	—	O	SDVDD	P5	N21
SD_VREF	—	—	—	—	I	SDVDD	M8	M21
$\overline{\text{SD\_WE}}$	—	—	—	—	O	SDVDD	R5	N20
External Interrupts Port[6]								
$\overline{\text{IRQ7}}$	PIRQ7	—	—	—	I	EVDD	L1	ABB13
$\overline{\text{IRQ4}}$	PIRQ4	—	SSI_CLKIN	—	I	EVDD	L2	ABB13
$\overline{\text{IRQ3}}$	PIRQ3	—	—	—	I	EVDD	L3	AB14
$\overline{\text{IRQ1}}$	PIRQ1	$\overline{\text{PCI\_INTA}}$	—	—	I	EVDD	F15	C6
FEC0								
FEC0_MDC	PFECI2C3	—	—	—	O	EVDD	F3	AB8
FEC0_MDIO	PFECI2C2	—	—	—	I/O	EVDD	F2	Y7
FEC0_COL	PFEC0H4	—	ULPI_DATA7	—	I	EVDD	E1	AB7
FEC0_CRS	PFEC0H0	—	ULPI_DATA6	—	I	EVDD	F1	AA7
FEC0_RXCLK	PFEC0H3	—	ULPI_DATA1	—	I	EVDD	G1	AA8
FEC0_RXDV	PFEC0H2	FEC0_RMII_ CRS_DV	—	—	I	EVDD	G2	Y8
FEC0_RXD[3:2]	PFEC0L[3:2]	—	ULPI_DATA[5:4]	—	I	EVDD	G3, G4	AB9, Y9
FEC0_RXD1	PFEC0L1	FEC0_RMII_RXD1	—	—	I	EVDD	H1	W9
FEC0_RXD0	PFEC0H1	FEC0_RMII_RXD0	—	—	I	EVDD	H2	AB10
FEC0_RXER	PFEC0L0	FEC0_RMII_RXER	—	—	I	EVDD	H3	AA10

Table 4. MCF5445*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
FEC0_TXCLK	PFEC0H7	FEC0_RMII_ REF_CLK	—	—	I	EVDD	H4	Y10
FEC0_TXD[3:2]	PFEC0L[7:6]	—	ULPI_DATA[3:2]	—	O	EVDD	J1, J2	W10, AB11
FEC0_TXD1	PFEC0L5	FEC0_RMII_TXD1	—	—	O	EVDD	J3	AA11
FEC0_TXD0	PFEC0H5	FEC0_RMII_TXD0	—	—	O	EVDD	J4	Y11
FEC0_TXEN	PFEC0H6	FEC0_RMII_TXEN	—	—	O	EVDD	K1	W11
FEC0_TXER	PFEC0L4	—	ULPI_DATA0	—	O	EVDD	K2	AB12
FEC1								
FEC1_MDC	PFECI2C5	—	$\overline{\text{ATA\_DIOR}}$	—	O	EVDD	—	W20
FEC1_MDIO	PFECI2C4	—	$\overline{\text{ATA\_DIOW}}$	—	I/O	EVDD	—	Y22
FEC1_COL	PFEC1H4	—	ATA_DATA7	—	I	EVDD	—	AB18
FEC1_CRS	PFEC1H0	—	ATA_DATA6	—	I	EVDD	—	AA18
FEC1_RXCLK	PFEC1H3	—	ATA_DATA5	—	I	EVDD	—	W14
FEC1_RXDV	PFEC1H2	FEC1_RMII_ CRS_DV	ATA_DATA15	—	I	EVDD	—	AB15
FEC1_RXD[3:2]	PFEC1L[3:2]	—	ATA_DATA[4:3]	—	I	EVDD	—	AA15, Y15
FEC1_RXD1	PFEC1L1	FEC1_RMII_RXD1	ATA_DATA14	—	I	EVDD	—	AA17
FEC1_RXD0	PFEC1H1	FEC1_RMII_RXD0	ATA_DATA13	—	I	EVDD	—	Y17
FEC1_RXER	PFEC1L0	FEC1_RMII_RXER	ATA_DATA12	—	I	EVDD	—	W17
FEC1_TXCLK	PFEC1H7	FEC1_RMII_ REF_CLK	ATA_DATA11	—	I	EVDD	—	AB19
FEC1_TXD[3:2]	PFEC1L[7:6]	—	ATA_DATA[2:1]	—	O	EVDD	—	Y19, W18
FEC1_TXD1	PFEC1L5	FEC1_RMII_TXD1	ATA_DATA10	—	O	EVDD	—	AA19
FEC1_TXD0	PFEC1H5	FEC1_RMII_TXD0	ATA_DATA9	—	O	EVDD	—	Y20
FEC1_TXEN	PFEC1H6	FEC1_RMII_TXEN	ATA_DATA8	—	O	EVDD	—	AA21
FEC1_TXER	PFEC1L4	—	ATA_DATA0	—	O	EVDD	—	AA22
USB On-the-Go								
USB_DM	—	—	—	—	O	USB VDD	F16	A14
USB_DP	—	—	—	—	O	USB VDD	E16	A15
USB_VBUS_EN	PUSB1	USB_PULLUP	ULPI_NXT	—	O	USB VDD	E5	AA2
USB_VBUS_OC	PUSB0	—	ULPI_STP	UD[7]	I	USB VDD	B3	V4

4.3 Pinout—360 TEPBGA

The pinout for the MCF54452, MCF54453, MCF54454, and MCF54455 packages are shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A		PCI_REQ0	PCI_AD10	PCI_AD11	PCI_AD13	PCI_SERR	PCI_STOP	PCI_AD15	PCI_GNT0	PCI_AD29	PCI_AD20	XTAL 32K	EXTAL 32K	USB_DM	USB_DP	EXTAL	XTAL	DACK0	DSPI_PCS2	DSPI_SCK	TDO		A
B	PCI_CBE0	PCI_FRAME	PCI_AD9	PCI_PERR	PCI_AD12	PCI_RST	PCI_GNT3	PCI_AD14	PCI_AD18	PCI_AD28	PCI_AD19	PCI_AD21	NC		NC	VDD_OSC	RSTOUT	DREQ0	DSPI_SIN	DSPI_PCS1	TMS	TRST	B
C	PCI_AD0	PCI_AD2	PCI_IRDY	PCI_PAR	PCI_REQ1	IRQ1	PCI_REQ3	PCI_GNT2	PCI_GNT1	PCI_TRDY	PCI_AD31	PCI_AD22	VDD_RTC	VDD_A_PLL	NC	VSS_OSC	DACK1	DREQ1	TDI	DSPI_SOUT	JTAG_EN	TCLK	C
D	PCI_CBE1	PCI_AD1	PCI_AD7	PCI_AD8	PCI_IDSEL	IVDD	PCI_REQ2	IVDD	PCI_AD17	PCI_AD16	PCI_AD30	PCI_AD23	EVDD	IVDD	PLL TEST	NC	DSPI_PCS0	DSPI_PCS5	EVDD	SSI_MCLK	SSI_RXD	SSI_TXD	D
E	PCI_AD4	PCI_AD5	PCI_AD6	PCI_CBE2															SSI_BCLK	SSI_FS	SD_DM2	SD_DQS2	E
F	PCI_AD24	PCI_DEVSEL	PCI_AD3	IVDD																SD_D16	SD_D17	SD_D18	F
G	T0IN	PCI_AD26	PCI_AD25	PCI_CBE3				EVDD			EVDD			EVDD		EVDD			SD_D19	SD_D20	SD_D21	SD_D22	G
H	T2IN	T3IN	T1IN	IVDD																SD_D23	SD_DM3	SD_DQS3	H
J	FB_AD29	FB_AD31	FB_CLK	PCI_AD27				EVDD								EVDD			SD_D26	SD_D27	SD_D25	SD_D24	J
K	FB_AD28	FB_AD27	FB_AD26	FB_AD30																SD_D28	SD_D29	SD_D30	K
L	FB_AD25	FB_AD23	FB_AD22	FB_AD24				EVDD								EVDD			SD_CAS	SD_CS1	SD_D31	SD_CLK	L
M	FB_AD21	FB_AD20	FB_AD19	FB_AD18																SD_CS0	SD_VREF	SD_CLK	M
N	FB_AD17	FB_AD16	U1TXD	IVDD												EVDD			SD_A2	SD_WE	SD_RAS	SD_CKE	N
P	FB_AD15	FB_AD14	U1RXD	FB_AD10				EVDD											SD_BA0	SD_A1	SD_A0	SD_BA1	P
R	FB_AD13	FB_AD12	FB_AD11	IVDD												EVDD				SD_A5	SD_A4	SD_A3	R
T	FB_AD9	FB_AD8	FB_AD7	FB_AD6				EVDD			EVDD			EVDD		EVDD			SD_A9	SD_A8	SD_A7	SD_A6	T
U	FB_AD5	FB_AD4	FB_AD3	U1RTS																SD_A12	SD_A11	SD_A10	U
V	FB_AD2	FB_AD1	U1CTS	USB_VBUS_OC															ATA_DA2	ATA_DA1	ATA_DA0	SD_A13	V
W	FB_AD0	FB_BE/BWE2	FB_BE/BWE1	IVDD	FB_CS3	PST DDATA4	IVDD	IVDD	FEC0_RXD1	FEC0_TXD3	FEC0_TXEN	IVDD	ATA_RESET	FEC1_RXCLK	U0TXD	IVDD	FEC1_RXER	FEC1_TXD2	IVDD	FEC1_MDC	ATA_CS1	ATA_CS0	W
Y	FB_BE/BWE3	FB_BE/BWE0	FB_TS	FB_CS0	PST DDATA0	PST DDATA3	FEC0_MDIO	FEC0_RXDV	FEC0_RXD2	FEC0_TXCLK	FEC0_TXD0	I2C_SDA	ATA_BUFFER_EN	ATA_IORDY	FEC1_RXD2	U0CTS	FEC1_RXD0	RESET	FEC1_TXD3	FEC1_TXD0	NC	FEC1_MDIO	Y
AA	FB_OE	USB_VBUS_EN	FB_R/W	FB_CS2	PST DDATA2	PST DDATA7	FEC0_CRS	FEC0_RXCLK	NC	FEC0_RXER	FEC0_TXD1	I2C_SCL	IRQ4	ATA_DMARQ	FEC1_RXD3	U0RTS	FEC1_RXD1	FEC1_CRS	FEC1_TXD1	NC	FEC1_TXEN	FEC1_TXER	AA
AB		FB_TA	FB_CS1	PST DDATA1	PST DDATA5	PST DDATA6	FEC0_COL	FEC0_MDC	FEC0_RXD3	FEC0_RXD0	FEC0_TXD2	FEC0_TXER	IRQ7	IRQ3	FEC1_RXDV	U0RXD	BOOT MOD1	FEC1_COL	FEC1_TXCLK	TEST	BOOT MOD0		AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure 6. MCF54452, MCF54453, MCF54454, and MCF54455 Pinout (360 TEPBGA)

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

5.3 ESD Protection

Table 7. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 8. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Units
Internal logic supply voltage[1]	IV_{DD}	1.35	1.65	V
PLL analog operation voltage range [1]	PV_{DD}	1.35	1.65	V
External I/O pad supply voltage	EV_{DD}	3.0	3.6	V
Internal oscillator supply voltage	$OSCV_{DD}$	3.0	3.6	V
Real-time clock supply voltage	$RTCV_{DD}$	1.35	1.65	V
SDRAM I/O pad supply voltage — DDR mode	SDV_{DD}	2.25	2.75	V
SDRAM I/O pad supply voltage — DDR2 mode	SDV_{DD}	1.7	1.9	V
SDRAM I/O pad supply voltage — Mobile DDR mode	SDV_{DD}	1.7	1.9	V
SDRAM input reference voltage	SDV_{REF}	0.49 x SDV_{DD}	0.51 x SDV_{DD}	V
Input High Voltage	V_{IH}	0.7 x EV_{DD}	3.65	V
Input Low Voltage	V_{IL}	V_{SS} – 0.3	0.35 x EV_{DD}	V
Input Hysteresis	V_{HYS}	0.06 x EV_{DD}	—	mV
Input Leakage Current[2] V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–2.5	2.5	µA
Input Leakage Current[3] V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–5	5	µA
High Impedance (Off-State) Leakage Current[4] V_{in} = V_{DD} or V_{SS}, All input/output and output pins	I_{OZ}	–10.0	10.0	µA
Output High Voltage (All input/output and all output pins) I_{OH} = –5.0 mA	V_{OH}	0.85 × EV_{DD}	—	V
Output Low Voltage (All input/output and all output pins) I_{OL} = 5.0mA	V_{OL}	—	0.15 × EV_{DD}	V

Table 8. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Units
Weak Internal Pull Up Device Current, tested at V_{IL} Max.[5]	I_{APU}	–10	–130	µA
Input Capacitance [6] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF
Load Capacitance Low drive strength High drive strength	C_L		 25 50	pF
DC Injection Current [3, 7, 8, 9] $V_{NEGCLAMP}$ =V_{SS}– 0.3 V, $V_{POSCLAMP}$ = V_{DD} + 0.3 Single Pin Limit Total MCU Limit, Includes sum of all stressed pins	I_{IC}	 -1.0 -10	 1.0 10	mA

1 IV_{DD} and PV_{DD} should be at the same voltage. PV_{DD} should have a filtered input. Please see the PLL section of this specification for an example circuit. There are three PV_{DD} inputs, one for each PLL. A filter circuit should used on each PV_{DD} input.

2 Valid for all parts, EXCEPT the MCF54452YVR200.

3 Valid just the MCF54452YVR200 part number.

4 Worst-case tristate leakage current with only one I/O pin high. Since all I/Os share power when high, the leakage current is distributed among them. With all I/Os high, this spec reduces to ±2 µA min/max.

5 Refer to the *MCF54455 Reference Manual* signals description chapter for pins having weak internal pull-up devices.

6 This parameter is characterized before qualification rather than 100% tested.

7 All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD}.

8 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

9 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure the external V_{DD} load shunts current greater than the maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, at power-up, the system clock is not present during the power-up sequence until the PLL has attained lock.

5.5 Clock Timing Specifications

The clock module configures the device for one of several clocking methods. Clocking modes include internal phase-locked loop (PLL) clocking with an external clock reference or an external crystal reference supported by an internal crystal amplifier. The PLL can also be disabled, and an external oscillator can directly clock the device.

The specifications in Table 9 are for the CLKIN input pin (EXTAL input driven by an external clock reference). The duty cycle specification is based on an acceptable tolerance for the PLL, which yields 50% duty-cycle internal clocks to all on-chip peripherals. The MCF5445*x* devices use the input clock signal as its synchronous bus clock for PCI. A poor duty cycle on the input clock, may affect the overall timing margin to external devices. If negative edge logic is used to interface to PCI, providing a 50% duty-cycle input clock aids in simplifying overall system design.

Table 9. Input Clock Timing Requirements

Item	Specification	Min	Max	Unit
C1	Cycle time	15	40	ns
1 / C1	Frequency	25	66.66	MHz
C2	Rise time (20% of vdd to 80% of vdd)	-	2	ns
C3	Fall time (80% of vdd to 20% of vdd)	-	2	ns
C4	Duty cycle (at 50% of vdd)	40	60	%

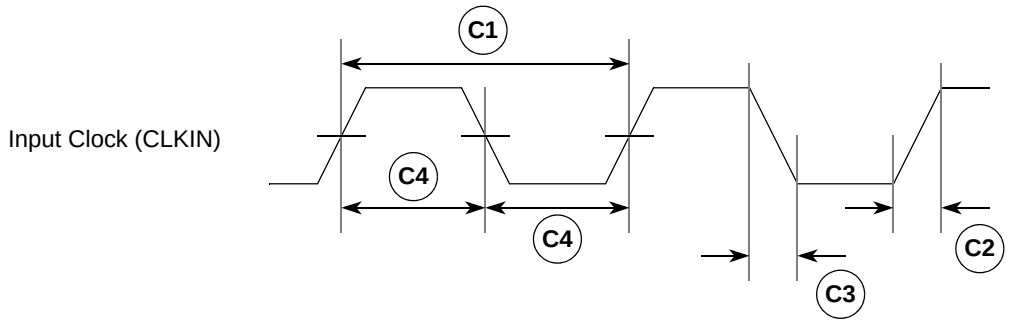


Figure 7. Input Clock Timing Diagram

Table 10. PLL Electrical Characteristics

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	PLL Reference Frequency Range Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 16 16	 40 66.66	 MHz MHz
2	Core/System Frequency	f_{sys}	512 Hz[1]	266.67 MHz	—
	Core/System Clock Period	t_{sys}	—	$1/f_{sys}$	ns
19	VCO Frequency ($f_{vco} = f_{ref} \times PFDR$)	f_{vco}	300	540	MHz
3	Crystal Start-up Time[2, 3]	t_{cst}	—	10	ms
4	EXTAL Input High Voltage Crystal Mode[4] All other modes (External, Limp)	 V_{IHEXT} V_{IHEXT}	 V_{XTAL} + 0.4 $E_{VDD}/2$ + 0.4	 — —	 V V
5	EXTAL Input Low Voltage Crystal Mode[4] All other modes (External, Limp)	 V_{ILEXT} V_{ILEXT}	 — —	 V_{XTAL} - 0.4 $E_{VDD}/2$ - 0.4	 V V
6	EXTAL Input Rise & Fall Time (20% to 80% E_{VDD}) (External, Limp)		1	2	ns
7	PLL Lock Time [3, 5]	t_{lpll}	—	50000	CLKIN
8	Duty Cycle of reference [3] (External, Limp)	t_{dc}	40	60	%
9	XTAL Current	I_{XTAL}	1	3	mA
10	Total on-chip stray capacitance on XTAL	C_{S_XTAL}	—	1.5	pF

Table 10. PLL Electrical Characteristics (continued)

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
11	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
12	Crystal capacitive load	C_L	See crystal spec		
13	Discrete load capacitance for XTAL Discrete load capacitance for EXTAL	C_{L_XTAL} C_{L_EXTAL}	—	$2 \times (C_L - C_{S\_XTAL} - C_{S\_EXTAL} - C_{S\_PCB})$[6]	pF
14	Frequency un-LOCK Range	f_{UL}	-4.0	4.0	% f_{sys}
15	Frequency LOCK Range	f_{LCK}	-2.0	2.0	% f_{sys}
17	CLKOUT Period Jitter, [3, 4, 7] Measured at f_{SYS} Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter	C_{jitter}	 — —	 10 TBD	 % FB_CLK % FB_CLK

1 The minimum system frequency is the minimum input clock divided by the maximum low-power divider (16 MHz ÷ 32,768). When the PLL is enabled, the minimum system frequency (f_{sys}) is 150 MHz.

2 This parameter is guaranteed by characterization before qualification rather than 100% tested. Applies to external clock reference only.

3 Proper PC board layout procedures must be followed to achieve specifications.

4 This parameter is guaranteed by design rather than 100% tested.

5 This specification is the PLL lock time only and does not include oscillator start-up time.

6 C_{S_PCB} is the measured PCB stray capacitance on EXTAL and XTAL.

7 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD}, EV_{DD}, and V_{SS} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

5.6 Reset Timing Specifications

Table 11 lists specifications for the reset timing parameters shown in Figure 8.

Table 11. Reset and Configuration Override Timing

Num	Characteristic	Min	Max	Unit
R1[1]	$\overline{\text{RESET}}$ valid to CLKIN (setup)	9	—	ns
R2	CLKIN to $\overline{\text{RESET}}$ invalid (hold)	1.5	—	ns
R3	$\overline{\text{RESET}}$ valid time[2]	5	—	CLKIN cycles
R4	CLKIN to $\overline{\text{RSTOUT}}$ valid	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Configuration Override inputs valid	0	—	ns
R6	Configuration Override inputs valid to $\overline{\text{RSTOUT}}$ invalid (setup)	20	—	CLKIN cycles
R7	Configuration Override inputs invalid after $\overline{\text{RSTOUT}}$ invalid (hold)	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override inputs High Impedance	—	1	CLKIN cycles

1 $\overline{\text{RESET}}$ and Configuration Override data lines are synchronized internally. Setup and hold times must be met only if recognition on a particular clock is required.

2 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

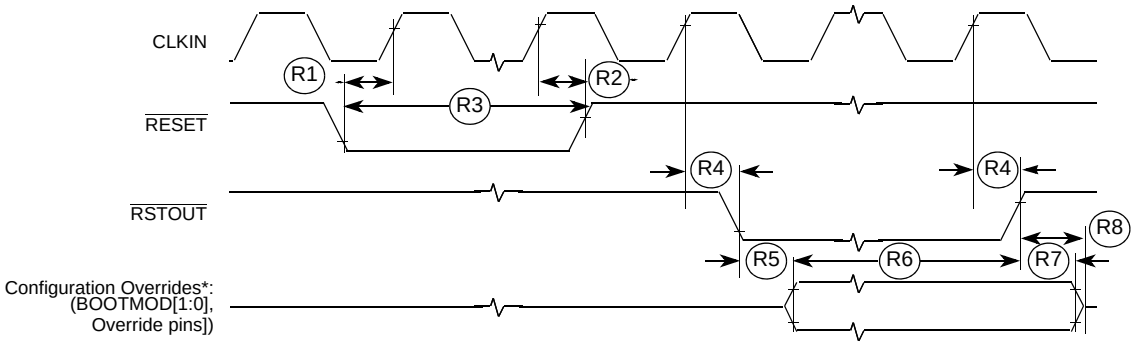


Figure 8. $\overline{\text{RESET}}$ and Configuration Override Timing

5.7 FlexBus Timing Specifications

A multi-function external bus interface called FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 66MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices, a simple chip-select based interface can be used.

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 12. FlexBus AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	25	66.66	MHz	
FB1	Clock Period	15	40	ns	
FB2	Output Valid	—	7.0	ns	[1]
FB3	Output Hold	1.0	—	ns	1
FB4	Input Setup	3.0	—	ns	[2]
FB5	Input Hold	0	—	ns	2

[1] Specification is valid for all FB_AD[31:0], $\overline{\text{FB\_BS}}$[3:0], $\overline{\text{FB\_CS}}$[3:0], $\overline{\text{FB\_OE}}$, FB_R/$\overline{\text{W}}$, $\overline{\text{FB\_TBST}}$, FB_TSIZ[1:0], and $\overline{\text{FB\_TS}}$.

[2] Specification is valid for all FB_AD[31:0] and $\overline{\text{FB\_TA}}$.

NOTE

The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial.

The address and data busses are muxed between the FlexBus and PCI controller. At the end of the read and write bus cycles the address signals are indeterminate.

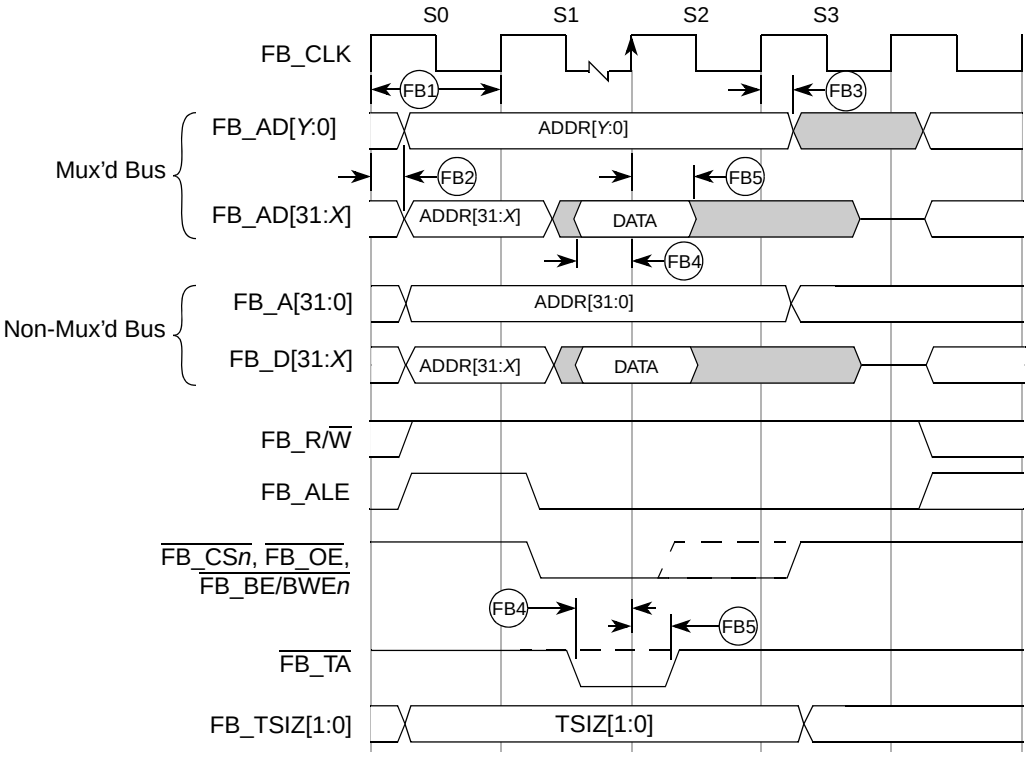


Figure 9. FlexBus Read Timing

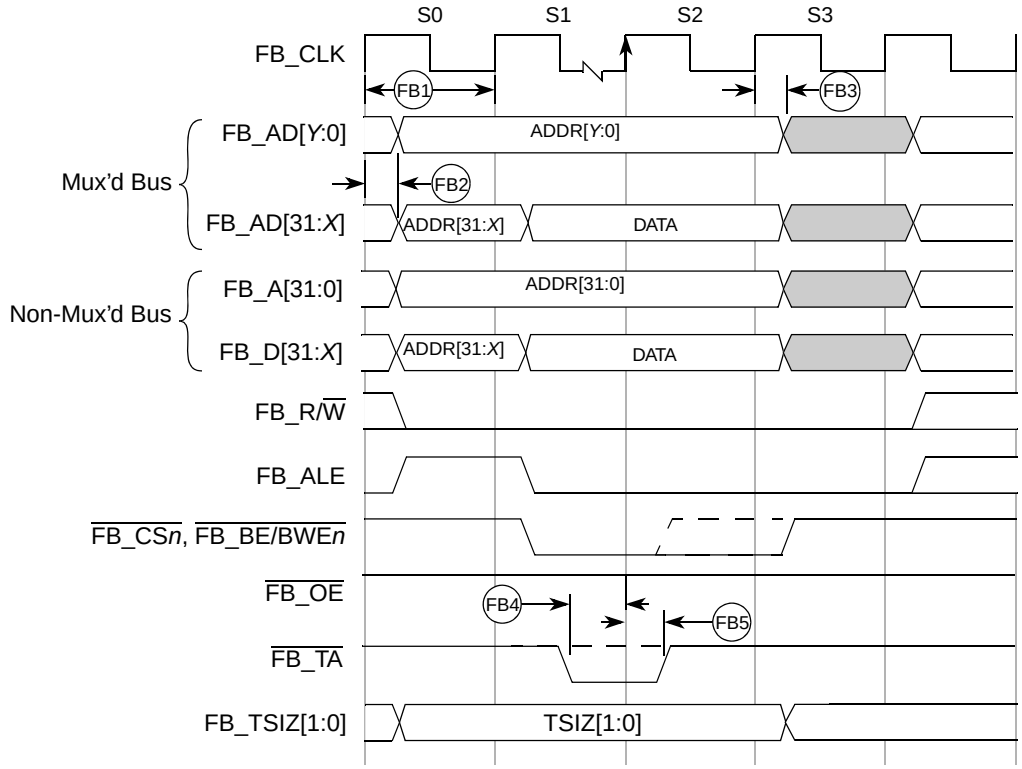


Figure 10. Flexbus Write Timing

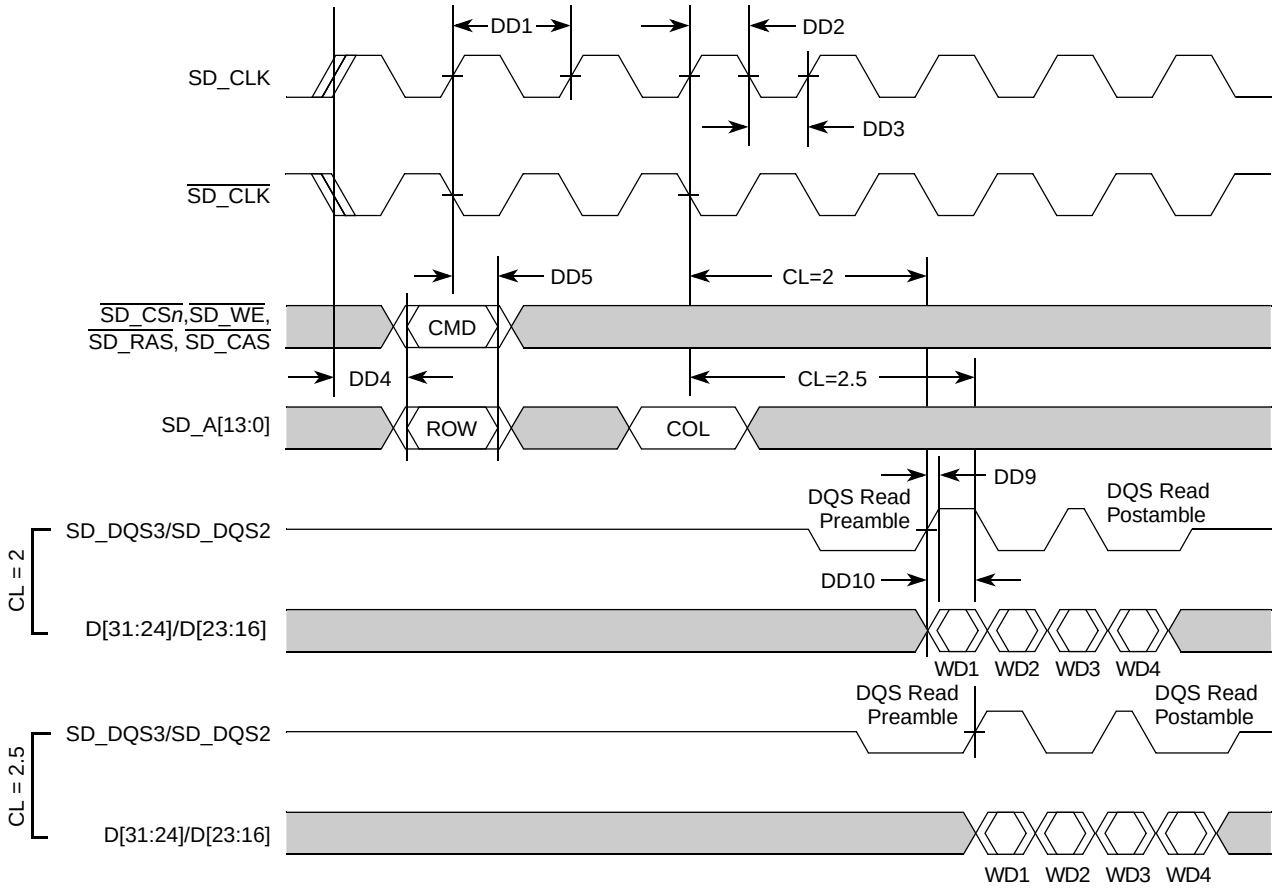


Figure 12. DDR Read Timing

5.9 PCI Bus Timing Specifications

The PCI bus on the device is PCI 2.2 compliant. The following timing numbers are mostly from the PCI 2.2 spec. Refer to the PCI 2.2 spec for a more detailed timing analysis.

Table 14. PCI Timing Specifications[1,2]

Num	Characteristic	33 MHz[3]		66 MHz[3]		
		Min	Max	Min	Max	Unit
	Frequency of Operation	—	33.33	33.33	66.66	MHz
P1	Clock Period	30	—	15	30	ns
P2	Bused PCI signals — input setup	7.0	—	3.0	—	ns
P3	$\overline{\text{PCI\_GNT}}$[3:0]/$\overline{\text{PCI\_REQ}}$[3:0] — input setup	10.0	—	5.0	—	ns
P4	All PCI signals — input hold	0	—	0	—	ns
P5	Bused PCI signals — output valid	—	11.0	—	6.0	ns

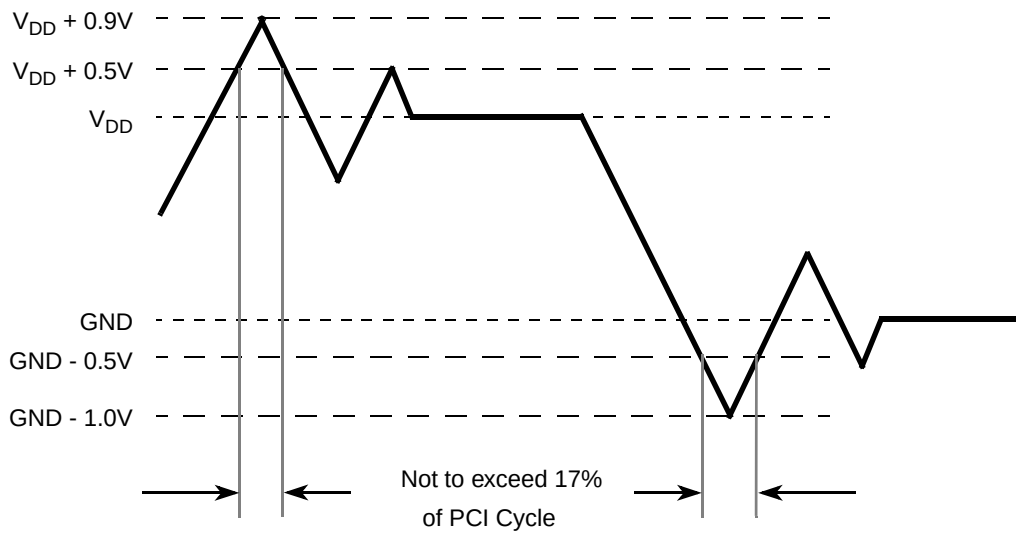


Figure 14. Overshoot and Undershoot Limits

5.10 ULPI Timing Specifications

The ULPI interface is fully compliant with the industry standard UTMI+ Low Pin Interface. Control and data timing requirements for the ULPI pins are given in Table 15. These timings apply to synchronous mode only. All timings are measured with respect to the clock as seen at the USB_CLKIN pin on the MCF5445*x*. The ULPI PHY is the source of the 60MHz clock.

NOTE

The USB controller requires a 60-MHz clock, even if using the on-chip FS/LS transceiver instead of the ULPI interface. In this case, the 60-MHz clock can be generated by the PLL or input on the USB_CLKIN pin.

Table 15. ULPI Interface Timing

Num	Characteristic	Min	Nominal	Max	Units
	USB_CLKIN operating frequency	—	60	—	MHz
	USB_CLKIN duty cycle	—	50	—	%
U1	USB_CLKIN clock period	—	16.67	—	ns
U2	Input Setup (control and data)	5.0	—	—	ns
U3	Input Hold (control and data)	1.0	—	—	ns
U4	Output Valid (control and data)	—	—	9.5	ns
U5	Output Hold (control and data)	1.0	—	—	

Table 19. I²C Output Timing Specifications between SCL and SDA (continued)

Num	Characteristic	Min	Max	Units
I6[1]	Clock high time	10	—	t_{SYS}
I7[1]	Data setup time	2	—	t_{SYS}
I8[1]	Start condition setup time (for repeated start condition only)	20	—	t_{SYS}
I9[1]	Stop condition setup time	10	—	t_{SYS}

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 19. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR. However, the numbers given in Table 19 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

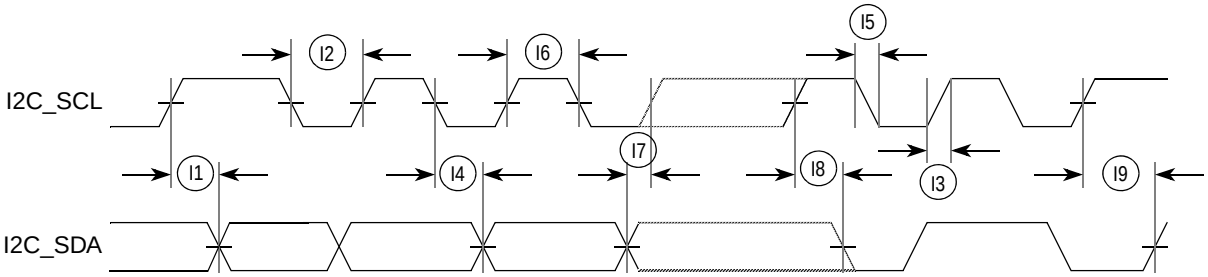


Figure 18. I²C Input/Output Timings

5.13 Fast Ethernet Timing Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

5.13.1 Receive Signal Timing Specifications

The following timing specs meet the requirements for MII and 7-Wire style interfaces for a range of transceiver devices.

Table 20. Receive Signal Timing

Num	Characteristic	MII Mode		RMII Mode		Unit
		Min	Max	Min	Max	
—	RXCLK frequency	—	25	—	50	MHz
E1	RXD[n:0], RXDV, RXER to RXCLK setup[1]	5	—	4	—	ns
E2	RXCLK to RXD[n:0], RXDV, RXER hold[1]	5	—	2	—	ns
E3	RXCLK pulse width high	35%	65%	35%	65%	RXCLK period
E4	RXCLK pulse width low	35%	65%	35%	65%	RXCLK period

1 In MII mode, n = 3; In RMII mode, n = 1

5.15 ATA Interface Timing Specifications

The ATA controller is compatible with the ATA/ATAPI-6 industry standard. Refer to the *ATA/ATAPI-6 Specficiation* and the ATA controller chapter of the *MCF54455 Reference Manual* for timing diagrams of the various modes of operation.

The timings of the various ATA data transfer modes are determined by a set of timing equations described in the ATA section of the *MCF54455 Reference Manual*. These timing equations must be fulfilled for the ATA host to meet timing. Table 25 provides implementation specific timing parameters necessary to complete the timing equations.

Table 25. ATA Interface Timing Specifications[1,2]

Name	Characteristic	Symbol	Min	Max	Unit	Notes
A1	Setup time — ATA_IORDY to SYSCLK falling	t_{SUI}	4.0	—	ns	
A2	Hold time — ATA_IORDY from SYSCLK falling	t_{HI}	3.0	—	ns	
A3	Setup time — ATA_DATA[15:0] to SYSCLK rising	t_{SU}	4.0	—	ns	
A4	Propagation delay — SYSCLK rising to all outputs	t_{CO}	—	7.0	ns	3
A5	Output skew	t_{SKEW1}	—	1.5	ns	3
A6	Setup time — ATA_DATA[15:0] valid to ATA_IORDY	t_{I_DS}	2.0	—	ns	4
A7	Hold time — ATA_IORDY to ATA_DATA[15:0] invalid	t_{I_DH}	3.5	—	ns	4

1 These parameters are guaranteed by design and not testable.

2 All timings specified with a capacitive load of 40pF.

3 Applies to $\overline{\text{ATA\_CS}}$[1:0], ATA_DA[2:0], ATA_DIOR, ATA_DIOW, ATA_DMACK, ATA_DATA[15:0]

4 Applies to Ultra DMA data-in burst only

5.16 DSPI Timing Specifications

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. Table 26 provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the *MCF54455 Reference Manual* for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 26. DSPI Module AC Timing Specifications[1]

Name	Characteristic	Symbol	Min	Max	Unit	Notes
DS1	DSPI_SCK Cycle Time	t_{SCK}	4 x t_{SYS}	—	ns	2
DS2	DSPI_SCK Duty Cycle	—	(t_{sck} ÷ 2) - 2.0	(t_{sck} ÷ 2) + 2.0	ns	3
Master Mode						
DS3	DSPI_PCS*n* to DSPI_SCK delay	t_{CSC}	(2 × t_{SYS}) - 1.5	—	ns	4
DS4	DSPI_SCK to DSPI_PCS*n* delay	t_{ASC}	(2 × t_{SYS}) - 3.0	—	ns	5
DS5	DSPI_SCK to DSPI_SOUT valid	—	—	5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	—	-5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	—	9	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	—	0	—	ns	
Slave Mode						
DS9	DSPI_SCK to DSPI_SOUT valid	—	—	10	ns	

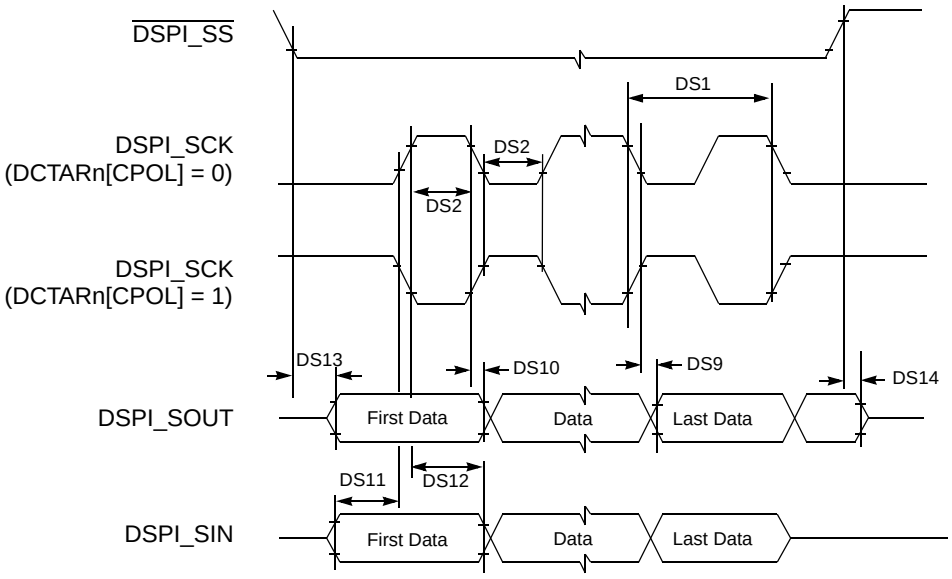


Figure 24. DSPI Classic SPI Timing—Slave Mode

5.17 SBF Timing Specifications

The Serial Boot Facility (SBF) provides a means to read configuration information and system boot code from a broad array of SPI-compatible EEPROMs, flashes, FRAMs, nVSRAMs, etc. Table 27 provides the AC timing specifications for the SBF.

Table 27. SBF AC Timing Specifications

Name	Characteristic	Symbol	Min	Max	Unit	Notes
SB1	SBF_CK Cycle Time	t_{SBFCK}	40	—	ns	[1]
SB2	SBF_CK High/Low Time	—	30%	—	t_{SBFCK}	
SB3	$\overline{\text{SBF\_CS}}$ to SBF_CK delay	—	t_{SBFCK} - 2.0	—	ns	
SB4	SBF_CK to $\overline{\text{SBF\_CS}}$ delay	—	t_{SBFCK} - 2.0	—	ns	
SB5	SBF_CK to SBF_DO valid	—	-5	—	ns	
SB6	SBF_CK to SBF_DO invalid	—	5	—	ns	
SB7	SBF_DI to SBF_SCK input setup	—	10	—	ns	
SB8	SBF_CK to SBF_DI input hold	—	0	—	ns	

[1] At reset, the SBF_CK cycle time is $t_{REF} \times 67$. The first byte of data read from the serial memory contains a divider value that is used to set the SBF_CK cycle time for the duration of the serial boot process.

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Document Number: MCF54455
Rev. 8
02/2012

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