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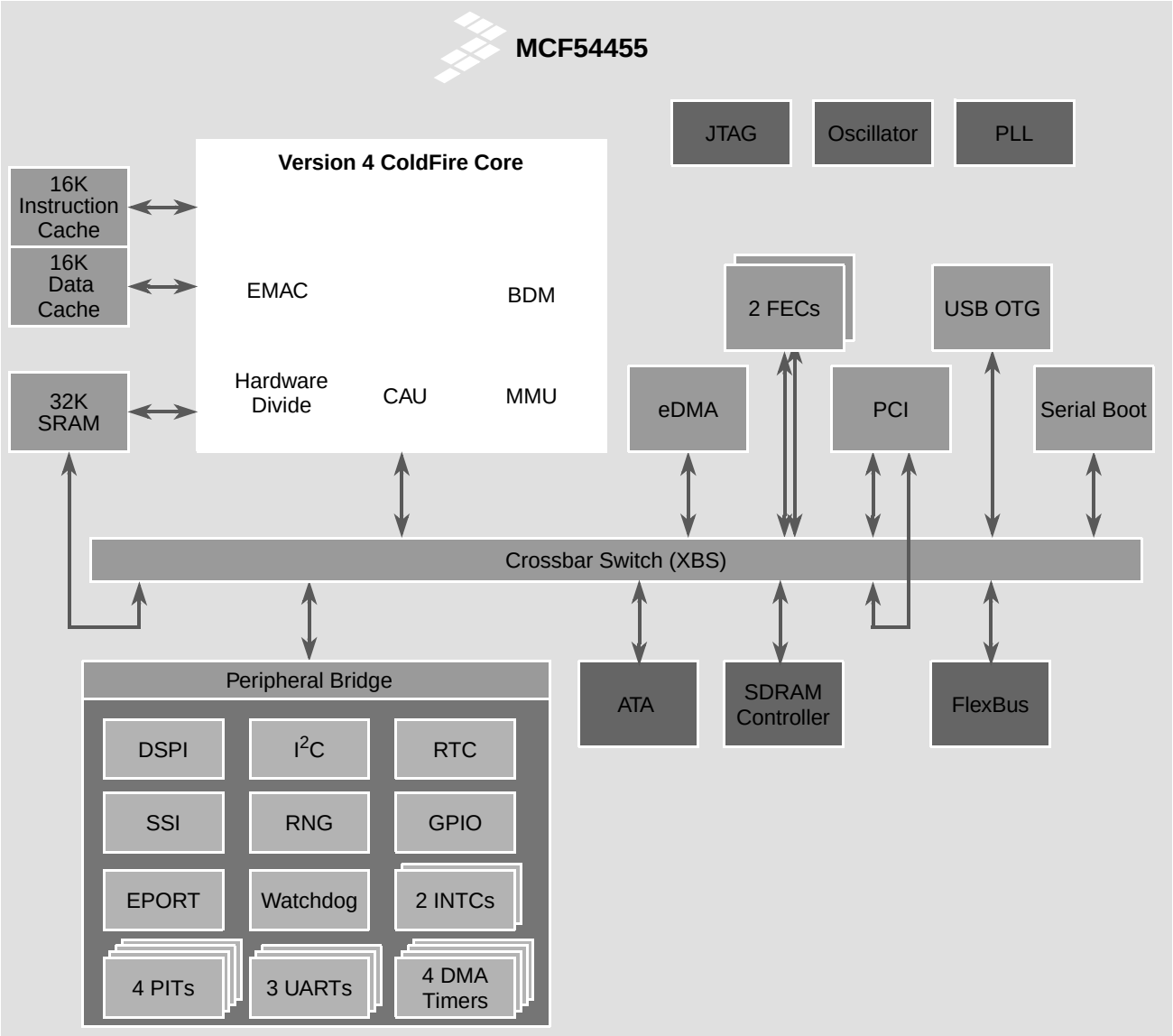
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V4
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	I²C, SPI, SSI, UART/USART, USB OTG
Peripherals	DMA, WDT
Number of I/O	132
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	360-BBGA
Supplier Device Package	360-TEPBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf54455cvr200



LEGEND

ATA	– Advanced Technology Attachment Controller	**INTC**	– Interrupt controller
BDM	– Background debug module	**JTAG**	– Joint Test Action Group interface
CAU	– Cryptography acceleration unit	**MMU**	– Memory management unit
DSPI	– DMA serial peripheral interface	**PCI**	– Peripheral Component Interconnect
eDMA	– Enhanced direct memory access	**PIT**	– Programmable interrupt timers
EMAC	– Enchance multiply-accumulate unit	**PLL**	– Phase locked loop module
EPORT	– Edge port module	**RNG**	– Random Number Generator
FEC	– Fast Ethernet controller	**RTC**	– Real time clock
GPIO	– General Purpose Input/Output	**SSI**	– Synchronous Serial Interface
I^{2}C	– Inter-Intergrated Circuit	**USB OTG**	– Universal Serial Bus On-the-Go controller

Figure 1. MCF54455 Block Diagram

3.2 Oscillator Power Filtering

Figure 3 shows an example for isolating the oscillator power supply from the I/O supply (EVDD) and ground.

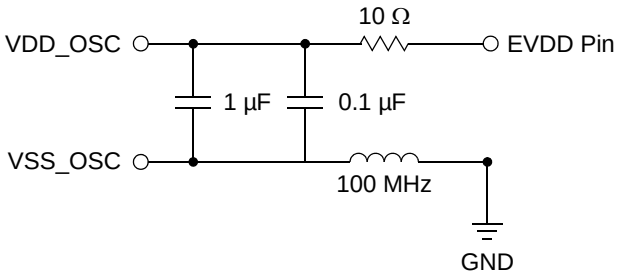
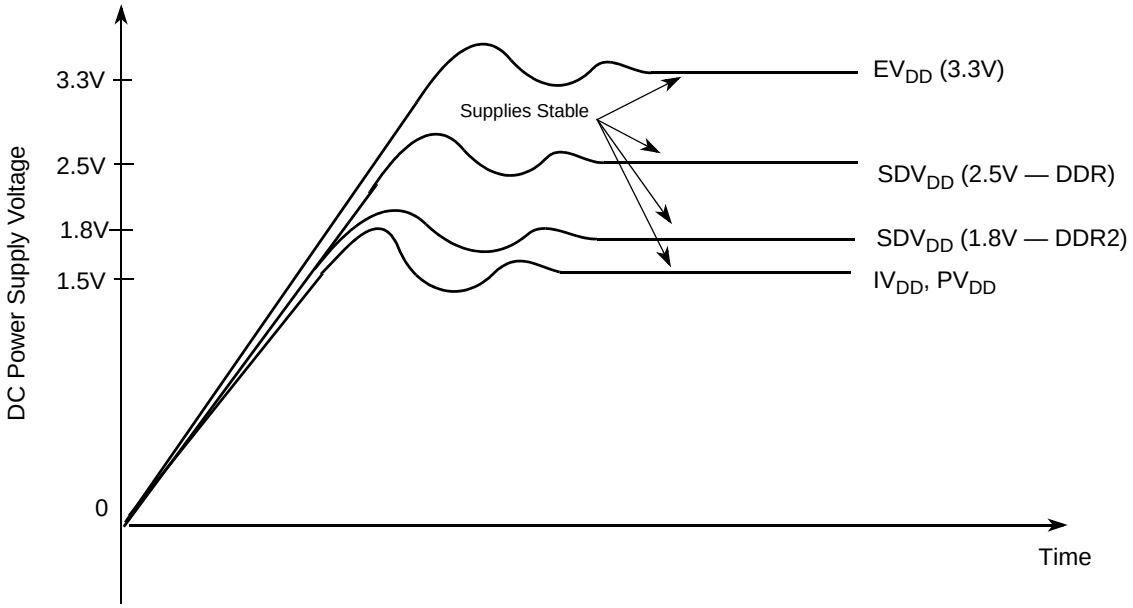


Figure 3. Oscillator Power Filter

3.3 Supply Voltage Sequencing

Figure 4 shows situations in sequencing the I/O V_{DD} (EV_{DD}), SDRAM V_{DD} (SDV_{DD}), PLL V_{DD} (PV_{DD}), and internal logic/core V_{DD} (IV_{DD}).



Notes:
1. Input voltage must not be greater than the supply voltage (EV_{DD}, SDV_{DD}, IV_{DD}, or PV_{DD}) by more than 0.5V at any time, including during power-up.
2. Use 50 V/millisecond or slower rise time for all supplies.

Figure 4. Supply Voltage Sequencing and Separation Cautions

The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. SDV_{DD} (2.5V or 1.8V) and EV_{DD} are specified relative to IV_{DD}.

Table 3. Special-Case Default Signal Functionality (continued)

Pin	256 MAPBGA	360 TEPBGA
$\overline{\text{PCI\_GNT}}$[3:0]	GPIO	$\overline{\text{PCI\_GNT}}$[3:0]
$\overline{\text{PCI\_REQ}}$[3:0]	GPIO	$\overline{\text{PCI\_REQ}}$[3:0]
$\overline{\text{IRQ1}}$	GPIO	$\overline{\text{PCI\_INTA}}$ and configured as an agent.
ATA_RESET	GPIO	ATA reset

Table 4. MCF5445*x* Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
Reset								
$\overline{\text{RESET}}$	—	—	—	U	I	EVDD	L4	Y18
$\overline{\text{RSTOUT}}$	—	—	—	—	O	EVDD	M15	B17
Clock								
EXTAL/PCI_CLK	—	—	—	—	I	EVDD	M16	A16
XTAL	—	—	—	U[3]	O	EVDD	L16	A17
Mode Selection								
BOOTMOD[1:0]	—	—	—	—	I	EVDD	M5, M7	AB17, AB21
FlexBus								
FB_AD[31:24]	PFBADH[7:0][4]	FB_D[31:24]	—	—	I/O	EVDD	A14, A13, D12, C12, B12, A12, D11, C11	J2, K4, J1, K1–3, L1, L4
FB_AD[23:16]	PFBADMH[7:0][4]	FB_D[23:16]	—	—	I/O	EVDD	B11, A11, D10, C10, B10, A10, D9, C9	L2, L3, M1–4, N1–2
FB_AD[15:8]	PFBADML[7:0][4]	FB_D[15:8]	—	—	I/O	EVDD	B9, A9, D8, C8, B8, A8, D7, C7	P1–2, R1–3, P4, T1–2
FB_AD[7:0]	PFBADL[7:0][4]	FB_D[7:0]	—	—	I/O	EVDD	B7, A7, D6, C6, B6, A6, D5, C5	T3–4, U1–3, V1–2, W1
$\overline{\text{FB\_BE/BWE}}$[3:2]	PBE[3:2]	FB_TSIZ[1:0]	—	—	O	EVDD	B5, A5	Y1, W2
$\overline{\text{FB\_BE/BWE}}$[1:0]	PBE[1:0]	—	—	—	O	EVDD	B4, A4	W3, Y2
FB_CLK	—	—	—	—	O	EVDD	B13	J3
$\overline{\text{FB\_CS}}$[3:1]	PCS[3:1]	—	—	—	O	EVDD	C2, D4, C3	W5, AA4, AB3
$\overline{\text{FB\_CS0}}$	—	—	—	—	O	EVDD	C4	Y4
$\overline{\text{FB\_OE}}$	PFBCTL3	—	—	—	O	EVDD	A2	AA1
FB_R/$\overline{\text{W}}$	PFBCTL2	—	—	—	O	EVDD	B2	AA3
$\overline{\text{FB\_TA}}$	PFBCTL1	—	—	U	I	EVDD	B1	AB2

Table 4. MCF5445*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
FB_TS	PFBCTL0	FB_ALE	FB_TBST	—	O	EVDD	A3	Y3
PCI Controller[5]								
PCI_AD[31:0]	—	FB_A[31:0]	—	—	I/O	EVDD	—	C11, D11, A10, B10, J4, G2, G3, F1, D12, C12, B12, A11, B11, B9, D9, D10, A8, B8, A5, B5, A4, A3, B3, D4, D3, E3–E1, F3, C2, D2, C1
—	—	FB_A[23:0]	—	—	I/O	EVDD	K14–13, J15–13, H13–15, G15–13, F14–13, E15–13, D16, B16, C15, B15, C14, D15, C16, D14	—
PCI_CBE[3:0]	—	—	—	—	I/O	EVDD	—	G4, E4, D1, B1
PCI_DEVSEL	—	—	—	—	O	EVDD	—	F2
PCI_FRAME	—	—	—	—	I/O	EVDD	—	B2
PCI_GNT3	PPCI7	ATA_DMACK	—	—	O	EVDD	—	B7
PCI_GNT[2:1]	PPCI[6:5]	—	—	—	O	EVDD	—	C8, C9
PCI_GNT0/ PCI_EXTREQ	PPCI4	—	—	—	O	EVDD	—	A9
PCI_IDSEL	—	—	—	—	I	EVDD	—	D5
PCI_IRDY	—	—	—	—	I/O	EVDD	—	C3
PCI_PAR	—	—	—	—	I/O	EVDD	—	C4
PCI_PERR	—	—	—	—	I/O	EVDD	—	B4
PCI_REQ3	PPCI3	ATA_INTRQ	—	—	I	EVDD	—	C7
PCI_REQ[2:1]	PPCI[2:1]	—	—	—	I	EVDD	—	D7, C5
PCI_REQ0/ PCI_EXTGNT	PPCI0	—	—	—	I	EVDD	—	A2
PCI_RST	—	—	—	—	O	EVDD	—	B6
PCI_SERR	—	—	—	—	I/O	EVDD	—	A6
PCI_STOP	—	—	—	—	I/O	EVDD	—	A7
PCI_TRDY	—	—	—	—	I/O	EVDD	—	C10
SDRAM Controller								
SD_A[13:0]	—	—	—	—	O	SDVDD	R1, P1, N2, P2, R2, T2, M4, N3, P3, R3, T3, T4, R4, N4	V22, U20–22, T19–22, R20–22, N19, P20–21

Table 4. MCF5445*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
FEC0_TXCLK	PFEC0H7	FEC0_RMII_ REF_CLK	—	—	I	EVDD	H4	Y10
FEC0_TXD[3:2]	PFEC0L[7:6]	—	ULPI_DATA[3:2]	—	O	EVDD	J1, J2	W10, AB11
FEC0_TXD1	PFEC0L5	FEC0_RMII_TXD1	—	—	O	EVDD	J3	AA11
FEC0_TXD0	PFEC0H5	FEC0_RMII_TXD0	—	—	O	EVDD	J4	Y11
FEC0_TXEN	PFEC0H6	FEC0_RMII_TXEN	—	—	O	EVDD	K1	W11
FEC0_TXER	PFEC0L4	—	ULPI_DATA0	—	O	EVDD	K2	AB12
FEC1								
FEC1_MDC	PFECI2C5	—	$\overline{\text{ATA\_DIOR}}$	—	O	EVDD	—	W20
FEC1_MDIO	PFECI2C4	—	$\overline{\text{ATA\_DIOW}}$	—	I/O	EVDD	—	Y22
FEC1_COL	PFEC1H4	—	ATA_DATA7	—	I	EVDD	—	AB18
FEC1_CRS	PFEC1H0	—	ATA_DATA6	—	I	EVDD	—	AA18
FEC1_RXCLK	PFEC1H3	—	ATA_DATA5	—	I	EVDD	—	W14
FEC1_RXDV	PFEC1H2	FEC1_RMII_ CRS_DV	ATA_DATA15	—	I	EVDD	—	AB15
FEC1_RXD[3:2]	PFEC1L[3:2]	—	ATA_DATA[4:3]	—	I	EVDD	—	AA15, Y15
FEC1_RXD1	PFEC1L1	FEC1_RMII_RXD1	ATA_DATA14	—	I	EVDD	—	AA17
FEC1_RXD0	PFEC1H1	FEC1_RMII_RXD0	ATA_DATA13	—	I	EVDD	—	Y17
FEC1_RXER	PFEC1L0	FEC1_RMII_RXER	ATA_DATA12	—	I	EVDD	—	W17
FEC1_TXCLK	PFEC1H7	FEC1_RMII_ REF_CLK	ATA_DATA11	—	I	EVDD	—	AB19
FEC1_TXD[3:2]	PFEC1L[7:6]	—	ATA_DATA[2:1]	—	O	EVDD	—	Y19, W18
FEC1_TXD1	PFEC1L5	FEC1_RMII_TXD1	ATA_DATA10	—	O	EVDD	—	AA19
FEC1_TXD0	PFEC1H5	FEC1_RMII_TXD0	ATA_DATA9	—	O	EVDD	—	Y20
FEC1_TXEN	PFEC1H6	FEC1_RMII_TXEN	ATA_DATA8	—	O	EVDD	—	AA21
FEC1_TXER	PFEC1L4	—	ATA_DATA0	—	O	EVDD	—	AA22
USB On-the-Go								
USB_DM	—	—	—	—	O	USB VDD	F16	A14
USB_DP	—	—	—	—	O	USB VDD	E16	A15
USB_VBUS_EN	PUSB1	USB_PULLUP	ULPI_NXT	—	O	USB VDD	E5	AA2
USB_VBUS_OC	PUSB0	—	ULPI_STP	UD[7]	I	USB VDD	B3	V4

Table 4. MCF5445*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
DSPI_SIN	PDSPI1	SBF_DI	—	[8]	I	EVDD	P15	B19
DSPI_SOUT	PDSPI0	SBF_DO	—	—	O	EVDD	N13	C20
UARTs								
$\overline{\text{U1CTS}}$	PUART7	—	—	—	I	EVDD	—	V3
$\overline{\text{U1RTS}}$	PUART6	—	—	—	O	EVDD	—	U4
U1RXD	PUART5	—	—	—	I	EVDD	—	P3
U1TXD	PUART4	—	—	—	O	EVDD	—	N3
$\overline{\text{U0CTS}}$	PUART3	—	—	—	I	EVDD	M3	Y16
$\overline{\text{U0RTS}}$	PUART2	—	—	—	O	EVDD	M2	AA16
U0RXD	PUART1	—	—	—	I	EVDD	N1	AB16
U0TXD	PUART0	—	—	—	O	EVDD	M1	W15
Note: The UART1 and UART 2 signals are multiplexed on the DMA timers and I2C pins.								
DMA Timers								
DT3IN	PTIMER3	DT3OUT	U2RXD	—	I	EVDD	C13	H2
DT2IN	PTIMER2	DT2OUT	U2TXD	—	I	EVDD	D13	H1
DT1IN	PTIMER1	DT1OUT	$\overline{\text{U2CTS}}$	—	I	EVDD	B14	H3
DT0IN	PTIMER0	DT0OUT	$\overline{\text{U2RTS}}$	—	I	EVDD	A15	G1
BDM/JTAG[9]								
PSTDDATA[7:0]	—	—	—	—	O	EVDD	E2, D1, F4, E3, D2, C1, E4, D3	AA6, AB6, AB5, W6, Y6, AA5, AB4, Y5
JTAG_EN	—	—	—	D	I	EVDD	M11	C21
PSTCLK	—	TCLK	—	—	I	EVDD	P13	C22
DSI	—	TDI	—	U	I	EVDD	T15	C19
DSO	—	TDO	—	—	O	EVDD	T14	A21
$\overline{\text{BKPT}}$	—	TMS	—	U	I	EVDD	R14	B21
DSCLK	—	$\overline{\text{TRST}}$	—	U	I	EVDD	M13	B22
Test								
TEST	—	—	—	D	I	EVDD	M6	AB20
PLLTEST	—	—	—	—	O	EVDD	K16	D15

4.3 Pinout—360 TEPBGA

The pinout for the MCF54452, MCF54453, MCF54454, and MCF54455 packages are shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A		PCI_REQ0	PCI_AD10	PCI_AD11	PCI_AD13	PCI_SERR	PCI_STOP	PCI_AD15	PCI_GNT0	PCI_AD29	PCI_AD20	XTAL 32K	EXTAL 32K	USB_DM	USB_DP	EXTAL	XTAL	DACK0	DSPI_PCS2	DSPI_SCK	TDO		A
B	PCI_CBE0	PCI_FRAME	PCI_AD9	PCI_PERR	PCI_AD12	PCI_RST	PCI_GNT3	PCI_AD14	PCI_AD18	PCI_AD28	PCI_AD19	PCI_AD21	NC		NC	VDD_OSC	RSTOUT	DREQ0	DSPI_SIN	DSPI_PCS1	TMS	TRST	B
C	PCI_AD0	PCI_AD2	PCI_IRDY	PCI_PAR	PCI_REQ1	IRQ1	PCI_REQ3	PCI_GNT2	PCI_GNT1	PCI_TRDY	PCI_AD31	PCI_AD22	VDD_RTC	VDD_A_PLL	NC	VSS_OSC	DACK1	DREQ1	TDI	DSPI_SOUT	JTAG_EN	TCLK	C
D	PCI_CBE1	PCI_AD1	PCI_AD7	PCI_AD8	PCI_IDSEL	IVDD	PCI_REQ2	IVDD	PCI_AD17	PCI_AD16	PCI_AD30	PCI_AD23	EVDD	IVDD	PLL TEST	NC	DSPI_PCS0	DSPI_PCS5	EVDD	SSI_MCLK	SSI_RXD	SSI_TXD	D
E	PCI_AD4	PCI_AD5	PCI_AD6	PCI_CBE2															SSI_BCLK	SSI_FS	SD_DM2	SD_DQS2	E
F	PCI_AD24	PCI_DEVSEL	PCI_AD3	IVDD																SD_D16	SD_D17	SD_D18	F
G	T0IN	PCI_AD26	PCI_AD25	PCI_CBE3				EVDD			EVDD			EVDD		EVDD			SD_D19	SD_D20	SD_D21	SD_D22	G
H	T2IN	T3IN	T1IN	IVDD																SD_D23	SD_DM3	SD_DQS3	H
J	FB_AD29	FB_AD31	FB_CLK	PCI_AD27				EVDD								EVDD			SD_D26	SD_D27	SD_D25	SD_D24	J
K	FB_AD28	FB_AD27	FB_AD26	FB_AD30																SD_D28	SD_D29	SD_D30	K
L	FB_AD25	FB_AD23	FB_AD22	FB_AD24				EVDD								EVDD			SD_CAS	SD_CS1	SD_D31	SD_CLK	L
M	FB_AD21	FB_AD20	FB_AD19	FB_AD18																SD_CS0	SD_VREF	SD_CLK	M
N	FB_AD17	FB_AD16	U1TXD	IVDD												EVDD			SD_A2	SD_WE	SD_RAS	SD_CKE	N
P	FB_AD15	FB_AD14	U1RXD	FB_AD10				EVDD											SD_BA0	SD_A1	SD_A0	SD_BA1	P
R	FB_AD13	FB_AD12	FB_AD11	IVDD												EVDD				SD_A5	SD_A4	SD_A3	R
T	FB_AD9	FB_AD8	FB_AD7	FB_AD6				EVDD			EVDD			EVDD		EVDD			SD_A9	SD_A8	SD_A7	SD_A6	T
U	FB_AD5	FB_AD4	FB_AD3	U1RTS																SD_A12	SD_A11	SD_A10	U
V	FB_AD2	FB_AD1	U1CTS	USB_VBUS_OC															ATA_DA2	ATA_DA1	ATA_DA0	SD_A13	V
W	FB_AD0	FB_BE/BWE2	FB_BE/BWE1	IVDD	FB_CS3	PST DDATA4	IVDD	IVDD	FEC0_RXD1	FEC0_TXD3	FEC0_TXEN	IVDD	ATA_RESET	FEC1_RXCLK	U0TXD	IVDD	FEC1_RXER	FEC1_TXD2	IVDD	FEC1_MDC	ATA_CS1	ATA_CS0	W
Y	FB_BE/BWE3	FB_BE/BWE0	FB_TS	FB_CS0	PST DDATA0	PST DDATA3	FEC0_MDIO	FEC0_RXDV	FEC0_RXD2	FEC0_TXCLK	FEC0_TXD0	I2C_SDA	ATA_BUFFER_EN	ATA_IORDY	FEC1_RXD2	U0CTS	FEC1_RXD0	RESET	FEC1_TXD3	FEC1_TXD0	NC	FEC1_MDIO	Y
AA	FB_OE	USB_VBUS_EN	FB_R/W	FB_CS2	PST DDATA2	PST DDATA7	FEC0_CRS	FEC0_RXCLK	NC	FEC0_RXER	FEC0_TXD1	I2C_SCL	IRQ4	ATA_DMARQ	FEC1_RXD3	U0RTS	FEC1_RXD1	FEC1_CRS	FEC1_TXD1	NC	FEC1_TXEN	FEC1_TXER	AA
AB		FB_TA	FB_CS1	PST DDATA1	PST DDATA5	PST DDATA6	FEC0_COL	FEC0_MDC	FEC0_RXD3	FEC0_RXD0	FEC0_TXD2	FEC0_TXER	IRQ7	IRQ3	FEC1_RXDV	U0RXD	BOOT MOD1	FEC1_COL	FEC1_TXCLK	TEST	BOOT MOD0		AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure 6. MCF54452, MCF54453, MCF54454, and MCF54455 Pinout (360 TEPBGA)

5 Electrical Characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF54455 microprocessor. This section contains detailed information on DC/AC electrical characteristics and AC timing specifications.

The electrical specifications are preliminary and from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. However, for production silicon, these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this MCU document supersede any values found in the module specifications.

5.1 Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Pin Name	Value	Units
External I/O pad supply voltage	EV_{DD}	EVDD	-0.3 to +4.0	V
Internal oscillator supply voltage	$OSCV_{DD}$	VDD_OSC	-0.3 to +4.0	V
Real-time clock supply voltage	$RTCV_{DD}$	VDD_RTC	-0.5 to +2.0	V
Internal logic supply voltage	IV_{DD}	IVDD	-0.5 to +2.0	V
SDRAM I/O pad supply voltage	SDV_{DD}	SD_VDD	-0.3 to +4.0	V
PLL supply voltage	PV_{DD}	VDD_A_PLL	-0.5 to +2.0	V
Digital input voltage[3]	V_{IN}	—	-0.3 to +3.6	V
Instantaneous maximum current Single pin limit (applies to all pins) [3, 4, 5]	I_{DD}	—	25	mA
Operating temperature range (packaged)	T_A (T_L - T_H)	—	-40 to +85	°C
Storage temperature range	T_{stg}	—	-55 to +150	°C

1 Functional operating conditions are given in Table 8. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., V_{SS} or EV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, and then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and EV_{DD}.

5 Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > EV_{DD}) is greater than I_{DD}, the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Ensure the external EV_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MPU is not consuming power (ex; no clock). The power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

5.2 Thermal Characteristics

Table 6. Thermal Characteristics

Characteristic		Symbol	256 MAPBGA	360 TEPBGA	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	29[1,2]	24[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	25[1,2]	21[1,2]	°C/W
Junction to board		θ_{JB}	18[3]	15[3]	°C/W
Junction to case		θ_{JC}	10[4]	11[4]	°C/W
Junction to top of package		Ψ_{jt}	2[1,5]	2[1,5]	°C/W
Maximum operating junction temperature		T_j	105	105	°C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C
Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = P_{INT} + $P_{I/O}$
P_{INT} = $I_{DD} \times IV_{DD}$, Watts - Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273°C)} \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

5.3 ESD Protection

Table 7. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 8. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Units
Internal logic supply voltage[1]	IV_{DD}	1.35	1.65	V
PLL analog operation voltage range [1]	PV_{DD}	1.35	1.65	V
External I/O pad supply voltage	EV_{DD}	3.0	3.6	V
Internal oscillator supply voltage	$OSCV_{DD}$	3.0	3.6	V
Real-time clock supply voltage	$RTCV_{DD}$	1.35	1.65	V
SDRAM I/O pad supply voltage — DDR mode	SDV_{DD}	2.25	2.75	V
SDRAM I/O pad supply voltage — DDR2 mode	SDV_{DD}	1.7	1.9	V
SDRAM I/O pad supply voltage — Mobile DDR mode	SDV_{DD}	1.7	1.9	V
SDRAM input reference voltage	SDV_{REF}	0.49 x SDV_{DD}	0.51 x SDV_{DD}	V
Input High Voltage	V_{IH}	0.7 x EV_{DD}	3.65	V
Input Low Voltage	V_{IL}	V_{SS} – 0.3	0.35 x EV_{DD}	V
Input Hysteresis	V_{HYS}	0.06 x EV_{DD}	—	mV
Input Leakage Current[2] V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–2.5	2.5	µA
Input Leakage Current[3] V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–5	5	µA
High Impedance (Off-State) Leakage Current[4] V_{in} = V_{DD} or V_{SS}, All input/output and output pins	I_{OZ}	–10.0	10.0	µA
Output High Voltage (All input/output and all output pins) I_{OH} = –5.0 mA	V_{OH}	0.85 × EV_{DD}	—	V
Output Low Voltage (All input/output and all output pins) I_{OL} = 5.0mA	V_{OL}	—	0.15 × EV_{DD}	V

Table 9. Input Clock Timing Requirements

Item	Specification	Min	Max	Unit
C1	Cycle time	15	40	ns
1 / C1	Frequency	25	66.66	MHz
C2	Rise time (20% of vdd to 80% of vdd)	-	2	ns
C3	Fall time (80% of vdd to 20% of vdd)	-	2	ns
C4	Duty cycle (at 50% of vdd)	40	60	%

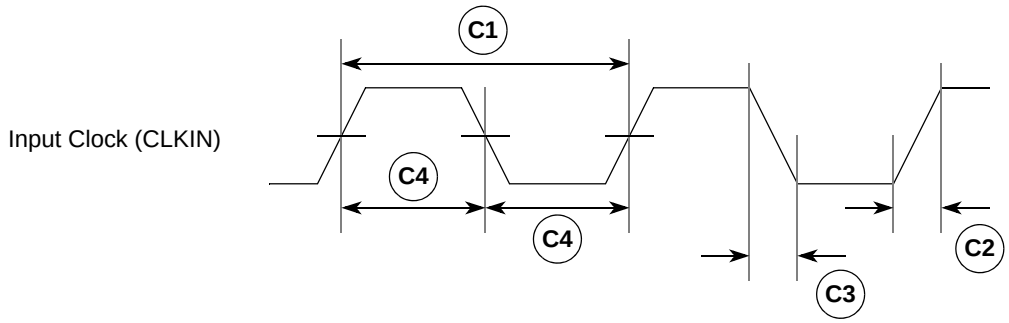


Figure 7. Input Clock Timing Diagram

Table 10. PLL Electrical Characteristics

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	PLL Reference Frequency Range Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 16 16	 40 66.66	 MHz MHz
2	Core/System Frequency	f_{sys}	512 Hz[1]	266.67 MHz	—
	Core/System Clock Period	t_{sys}	—	$1/f_{sys}$	ns
19	VCO Frequency ($f_{vco} = f_{ref} \times PFDR$)	f_{vco}	300	540	MHz
3	Crystal Start-up Time[2, 3]	t_{cst}	—	10	ms
4	EXTAL Input High Voltage Crystal Mode[4] All other modes (External, Limp)	 V_{IHEXT} V_{IHEXT}	 V_{XTAL} + 0.4 $E_{VDD}/2$ + 0.4	 — —	 V V
5	EXTAL Input Low Voltage Crystal Mode[4] All other modes (External, Limp)	 V_{ILEXT} V_{ILEXT}	 — —	 V_{XTAL} - 0.4 $E_{VDD}/2$ - 0.4	 V V
6	EXTAL Input Rise & Fall Time (20% to 80% E_{VDD}) (External, Limp)		1	2	ns
7	PLL Lock Time [3, 5]	t_{lpll}	—	50000	CLKIN
8	Duty Cycle of reference [3] (External, Limp)	t_{dc}	40	60	%
9	XTAL Current	I_{XTAL}	1	3	mA
10	Total on-chip stray capacitance on XTAL	C_{S_XTAL}	—	1.5	pF

5.8 SDRAM AC Timing Characteristics

The following timing numbers must be followed to properly latch or drive data onto the SDRAM memory bus. All timing numbers are relative to the four DQS byte lanes.

Table 13. SDRAM Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of Operation		60	133.33	MHz	1
DD1	Clock Period	t_{SDCK}	7.5	16.67	ns	
DD2	Pulse Width High	t_{SDCKH}	0.45	0.55	t_{SDCK}	2
DD3	Pulse Width Low	t_{SDCKL}	0.45	0.55	t_{SDCK}	3
DD4	Address, SD_CKE, $\overline{SD\_CAS}$, $\overline{SD\_RAS}$, $\overline{SD\_WE}$, $\overline{SD\_CS}$[1:0] — Output Valid	t_{CMV}	—	(0.5 x t_{SDCK}) + 1.0ns	ns	3
DD5	Address, SD_CKE, $\overline{SD\_CAS}$, $\overline{SD\_RAS}$, $\overline{SD\_WE}$, $\overline{SD\_CS}$[1:0] — Output Hold	t_{CMH}	2.0	—	ns	
DD6	Write Command to first DQS Latching Transition	t_{DQSS}	(1.0 x t_{SDCK}) - 0.6ns	(1.0 x t_{SDCK}) + 0.6ns	ns	
DD7	Data and Data Mask Output Setup (DQ-->DQS) Relative to DQS (DDR Write Mode)	t_{QS}	1.0	—	ns	4 5
DD8	Data and Data Mask Output Hold (DQS-->DQ) Relative to DQS (DDR Write Mode)	t_{QH}	1.0	—	ns	6
DD9	Input Data Skew Relative to DQS (Input Setup)	t_{IS}	—	1.0	ns	7
DD10	Input Data Hold Relative to DQS.	t_{IH}	(0.25 x t_{SDCK}) + 0.5ns	—	ns	8

1 The SDRAM interface operates at the same frequency as the internal system bus.

2 Pulse width high plus pulse width low cannot exceed min and max clock period.

3 Command output valid should be 1/2 the memory bus clock (t_{SDCK}) plus some minor adjustments for process, temperature, and voltage variations.

4 This specification relates to the required input setup time of DDR memories. The microprocessor's output setup should be larger than the input setup of the DDR memories. If it is not larger, then the input setup on the memory is in violation.
SD_D[31:24] is relative to SD_DQS[3]; SD_D[23:16] is relative to SD_DQS[2]

5 The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.

6 This specification relates to the required hold time of DDR memories.
SD_D[31:24] is relative to SD_DQS[3]; SD_D[23:16] is relative to SD_DQS[2]

7 Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

8 Data input hold is derived from each DQS clock edge. It begins with a DQS transition and ends when the first data line becomes invalid.

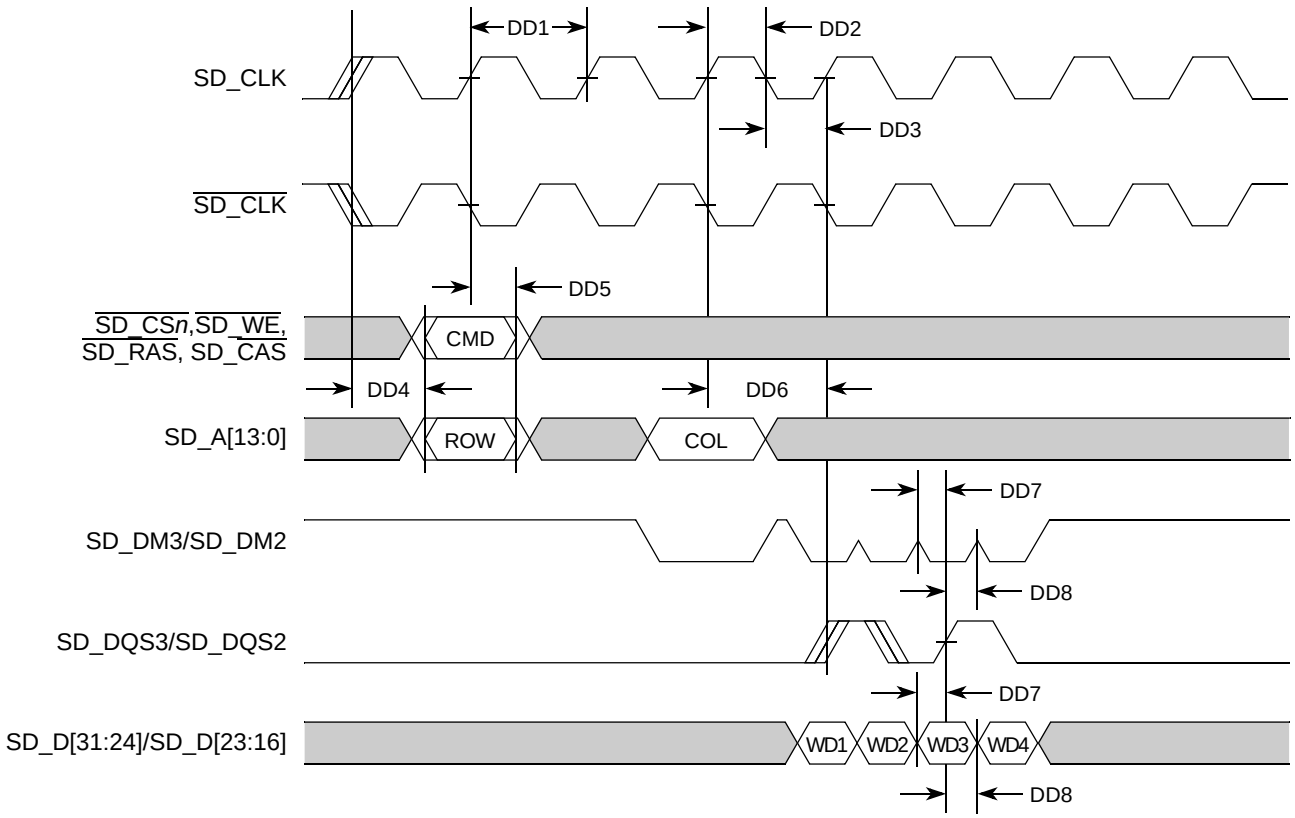


Figure 11. DDR Write Timing

Table 19. I²C Output Timing Specifications between SCL and SDA (continued)

Num	Characteristic	Min	Max	Units
I6[1]	Clock high time	10	—	t_{SYS}
I7[1]	Data setup time	2	—	t_{SYS}
I8[1]	Start condition setup time (for repeated start condition only)	20	—	t_{SYS}
I9[1]	Stop condition setup time	10	—	t_{SYS}

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 19. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR. However, the numbers given in Table 19 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

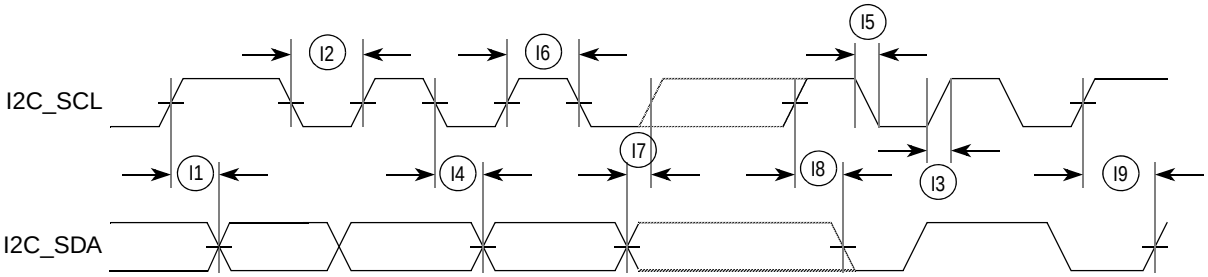


Figure 18. I²C Input/Output Timings

5.13 Fast Ethernet Timing Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

5.13.1 Receive Signal Timing Specifications

The following timing specs meet the requirements for MII and 7-Wire style interfaces for a range of transceiver devices.

Table 20. Receive Signal Timing

Num	Characteristic	MII Mode		RMII Mode		Unit
		Min	Max	Min	Max	
—	RXCLK frequency	—	25	—	50	MHz
E1	RXD[n:0], RXDV, RXER to RXCLK setup[1]	5	—	4	—	ns
E2	RXCLK to RXD[n:0], RXDV, RXER hold[1]	5	—	2	—	ns
E3	RXCLK pulse width high	35%	65%	35%	65%	RXCLK period
E4	RXCLK pulse width low	35%	65%	35%	65%	RXCLK period

1 In MII mode, n = 3; In RMII mode, n = 1

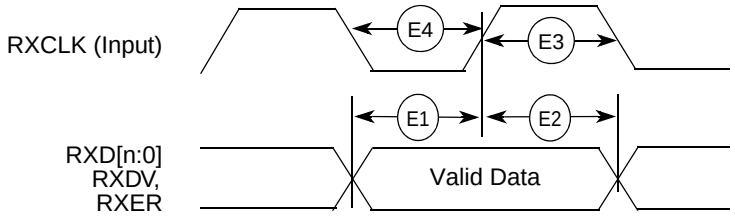


Figure 19. MII Receive Signal Timing Diagram

5.13.2 Transmit Signal Timing Specifications

Table 21. Transmit Signal Timing

Num	Characteristic	MII Mode		RMII Mode		Unit
		Min	Max	Min	Max	
—	TXCLK frequency	—	25	—	50	MHz
E5	TXCLK to TXD[n:0], TXEN, TXER invalid[1]	5	—	5	—	ns
E6	TXCLK to TXD[n:0], TXEN, TXER valid[1]	—	25	—	14	ns
E7	TXCLK pulse width high	35%	65%	35%	65%	t_{TXCLK}
E8	TXCLK pulse width low	35%	65%	35%	65%	t_{TXCLK}

1 In MII mode, n = 3; In RMII mode, n = 1

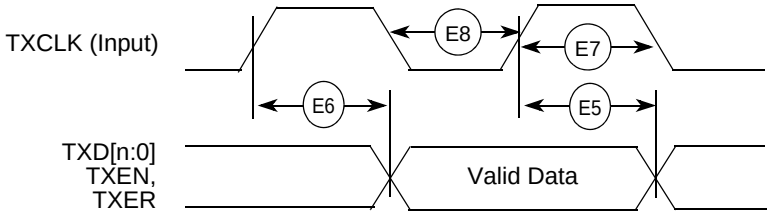


Figure 20. MII Transmit Signal Timing Diagram

5.13.3 Asynchronous Input Signal Timing Specifications

Table 22. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
E9	CRS, COL minimum pulse width	1.5	—	TXCLK period

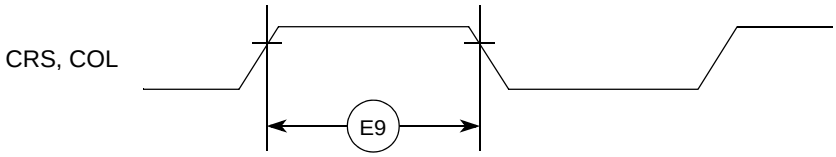


Figure 21. MII Async Inputs Timing Diagram

5.13.4 MII Serial Management Timing Specifications

Table 23. MII Serial Management Channel Signal Timing

Num	Characteristic	Symbol	Min	Max	Unit
E10	MDC cycle time	t_{MDC}	400	—	ns
E11	MDC pulse width		40	60	% t_{MDC}
E12	MDC to MDIO output valid		—	375	ns
E13	MDC to MDIO output invalid		25	—	ns
E14	MDIO input to MDC setup		10	—	ns
E15	MDIO input to MDC hold		0	—	ns

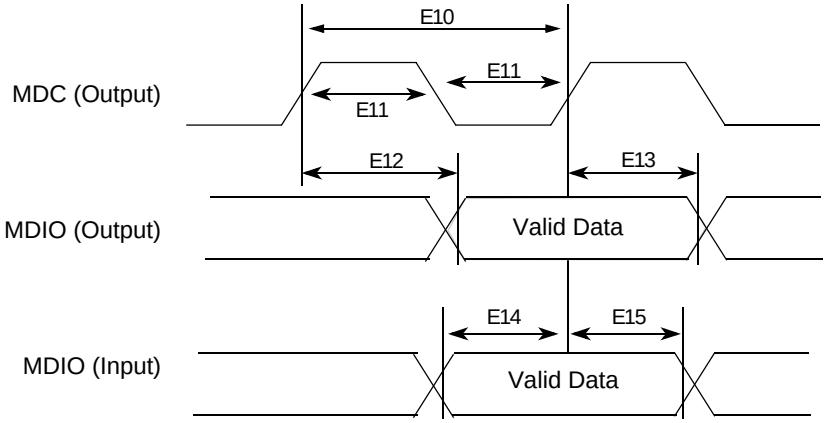


Figure 22. MII Serial Management Channel TIming Diagram

5.14 32-Bit Timer Module Timing Specifications

Table 24 lists timer module AC timings.

Table 24. Timer Module AC Timing Specifications

Name	Characteristic	Min	Max	Unit
T1	DT*n*IN cycle time (*n* = 0:3)	3	—	$t_{sys/2}$
T2	DT*n*IN pulse width (*n* = 0:3)	1	—	$t_{sys/2}$

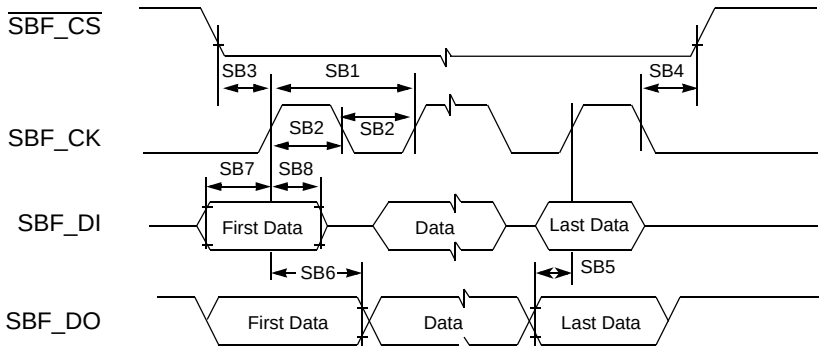


Figure 25. SBF Timing

5.18 General Purpose I/O Timing Specifications

Table 28. GPIO Timing[1]

Num	Characteristic	Min	Max	Unit
G1	FB_CLK High to GPIO Output Valid	—	9	ns
G2	FB_CLK High to GPIO Output Invalid	1.5	—	ns
G3	GPIO Input Valid to FB_CLK High	9	—	ns
G4	FB_CLK High to GPIO Input Invalid	1.5	—	ns

1 These general purpose specifications apply to the following signals: $\overline{\text{IRQ}}n$, all UART signals, all timer signals, $\overline{\text{DACK}}n$ and $\overline{\text{DREQ}}n$, and all signals configured as GPIO.

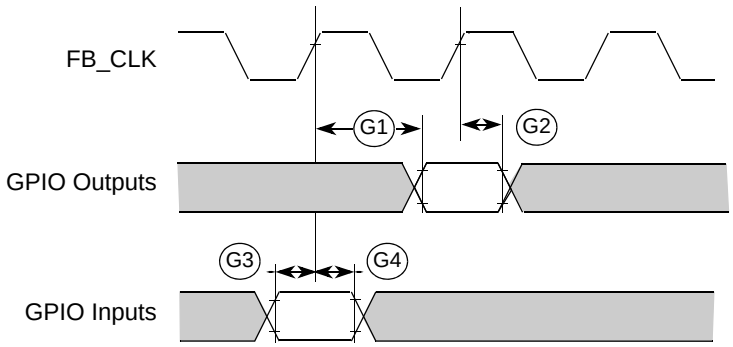


Figure 26. GPIO Timing

5.20 Debug AC Timing Specifications

Table 30 lists specifications for the debug AC timing parameters shown in Figure 31 and Table 32.

Table 30. Debug AC Timing Specification

Num	Characteristic	Min	Max	Units
D0	PSTCLK cycle time	1	1	t_{SYS}
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	1.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4[1]	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

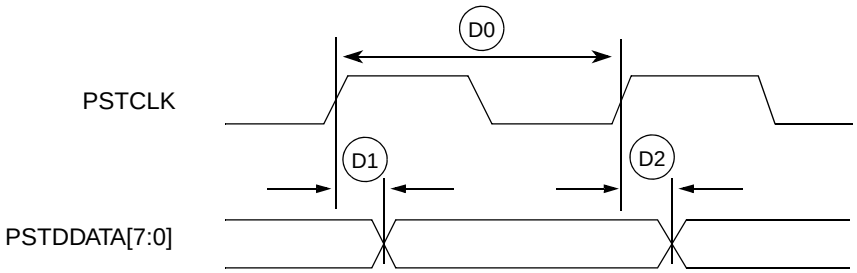


Figure 31. Real-Time Trace AC Timing

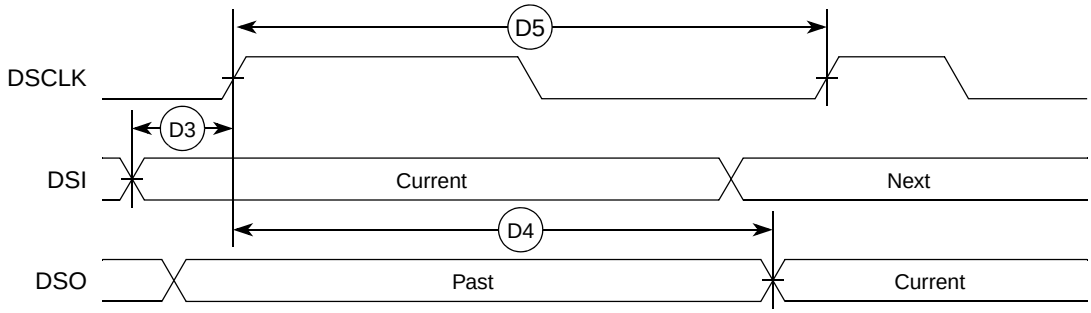


Figure 32. BDM Serial Port AC Timing

6 Power Consumption

All power consumption data is lab data measured on an M54455EVB running the Freescale Linux BSP.

Table 31. MCF4455 Application Power Consumption[1]

Core Freq.		Idle	MP3 Playback	TFTP Download	USB HS File Copy	Units
266 MHz	IV_{DD}	215.6	288.8	274.4	263.7	mA
	EV_{DD}	27.6	33.6	32.6	32.4	
	SDV_{DD}	142.9	158.2	161.1	158.0	
	Total Power	**672**	**829**	**809**	**787**	**mW**
200 MHz	IV_{DD}	163.8	228.0	213.8	207.9	mA
	EV_{DD}	29.9	34.7	34.3	33.8	
	SDV_{DD}	142.2	158.5	160.0	153.4	
	Total Power	**601**	**742**	**722**	**699**	**mW**

1 All voltage rails at nominal values: IV_{DD} = 1.5 V, EV_{DD} = 3.3 V, and SDV_{DD} = 1.8 V.

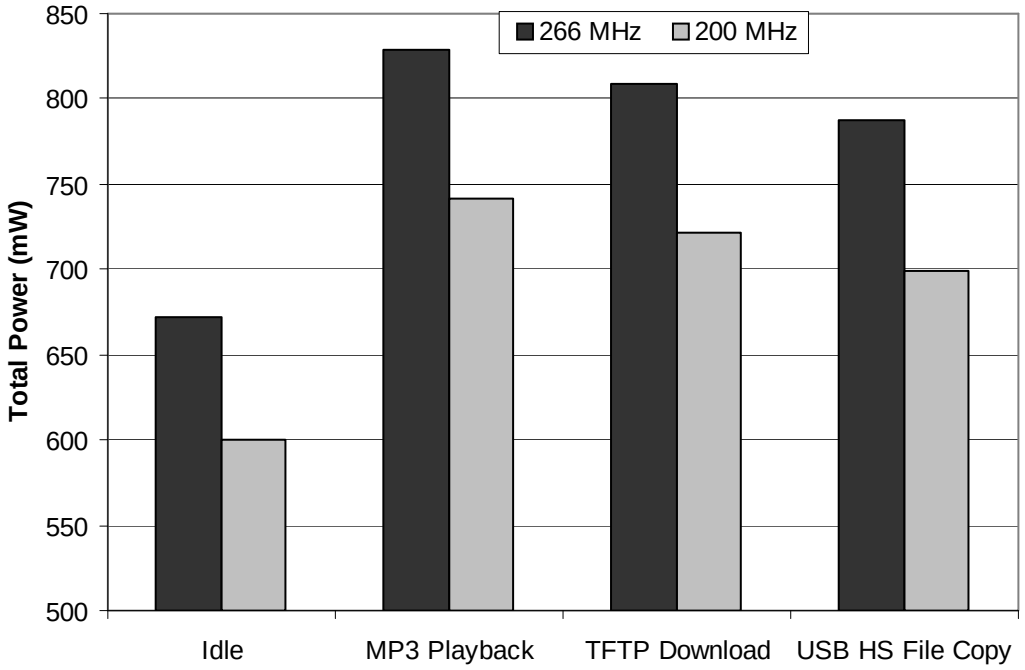


Figure 33. Power Consumption in Various Applications

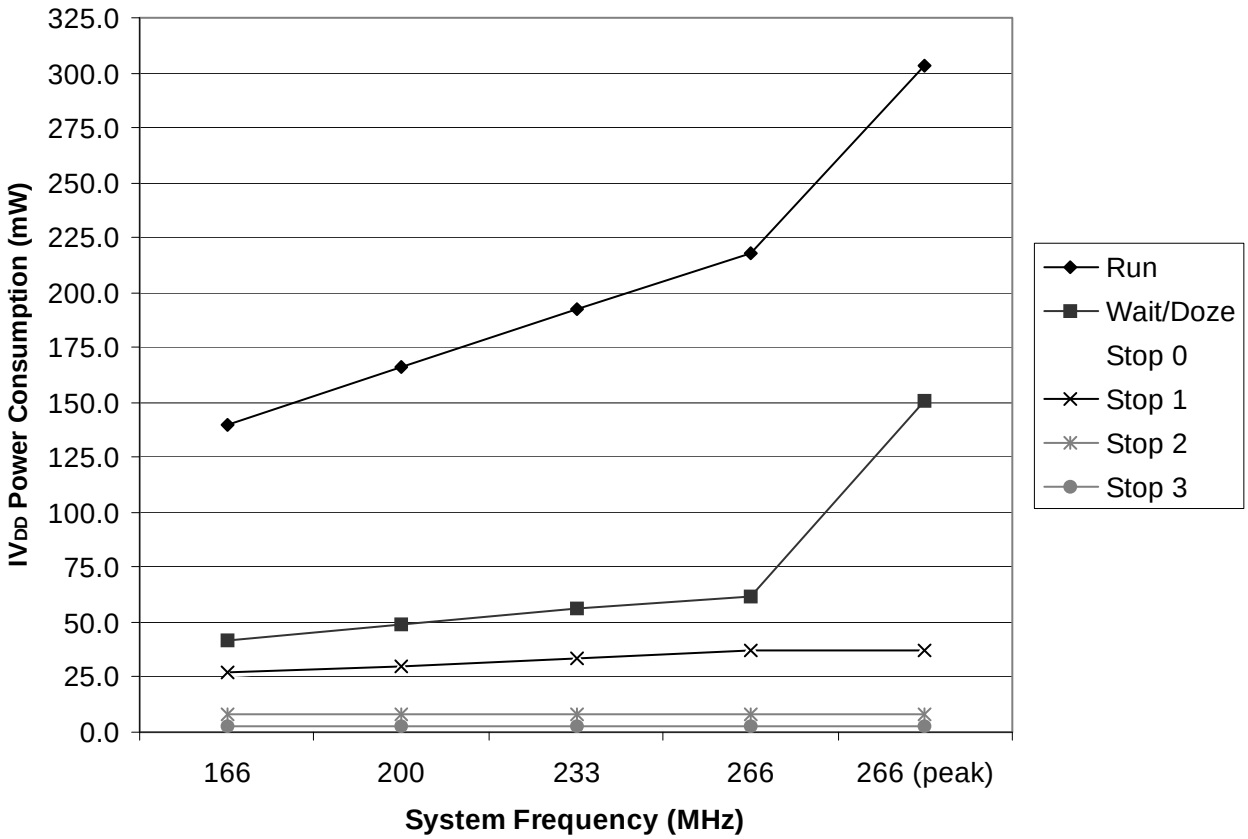


Figure 34. IV_{DD} Power Consumption in Low-Power Modes

7 Package Information

The latest package outline drawings are available on the product summary pages on http://www.freescale.com/coldfire. Table 33 lists the case outline numbers per device. Use these numbers in the web page's keyword search engine to find the latest package outline drawings.

Table 33. Package Information

Device	Package Type	Case Outline Numbers
MCF54450	256 MAPBGA	98ARH98219A
MCF54451		
MCF54452	360 TEPBGA	98ARE10605D
MCF54453		
MCF54454		
MCF54455		

8 Product Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com/coldfire.