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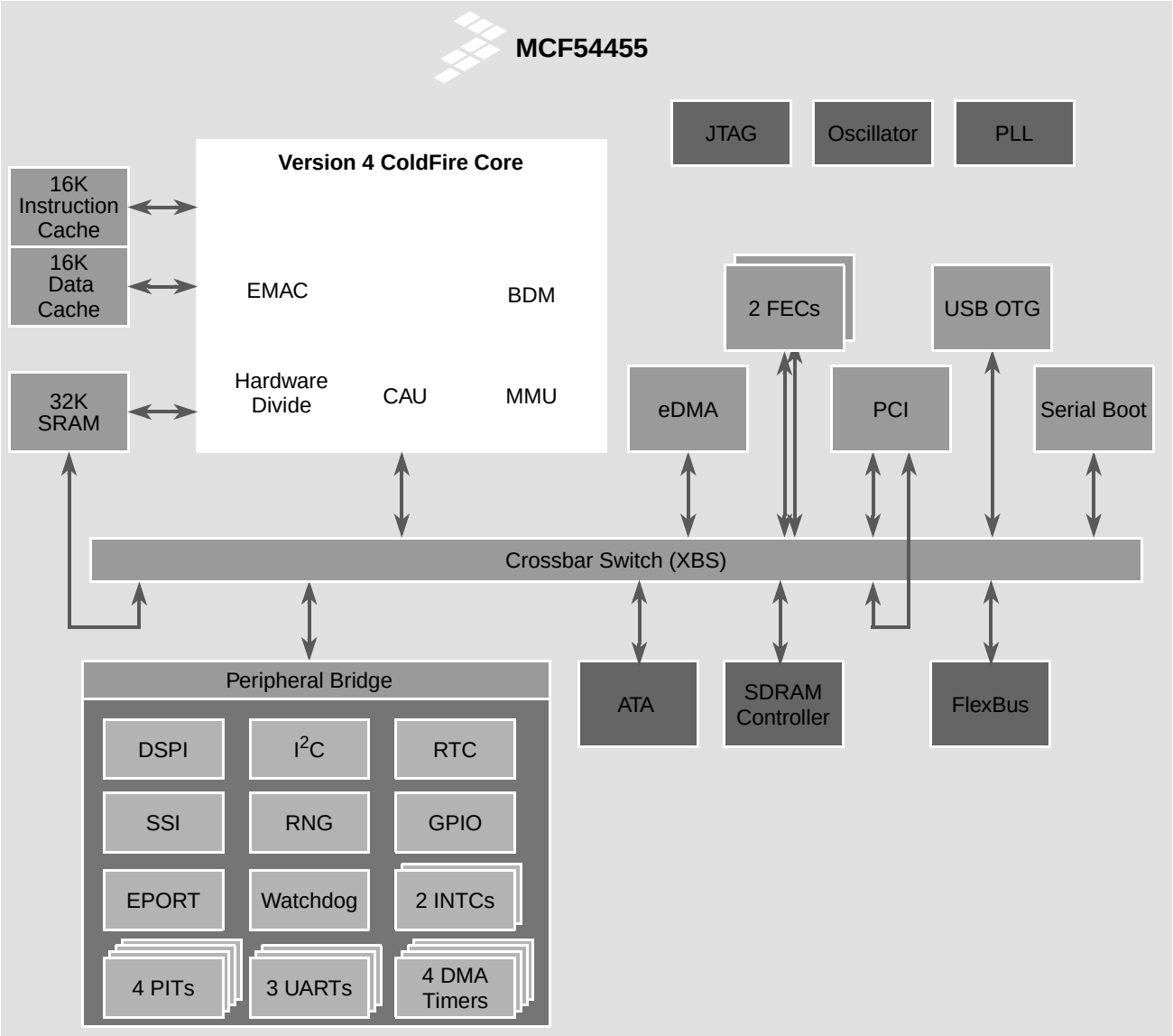
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V4
Core Size	32-Bit Single-Core
Speed	266MHz
Connectivity	I²C, SPI, SSI, UART/USART, USB OTG
Peripherals	DMA, WDT
Number of I/O	132
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	360-BBGA
Supplier Device Package	360-TEPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf54455vr266



LEGEND

ATA	– Advanced Technology Attachment Controller	**INTC**	– Interrupt controller
BDM	– Background debug module	**JTAG**	– Joint Test Action Group interface
CAU	– Cryptography acceleration unit	**MMU**	– Memory management unit
DSPI	– DMA serial peripheral interface	**PCI**	– Peripheral Component Interconnect
eDMA	– Enhanced direct memory access	**PIT**	– Programmable interrupt timers
EMAC	– Enchance multiply-accumulate unit	**PLL**	– Phase locked loop module
EPORT	– Edge port module	**RNG**	– Random Number Generator
FEC	– Fast Ethernet controller	**RTC**	– Real time clock
GPIO	– General Purpose Input/Output	**SSI**	– Synchronous Serial Interface
I^{2}C	– Inter-Intergrated Circuit	**USB OTG**	– Universal Serial Bus On-the-Go controller

Figure 1. MCF54455 Block Diagram

1 MCF5445*x* Family Comparison

The following table compares the various device derivatives available within the MCF5445*x* family.

Table 1. MCF5445*x* Family Configurations

Module	MCF54450	MCF54451	MCF54452	MCF54453	MCF54454	MCF54455
ColdFire Version 4 Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•	•	•	•	•
Core (System) Clock	up to 240 MHz		up to 266 MHz			
Peripheral Bus Clock (Core clock ÷ 2)	up to 120 MHz		up to 133 MHz			
External Bus Clock (Core clock ÷ 4)	up to 60 MHz		up to 66 MHz			
Performance (Dhrystone/2.1 MIPS)	up to 370		up to 410			
Independent Data/Instruction Cache	16 Kbytes each					
Static RAM (SRAM)	32 Kbytes					
PCI Controller	—	—	•	•	•	•
Cryptography Acceleration Unit (CAU)	—	•	—	•	—	•
ATA Controller	—	—	—	—	•	•
DDR SDRAM Controller	•	•	•	•	•	•
FlexBus External Interface	•	•	•	•	•	•
USB 2.0 On-the-Go	•	•	•	•	•	•
UTMI+ Low Pin Interface (ULPI)	•	•	•	•	•	•
Synchronous Serial Interface (SSI)	•	•	•	•	•	•
Fast Ethernet Controller (FEC)	1	1	2	2	2	2
UARTs	3	3	3	3	3	3
I^2C	•	•	•	•	•	•
DSPI	•	•	•	•	•	•
Real Time Clock	•	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4	4
Watchdog Timer (WDT)	•	•	•	•	•	•
Periodic Interrupt Timers (PIT)	4	4	4	4	4	4
Edge Port Module (EPORT)	•	•	•	•	•	•
Interrupt Controllers (INTC)	2	2	2	2	2	2
16-channel Direct Memory Access (DMA)	•	•	•	•	•	•
General Purpose I/O (GPIO)	•	•	•	•	•	•
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•	•	•
Package	256 MAPBGA		360 TEPBGA			

3.2 Oscillator Power Filtering

Figure 3 shows an example for isolating the oscillator power supply from the I/O supply (EVDD) and ground.

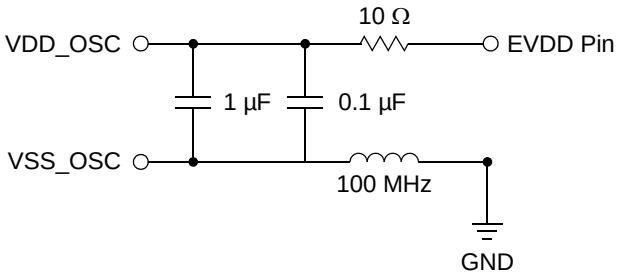
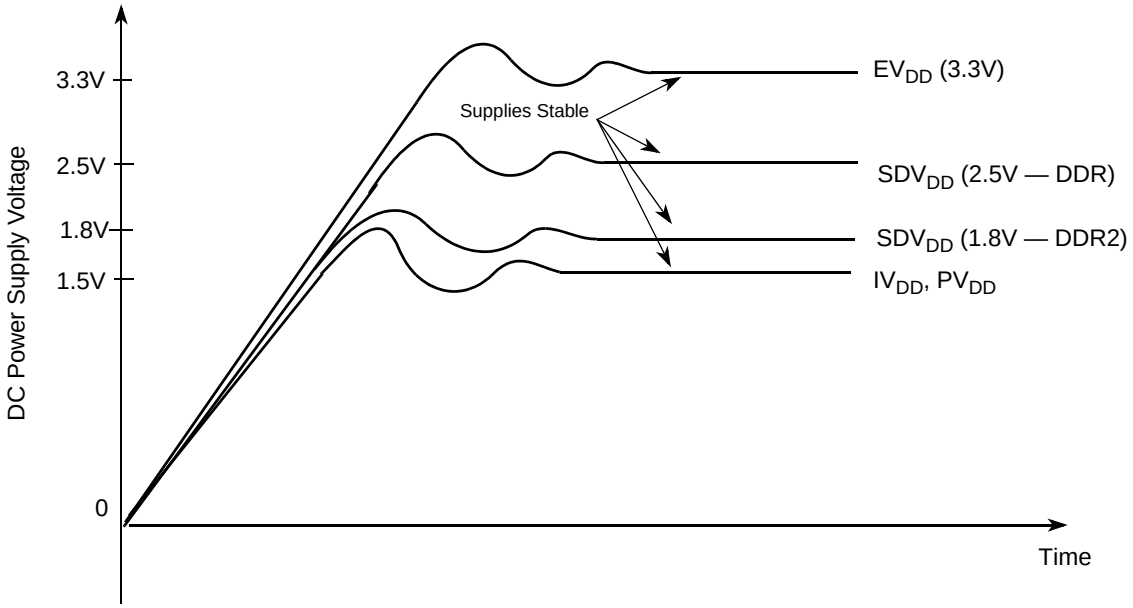


Figure 3. Oscillator Power Filter

3.3 Supply Voltage Sequencing

Figure 4 shows situations in sequencing the I/O V_{DD} (EV_{DD}), SDRAM V_{DD} (SDV_{DD}), PLL V_{DD} (PV_{DD}), and internal logic/core V_{DD} (IV_{DD}).



Notes:
1. Input voltage must not be greater than the supply voltage (EV_{DD}, SDV_{DD}, IV_{DD}, or PV_{DD}) by more than 0.5V at any time, including during power-up.
2. Use 50 V/millisecond or slower rise time for all supplies.

Figure 4. Supply Voltage Sequencing and Separation Cautions

The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. SDV_{DD} (2.5V or 1.8V) and EV_{DD} are specified relative to IV_{DD}.

Table 3. Special-Case Default Signal Functionality (continued)

Pin	256 MAPBGA	360 TEPBGA
$\overline{\text{PCI\_GNT}}$[3:0]	GPIO	$\overline{\text{PCI\_GNT}}$[3:0]
$\overline{\text{PCI\_REQ}}$[3:0]	GPIO	$\overline{\text{PCI\_REQ}}$[3:0]
$\overline{\text{IRQ1}}$	GPIO	$\overline{\text{PCI\_INTA}}$ and configured as an agent.
ATA_RESET	GPIO	ATA reset

Table 4. MCF5445*x* Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
Reset								
$\overline{\text{RESET}}$	—	—	—	U	I	EVDD	L4	Y18
$\overline{\text{RSTOUT}}$	—	—	—	—	O	EVDD	M15	B17
Clock								
EXTAL/PCI_CLK	—	—	—	—	I	EVDD	M16	A16
XTAL	—	—	—	U[3]	O	EVDD	L16	A17
Mode Selection								
BOOTMOD[1:0]	—	—	—	—	I	EVDD	M5, M7	AB17, AB21
FlexBus								
FB_AD[31:24]	PFBADH[7:0][4]	FB_D[31:24]	—	—	I/O	EVDD	A14, A13, D12, C12, B12, A12, D11, C11	J2, K4, J1, K1–3, L1, L4
FB_AD[23:16]	PFBADMH[7:0][4]	FB_D[23:16]	—	—	I/O	EVDD	B11, A11, D10, C10, B10, A10, D9, C9	L2, L3, M1–4, N1–2
FB_AD[15:8]	PFBADML[7:0][4]	FB_D[15:8]	—	—	I/O	EVDD	B9, A9, D8, C8, B8, A8, D7, C7	P1–2, R1–3, P4, T1–2
FB_AD[7:0]	PFBADL[7:0][4]	FB_D[7:0]	—	—	I/O	EVDD	B7, A7, D6, C6, B6, A6, D5, C5	T3–4, U1–3, V1–2, W1
$\overline{\text{FB\_BE/BWE}}$[3:2]	PBE[3:2]	FB_TSIZ[1:0]	—	—	O	EVDD	B5, A5	Y1, W2
$\overline{\text{FB\_BE/BWE}}$[1:0]	PBE[1:0]	—	—	—	O	EVDD	B4, A4	W3, Y2
FB_CLK	—	—	—	—	O	EVDD	B13	J3
$\overline{\text{FB\_CS}}$[3:1]	PCS[3:1]	—	—	—	O	EVDD	C2, D4, C3	W5, AA4, AB3
$\overline{\text{FB\_CS0}}$	—	—	—	—	O	EVDD	C4	Y4
$\overline{\text{FB\_OE}}$	PFBCTL3	—	—	—	O	EVDD	A2	AA1
FB_R/$\overline{\text{W}}$	PFBCTL2	—	—	—	O	EVDD	B2	AA3
$\overline{\text{FB\_TA}}$	PFBCTL1	—	—	U	I	EVDD	B1	AB2

Table 4. MCF5445*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
SD_BA[1:0]	—	—	—	—	O	SDVDD	P4, T5	P22, P19
$\overline{\text{SD\_CAS}}$	—	—	—	—	O	SDVDD	T6	L19
SD_CKE	—	—	—	—	O	SDVDD	N5	N22
SD_CLK	—	—	—	—	O	SDVDD	T9	L22
$\overline{\text{SD\_CLK}}$	—	—	—	—	O	SDVDD	T8	M22
$\overline{\text{SD\_CS}}$[1:0]	—	—	—	—	O	SDVDD	P6, R6	L20, M20
SD_D[31:16]	—	—	—	—	I/O	SDVDD	N6, T7, N7, P7, R7, R8, P8, N8, N9, T10, R10, P10, N10, T11, R11, P11	L21, K22, K21, K20, J20, J19, J21, J22, H20, G22, G21, G20, G19, F22, F21, F20
SD_DM[3:2]	—	—	—	—	O	SDVDD	P9, N12	H21, E21
SD_DQS[3:2]	—	—	—	—	O	SDVDD	R9, N11	H22, E22
$\overline{\text{SD\_RAS}}$	—	—	—	—	O	SDVDD	P5	N21
SD_VREF	—	—	—	—	I	SDVDD	M8	M21
$\overline{\text{SD\_WE}}$	—	—	—	—	O	SDVDD	R5	N20
External Interrupts Port[6]								
$\overline{\text{IRQ7}}$	PIRQ7	—	—	—	I	EVDD	L1	ABB13
$\overline{\text{IRQ4}}$	PIRQ4	—	SSI_CLKIN	—	I	EVDD	L2	ABB13
$\overline{\text{IRQ3}}$	PIRQ3	—	—	—	I	EVDD	L3	AB14
$\overline{\text{IRQ1}}$	PIRQ1	$\overline{\text{PCI\_INTA}}$	—	—	I	EVDD	F15	C6
FEC0								
FEC0_MDC	PFECI2C3	—	—	—	O	EVDD	F3	AB8
FEC0_MDIO	PFECI2C2	—	—	—	I/O	EVDD	F2	Y7
FEC0_COL	PFEC0H4	—	ULPI_DATA7	—	I	EVDD	E1	AB7
FEC0_CRS	PFEC0H0	—	ULPI_DATA6	—	I	EVDD	F1	AA7
FEC0_RXCLK	PFEC0H3	—	ULPI_DATA1	—	I	EVDD	G1	AA8
FEC0_RXDV	PFEC0H2	FEC0_RMII_ CRS_DV	—	—	I	EVDD	G2	Y8
FEC0_RXD[3:2]	PFEC0L[3:2]	—	ULPI_DATA[5:4]	—	I	EVDD	G3, G4	AB9, Y9
FEC0_RXD1	PFEC0L1	FEC0_RMII_RXD1	—	—	I	EVDD	H1	W9
FEC0_RXD0	PFEC0H1	FEC0_RMII_RXD0	—	—	I	EVDD	H2	AB10
FEC0_RXER	PFEC0L0	FEC0_RMII_RXER	—	—	I	EVDD	H3	AA10

Table 4. MCF5445*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
FEC0_TXCLK	PFEC0H7	FEC0_RMII_ REF_CLK	—	—	I	EVDD	H4	Y10
FEC0_TXD[3:2]	PFEC0L[7:6]	—	ULPI_DATA[3:2]	—	O	EVDD	J1, J2	W10, AB11
FEC0_TXD1	PFEC0L5	FEC0_RMII_TXD1	—	—	O	EVDD	J3	AA11
FEC0_TXD0	PFEC0H5	FEC0_RMII_TXD0	—	—	O	EVDD	J4	Y11
FEC0_TXEN	PFEC0H6	FEC0_RMII_TXEN	—	—	O	EVDD	K1	W11
FEC0_TXER	PFEC0L4	—	ULPI_DATA0	—	O	EVDD	K2	AB12
FEC1								
FEC1_MDC	PFECI2C5	—	$\overline{\text{ATA\_DIOR}}$	—	O	EVDD	—	W20
FEC1_MDIO	PFECI2C4	—	$\overline{\text{ATA\_DIOW}}$	—	I/O	EVDD	—	Y22
FEC1_COL	PFEC1H4	—	ATA_DATA7	—	I	EVDD	—	AB18
FEC1_CRS	PFEC1H0	—	ATA_DATA6	—	I	EVDD	—	AA18
FEC1_RXCLK	PFEC1H3	—	ATA_DATA5	—	I	EVDD	—	W14
FEC1_RXDV	PFEC1H2	FEC1_RMII_ CRS_DV	ATA_DATA15	—	I	EVDD	—	AB15
FEC1_RXD[3:2]	PFEC1L[3:2]	—	ATA_DATA[4:3]	—	I	EVDD	—	AA15, Y15
FEC1_RXD1	PFEC1L1	FEC1_RMII_RXD1	ATA_DATA14	—	I	EVDD	—	AA17
FEC1_RXD0	PFEC1H1	FEC1_RMII_RXD0	ATA_DATA13	—	I	EVDD	—	Y17
FEC1_RXER	PFEC1L0	FEC1_RMII_RXER	ATA_DATA12	—	I	EVDD	—	W17
FEC1_TXCLK	PFEC1H7	FEC1_RMII_ REF_CLK	ATA_DATA11	—	I	EVDD	—	AB19
FEC1_TXD[3:2]	PFEC1L[7:6]	—	ATA_DATA[2:1]	—	O	EVDD	—	Y19, W18
FEC1_TXD1	PFEC1L5	FEC1_RMII_TXD1	ATA_DATA10	—	O	EVDD	—	AA19
FEC1_TXD0	PFEC1H5	FEC1_RMII_TXD0	ATA_DATA9	—	O	EVDD	—	Y20
FEC1_TXEN	PFEC1H6	FEC1_RMII_TXEN	ATA_DATA8	—	O	EVDD	—	AA21
FEC1_TXER	PFEC1L4	—	ATA_DATA0	—	O	EVDD	—	AA22
USB On-the-Go								
USB_DM	—	—	—	—	O	USB VDD	F16	A14
USB_DP	—	—	—	—	O	USB VDD	E16	A15
USB_VBUS_EN	PUSB1	USB_PULLUP	ULPI_NXT	—	O	USB VDD	E5	AA2
USB_VBUS_OC	PUSB0	—	ULPI_STP	UD[7]	I	USB VDD	B3	V4

Table 4. MCF5445*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF54450 MCF54451 256 MAPBGA	MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA
ATA								
ATA_BUFFER_EN	PATAH5	—	—	—	O	EVDD	—	Y13
$\overline{\text{ATA\_CS}}$[1:0]	PATAH[4:3]	—	—	—	O	EVDD	—	W21, W22
ATA_DA[2:0]	PATAH[2:0]	—	—	—	O	EVDD	—	V19–21
$\overline{\text{ATA\_RESET}}$	PATAL2	—	—	—	O	EVDD	—	W13
ATA_DMARQ	PATAL1	—	—	—	I	EVDD	—	AA14
ATA_IORDY	PATAL0	—	—	—	I	EVDD	—	Y14
Real Time Clock								
EXTAL32K	—	—	—	—	I	EVDD	J16	A13
XTAL32K	—	—	—	—	O	EVDD	H16	A12
SSI								
SSI_MCLK	PSSI4	—	—	—	O	EVDD	T13	D20
SSI_BCLK	PSSI3	$\overline{\text{U1CTS}}$	—	—	I/O	EVDD	R13	E19
SSI_FS	PSSI2	$\overline{\text{U1RTS}}$	—	—	I/O	EVDD	P12	E20
SSI_RXD	PSSI1	U1RXD	—	UD	I	EVDD	T12	D21
SSI_TXD	PSSI0	U1TXD	—	UD	O	EVDD	R12	D22
I^2C								
I2C_SCL	PFECI2C1	—	U2TXD	U	I/O	EVDD	K3	AA12
I2C_SDA	PFECI2C0	—	U2RXD	U	I/O	EVDD	K4	Y12
DMA								
$\overline{\text{DACK1}}$	PDMA3	—	ULPI_DIR	—	O	EVDD	M14	C17
$\overline{\text{DREQ1}}$	PDMA2	—	USB_CLKIN	U	I	EVDD	P16	C18
$\overline{\text{DACK0}}$	PDMA1	DSPI_PCS3	—	—	O	EVDD	N15	A18
$\overline{\text{DREQ0}}$	PDMA0	—	—	U	I	EVDD	N16	B18
DSPI								
DSPI_PCS5/$\overline{\text{PCSS}}$	PDSPI6	—	—	—	O	EVDD	N14	D18
DSPI_PCS2	PDSPI5	—	—	—	O	EVDD	L13	A19
DSPI_PCS1	PDSPI4	$\overline{\text{SBF\_CS}}$	—	—	O	EVDD	P14	B20
DSPI_PCS0/$\overline{\text{SS}}$	PDSPI3	—	—	U	I/O	EVDD	R16	D17
DSPI_SCK	PDSPI2	SBF_CK	—	—	I/O	EVDD	R15	A20

4.2 Pinout—256 MAPBGA

The pinout for the MCF54450 and MCF54451 packages are shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A		FB_OE	FB_TS	FB_BE/BWE0	FB_BE/BWE2	FB_AD 2	FB_AD 6	FB_AD 10	FB_AD 14	FB_AD 18	FB_AD 22	FB_AD 26	FB_AD 30	FB_AD 31	T0IN		A
B	FB_TA	FB_R/W	USB_VBUS_OC	FB_BE/BWE1	FB_BE/BWE3	FB_AD 3	FB_AD 7	FB_AD 11	FB_AD 15	FB_AD 19	FB_AD 23	FB_AD 27	FB_CLK	T1IN	FB_A 4	FB_A 6	B
C	PST DDATA2	FB_CS3	FB_CS1	FB_CS0	FB_AD 0	FB_AD 4	FB_AD 8	FB_AD 12	FB_AD 16	FB_AD 20	FB_AD 24	FB_AD 28	T3IN	FB_A 3	FB_A 5	FB_A 1	C
D	PST DDATA6	PST DDATA3	PST DDATA0	FB_CS2	FB_AD 1	FB_AD 5	FB_AD 9	FB_AD 13	FB_AD 17	FB_AD 21	FB_AD 25	FB_AD 29	T2IN	FB_A 0	FB_A 2	FB_A 7	D
E	FEC0_COL	PST DDATA7	PST DDATA4	PST DDATA1	USB_VBUS_EN	IVDD	IVDD	IVDD	IVDD	IVDD	IVDD	IVDD	FB_A 8	FB_A 9	FB_A 10	USB_DP	E
F	FEC0_CRS	FEC0_MDIO	FEC0_MDC	PST DDATA5	IVDD							IVDD	FB_A 11	FB_A 12	IRQ_1	USB_DM	F
G	FEC0_RXCLK	FEC0_RXDV	FEC0_RXD3	FEC0_RXD2	EVDD							EVDD	FB_A 13	FB_A 14	FB_A 15	NC	G
H	FEC0_RXD1	FEC0_RXD0	FEC0_RXER	FEC0_TXCLK	EVDD							EVDD	FB_A 18	FB_A 17	FB_A 16	XTAL 32K	H
J	FEC0_TXD3	FEC0_TXD2	FEC0_TXD1	FEC0_TXD0	EVDD							EVDD	FB_A 19	FB_A 20	FB_A 21	EXTAL 32K	J
K	FEC0_TXEN	FEC0_TXER	I2C_SCL	I2C_SDA	EVDD							EVDD	FB_A 22	FB_A 23	VDD_A_PLL	PLL TEST	K
L	IRQ_7	IRQ_4	IRQ_3	RESET	EVDD	EVDD						EVDD	DSPI_PCS2	VDD_OSC	VSS_OSC	XTAL	L
M	U0TXD	U0RTS	U0CTS	SD_A7	BOOT MOD1	TEST	BOOT MOD0	SD_VREF			JTAG_EN	VDD_RTC	TRST	DACK1	RST OUT	EXTAL	M
N	U0RXD	SD_A11	SD_A6	SD_A0	SD_CKE	SD_D31	SD_D29	SD_D24	SD_D23	SD_D19	SD_DQS2	SD_DM2	DSPI_SOUT	DSPI_PCS5	DACK0	DREQ0	N
P	SD_A12	SD_A10	SD_A5	SD_BA1	SD_RAS	SD_CS1	SD_D28	SD_D25	SD_DM3	SD_D20	SD_D16	SSI_FS	TCLK	DSPI_PCS1	DSPI_SIN	DREQ1	P
R	SD_A13	SD_A9	SD_A4	SD_A1	SD_WE	SD_CS0	SD_D27	SD_D26	SD_DQS3	SD_D21	SD_D17	SSI_TXD	SSI_BCLK	TMS	DSPI_SCK	DSPI_PCS0	R
T		SD_A8	SD_A3	SD_A2	SD_BA0	SD_CAS	SD_D30	SD_CLK	SD_CLK	SD_D22	SD_D18	SSI_RXD	SSI_MCLK	TDO	TDI		T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 5. MCF54450 and MCF54451 Pinout (256 MAPBGA)

4.3 Pinout—360 TEPBGA

The pinout for the MCF54452, MCF54453, MCF54454, and MCF54455 packages are shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A		PCI_REQ0	PCI_AD10	PCI_AD11	PCI_AD13	PCI_SERR	PCI_STOP	PCI_AD15	PCI_GNT0	PCI_AD29	PCI_AD20	XTAL 32K	EXTAL 32K	USB_DM	USB_DP	EXTAL	XTAL	DACK0	DSPI_PCS2	DSPI_SCK	TDO		A
B	PCI_CBE0	PCI_FRAME	PCI_AD9	PCI_PERR	PCI_AD12	PCI_RST	PCI_GNT3	PCI_AD14	PCI_AD18	PCI_AD28	PCI_AD19	PCI_AD21	NC		NC	VDD_OSC	RSTOUT	DREQ0	DSPI_SIN	DSPI_PCS1	TMS	TRST	B
C	PCI_AD0	PCI_AD2	PCI_IRDY	PCI_PAR	PCI_REQ1	IRQ1	PCI_REQ3	PCI_GNT2	PCI_GNT1	PCI_TRDY	PCI_AD31	PCI_AD22	VDD_RTC	VDD_A_PLL	NC	VSS_OSC	DACK1	DREQ1	TDI	DSPI_SOUT	JTAG_EN	TCLK	C
D	PCI_CBE1	PCI_AD1	PCI_AD7	PCI_AD8	PCI_IDSEL	IVDD	PCI_REQ2	IVDD	PCI_AD17	PCI_AD16	PCI_AD30	PCI_AD23	EVDD	IVDD	PLL TEST	NC	DSPI_PCS0	DSPI_PCS5	EVDD	SSI_MCLK	SSI_RXD	SSI_TXD	D
E	PCI_AD4	PCI_AD5	PCI_AD6	PCI_CBE2															SSI_BCLK	SSI_FS	SD_DM2	SD_DQS2	E
F	PCI_AD24	PCI_DEVSEL	PCI_AD3	IVDD																SD_D16	SD_D17	SD_D18	F
G	T0IN	PCI_AD26	PCI_AD25	PCI_CBE3				EVDD			EVDD			EVDD		EVDD			SD_D19	SD_D20	SD_D21	SD_D22	G
H	T2IN	T3IN	T1IN	IVDD																SD_D23	SD_DM3	SD_DQS3	H
J	FB_AD29	FB_AD31	FB_CLK	PCI_AD27				EVDD								EVDD			SD_D26	SD_D27	SD_D25	SD_D24	J
K	FB_AD28	FB_AD27	FB_AD26	FB_AD30																SD_D28	SD_D29	SD_D30	K
L	FB_AD25	FB_AD23	FB_AD22	FB_AD24				EVDD								EVDD			SD_CAS	SD_CS1	SD_D31	SD_CLK	L
M	FB_AD21	FB_AD20	FB_AD19	FB_AD18																SD_CS0	SD_VREF	SD_CLK	M
N	FB_AD17	FB_AD16	U1TXD	IVDD												EVDD			SD_A2	SD_WE	SD_RAS	SD_CKE	N
P	FB_AD15	FB_AD14	U1RXD	FB_AD10				EVDD											SD_BA0	SD_A1	SD_A0	SD_BA1	P
R	FB_AD13	FB_AD12	FB_AD11	IVDD												EVDD				SD_A5	SD_A4	SD_A3	R
T	FB_AD9	FB_AD8	FB_AD7	FB_AD6				EVDD			EVDD			EVDD		EVDD			SD_A9	SD_A8	SD_A7	SD_A6	T
U	FB_AD5	FB_AD4	FB_AD3	U1RTS																SD_A12	SD_A11	SD_A10	U
V	FB_AD2	FB_AD1	U1CTS	USB_VBUS_OC															ATA_DA2	ATA_DA1	ATA_DA0	SD_A13	V
W	FB_AD0	FB_BE/BWE2	FB_BE/BWE1	IVDD	FB_CS3	PST DDATA4	IVDD	IVDD	FEC0_RXD1	FEC0_TXD3	FEC0_TXEN	IVDD	ATA_RESET	FEC1_RXCLK	U0TXD	IVDD	FEC1_RXER	FEC1_TXD2	IVDD	FEC1_MDC	ATA_CS1	ATA_CS0	W
Y	FB_BE/BWE3	FB_BE/BWE0	FB_TS	FB_CS0	PST DDATA0	PST DDATA3	FEC0_MDIO	FEC0_RXDV	FEC0_RXD2	FEC0_TXCLK	FEC0_TXD0	I2C_SDA	ATA_BUFFER_EN	ATA_IORDY	FEC1_RXD2	U0CTS	FEC1_RXD0	RESET	FEC1_TXD3	FEC1_TXD0	NC	FEC1_MDIO	Y
AA	FB_OE	USB_VBUS_EN	FB_R/W	FB_CS2	PST DDATA2	PST DDATA7	FEC0_CRS	FEC0_RXCLK	NC	FEC0_RXER	FEC0_TXD1	I2C_SCL	IRQ4	ATA_DMARQ	FEC1_RXD3	U0RTS	FEC1_RXD1	FEC1_CRS	FEC1_TXD1	NC	FEC1_TXEN	FEC1_TXER	AA
AB		FB_TA	FB_CS1	PST DDATA1	PST DDATA5	PST DDATA6	FEC0_COL	FEC0_MDC	FEC0_RXD3	FEC0_RXD0	FEC0_TXD2	FEC0_TXER	IRQ7	IRQ3	FEC1_RXDV	U0RXD	BOOT MOD1	FEC1_COL	FEC1_TXCLK	TEST	BOOT MOD0		AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure 6. MCF54452, MCF54453, MCF54454, and MCF54455 Pinout (360 TEPBGA)

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

5.3 ESD Protection

Table 7. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 8. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Units
Internal logic supply voltage[1]	IV_{DD}	1.35	1.65	V
PLL analog operation voltage range [1]	PV_{DD}	1.35	1.65	V
External I/O pad supply voltage	EV_{DD}	3.0	3.6	V
Internal oscillator supply voltage	$OSCV_{DD}$	3.0	3.6	V
Real-time clock supply voltage	$RTCV_{DD}$	1.35	1.65	V
SDRAM I/O pad supply voltage — DDR mode	SDV_{DD}	2.25	2.75	V
SDRAM I/O pad supply voltage — DDR2 mode	SDV_{DD}	1.7	1.9	V
SDRAM I/O pad supply voltage — Mobile DDR mode	SDV_{DD}	1.7	1.9	V
SDRAM input reference voltage	SDV_{REF}	0.49 x SDV_{DD}	0.51 x SDV_{DD}	V
Input High Voltage	V_{IH}	0.7 x EV_{DD}	3.65	V
Input Low Voltage	V_{IL}	V_{SS} – 0.3	0.35 x EV_{DD}	V
Input Hysteresis	V_{HYS}	0.06 x EV_{DD}	—	mV
Input Leakage Current[2] V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–2.5	2.5	µA
Input Leakage Current[3] V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–5	5	µA
High Impedance (Off-State) Leakage Current[4] V_{in} = V_{DD} or V_{SS}, All input/output and output pins	I_{OZ}	–10.0	10.0	µA
Output High Voltage (All input/output and all output pins) I_{OH} = –5.0 mA	V_{OH}	0.85 × EV_{DD}	—	V
Output Low Voltage (All input/output and all output pins) I_{OL} = 5.0mA	V_{OL}	—	0.15 × EV_{DD}	V

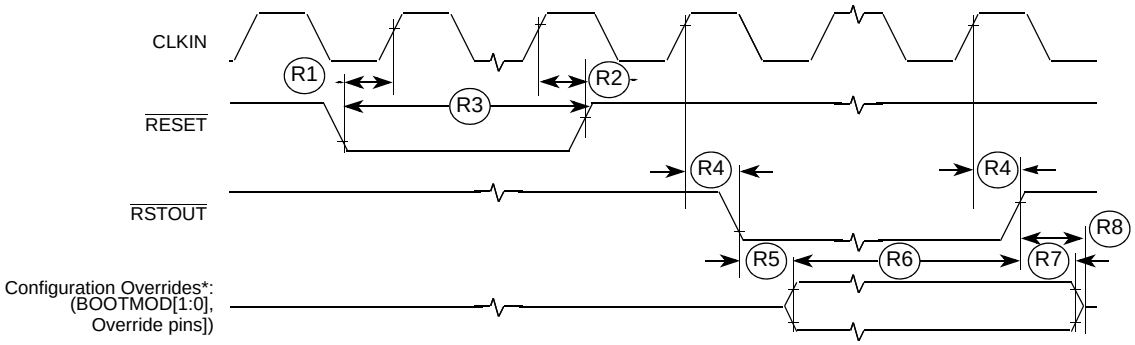


Figure 8. $\overline{\text{RESET}}$ and Configuration Override Timing

5.7 FlexBus Timing Specifications

A multi-function external bus interface called FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 66MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices, a simple chip-select based interface can be used.

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 12. FlexBus AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	25	66.66	MHz	
FB1	Clock Period	15	40	ns	
FB2	Output Valid	—	7.0	ns	[1]
FB3	Output Hold	1.0	—	ns	1
FB4	Input Setup	3.0	—	ns	[2]
FB5	Input Hold	0	—	ns	2

[1] Specification is valid for all FB_AD[31:0], $\overline{\text{FB\_BS}}$[3:0], $\overline{\text{FB\_CS}}$[3:0], $\overline{\text{FB\_OE}}$, FB_R/$\overline{\text{W}}$, $\overline{\text{FB\_TBST}}$, FB_TSIZ[1:0], and $\overline{\text{FB\_TS}}$.

[2] Specification is valid for all FB_AD[31:0] and $\overline{\text{FB\_TA}}$.

NOTE

The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial.

The address and data busses are muxed between the FlexBus and PCI controller. At the end of the read and write bus cycles the address signals are indeterminate.

5.8 SDRAM AC Timing Characteristics

The following timing numbers must be followed to properly latch or drive data onto the SDRAM memory bus. All timing numbers are relative to the four DQS byte lanes.

Table 13. SDRAM Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of Operation		60	133.33	MHz	1
DD1	Clock Period	t_{SDCK}	7.5	16.67	ns	
DD2	Pulse Width High	t_{SDCKH}	0.45	0.55	t_{SDCK}	2
DD3	Pulse Width Low	t_{SDCKL}	0.45	0.55	t_{SDCK}	3
DD4	Address, SD_CKE, $\overline{SD\_CAS}$, $\overline{SD\_RAS}$, $\overline{SD\_WE}$, $\overline{SD\_CS}$[1:0] — Output Valid	t_{CMV}	—	(0.5 x t_{SDCK}) + 1.0ns	ns	3
DD5	Address, SD_CKE, $\overline{SD\_CAS}$, $\overline{SD\_RAS}$, $\overline{SD\_WE}$, $\overline{SD\_CS}$[1:0] — Output Hold	t_{CMH}	2.0	—	ns	
DD6	Write Command to first DQS Latching Transition	t_{DQSS}	(1.0 x t_{SDCK}) - 0.6ns	(1.0 x t_{SDCK}) + 0.6ns	ns	
DD7	Data and Data Mask Output Setup (DQ-->DQS) Relative to DQS (DDR Write Mode)	t_{QS}	1.0	—	ns	4 5
DD8	Data and Data Mask Output Hold (DQS-->DQ) Relative to DQS (DDR Write Mode)	t_{QH}	1.0	—	ns	6
DD9	Input Data Skew Relative to DQS (Input Setup)	t_{IS}	—	1.0	ns	7
DD10	Input Data Hold Relative to DQS.	t_{IH}	(0.25 x t_{SDCK}) + 0.5ns	—	ns	8

1 The SDRAM interface operates at the same frequency as the internal system bus.

2 Pulse width high plus pulse width low cannot exceed min and max clock period.

3 Command output valid should be 1/2 the memory bus clock (t_{SDCK}) plus some minor adjustments for process, temperature, and voltage variations.

4 This specification relates to the required input setup time of DDR memories. The microprocessor's output setup should be larger than the input setup of the DDR memories. If it is not larger, then the input setup on the memory is in violation.
SD_D[31:24] is relative to SD_DQS[3]; SD_D[23:16] is relative to SD_DQS[2]

5 The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.

6 This specification relates to the required hold time of DDR memories.
SD_D[31:24] is relative to SD_DQS[3]; SD_D[23:16] is relative to SD_DQS[2]

7 Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

8 Data input hold is derived from each DQS clock edge. It begins with a DQS transition and ends when the first data line becomes invalid.

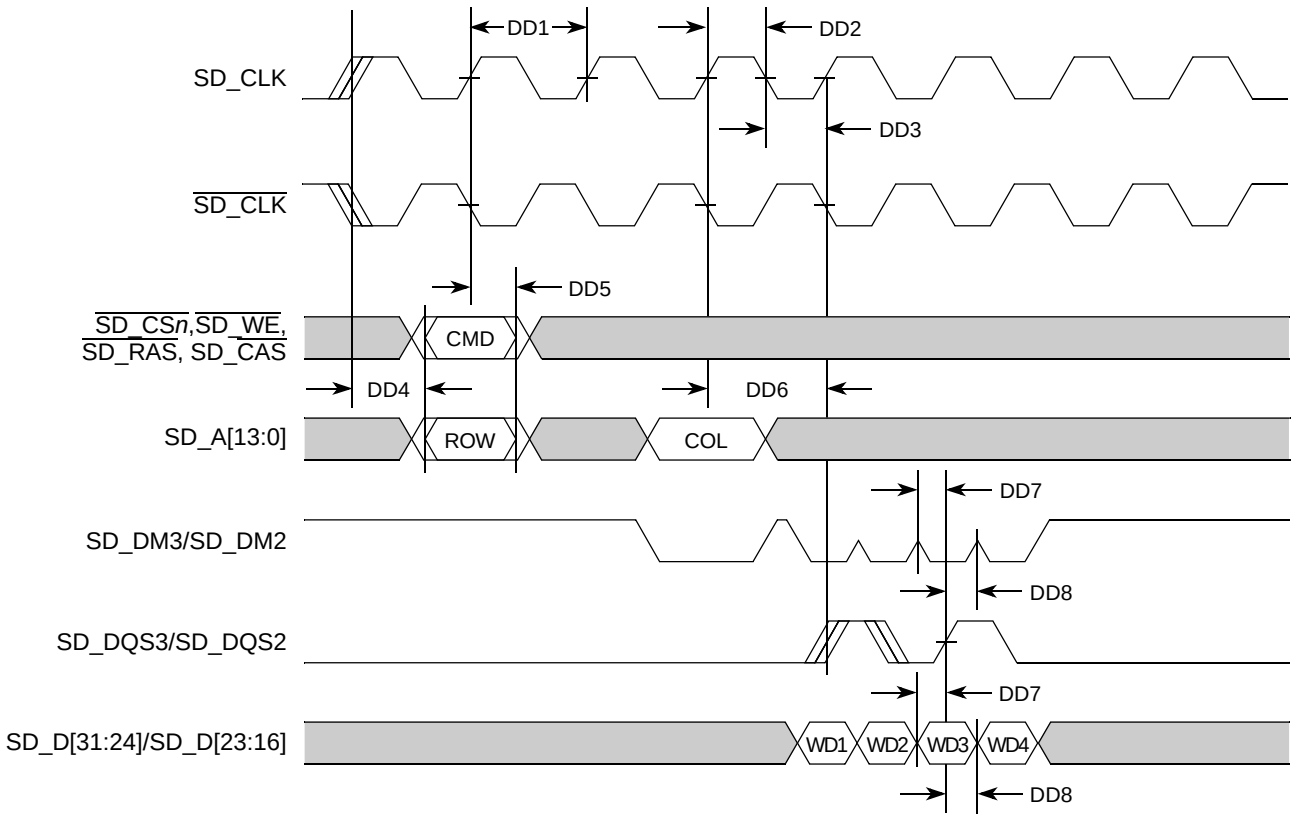


Figure 11. DDR Write Timing

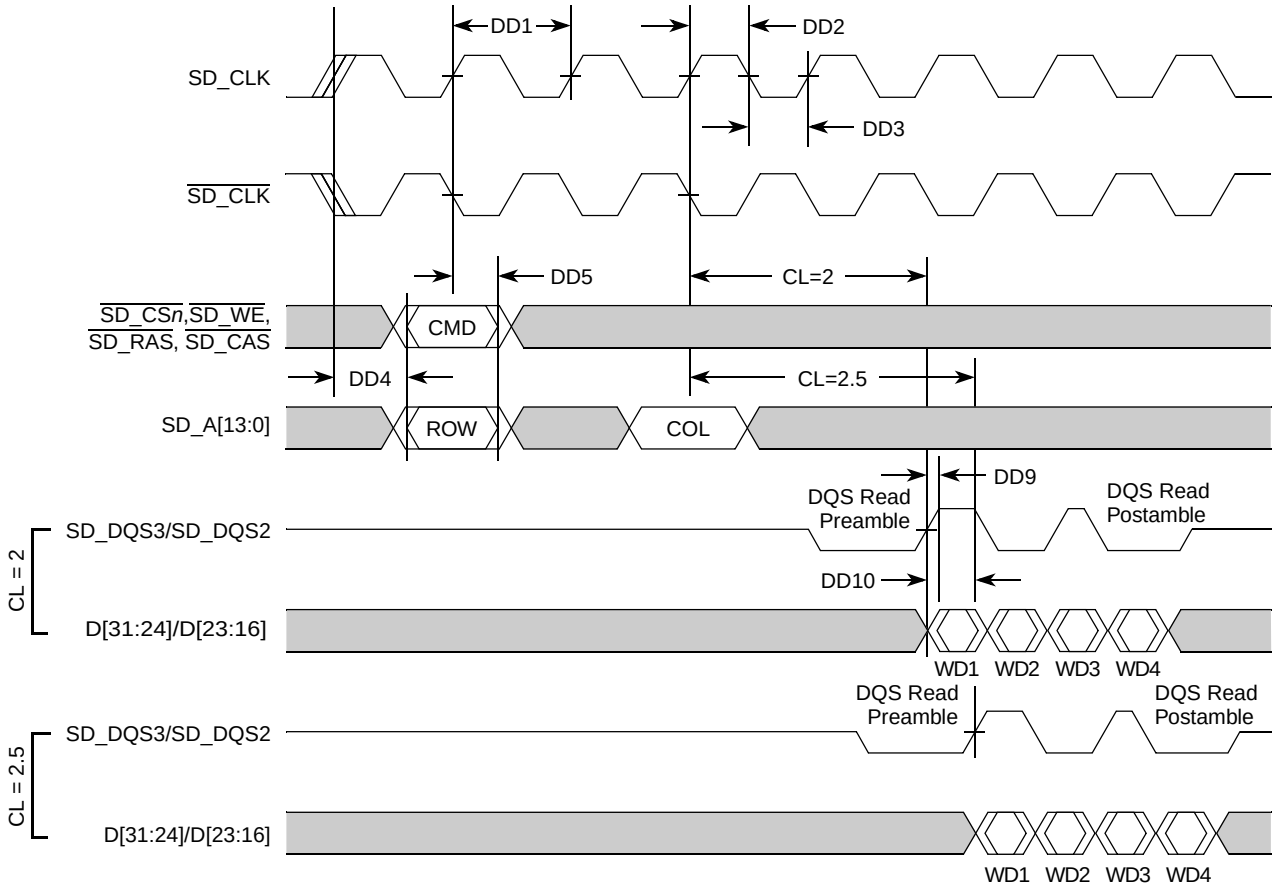


Figure 12. DDR Read Timing

5.9 PCI Bus Timing Specifications

The PCI bus on the device is PCI 2.2 compliant. The following timing numbers are mostly from the PCI 2.2 spec. Refer to the PCI 2.2 spec for a more detailed timing analysis.

Table 14. PCI Timing Specifications[1,2]

Num	Characteristic	33 MHz[3]		66 MHz[3]		
		Min	Max	Min	Max	Unit
	Frequency of Operation	—	33.33	33.33	66.66	MHz
P1	Clock Period	30	—	15	30	ns
P2	Bused PCI signals — input setup	7.0	—	3.0	—	ns
P3	$\overline{\text{PCI\_GNT}}$[3:0]/$\overline{\text{PCI\_REQ}}$[3:0] — input setup	10.0	—	5.0	—	ns
P4	All PCI signals — input hold	0	—	0	—	ns
P5	Bused PCI signals — output valid	—	11.0	—	6.0	ns

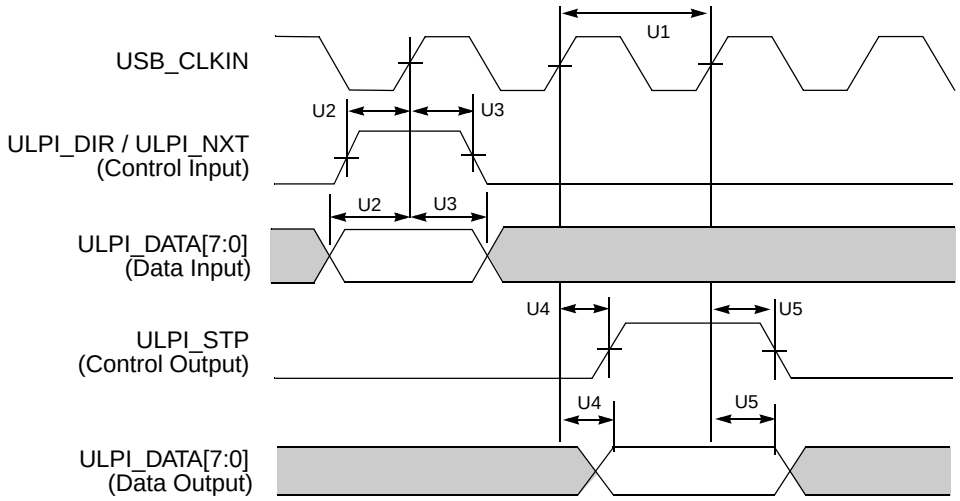


Figure 15. ULPI Timing Diagram

5.11 SSI Timing Specifications

This section provides the AC timings for the SSI in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (SSI_TCR[TSCKP] = 0, SSI_RCR[RSCKP] = 0) and a non-inverted frame sync (SSI_TCR[TFSI] = 0, SSI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SSI_BCLK) and/or the frame sync (SSI_FS) shown in the figures below.

Table 16. SSI Timing — Master Modes[1]

Num	Description	Symbol	Min	Max	Units	Notes
S1	SSI_MCLK cycle time	t_{MCLK}	$2 \times t_{SYS}$	—	ns	2
S2	SSI_MCLK pulse width high / low		45%	55%	t_{MCLK}	
S3	SSI_BCLK cycle time	t_{BCLK}	$8 \times t_{SYS}$	—	ns	3
S4	SSI_BCLK pulse width		45%	55%	t_{BCLK}	
S5	SSI_BCLK to SSI_FS output valid		—	15	ns	
S6	SSI_BCLK to SSI_FS output invalid		0	—	ns	
S7	SSI_BCLK to SSI_TXD valid		—	15	ns	
S8	SSI_BCLK to SSI_TXD invalid / high impedence		-2	—	ns	
S9	SSI_RXD / SSI_FS input setup before SSI_BCLK		10	—	ns	
S10	SSI_RXD / SSI_FS input hold after SSI_BCLK		0	—	ns	

1 All timings specified with a capactive load of 25pF.

2 SSI_MCLK can be generated from SSI_CLKIN or a divided version of the internal system clock (f_{sys}).

3 SSI_BCLK can be derived from SSI_CLKIN or a divided version of the internal system clock (f_{sys}).

Table 19. I²C Output Timing Specifications between SCL and SDA (continued)

Num	Characteristic	Min	Max	Units
I6[1]	Clock high time	10	—	t_{SYS}
I7[1]	Data setup time	2	—	t_{SYS}
I8[1]	Start condition setup time (for repeated start condition only)	20	—	t_{SYS}
I9[1]	Stop condition setup time	10	—	t_{SYS}

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 19. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR. However, the numbers given in Table 19 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

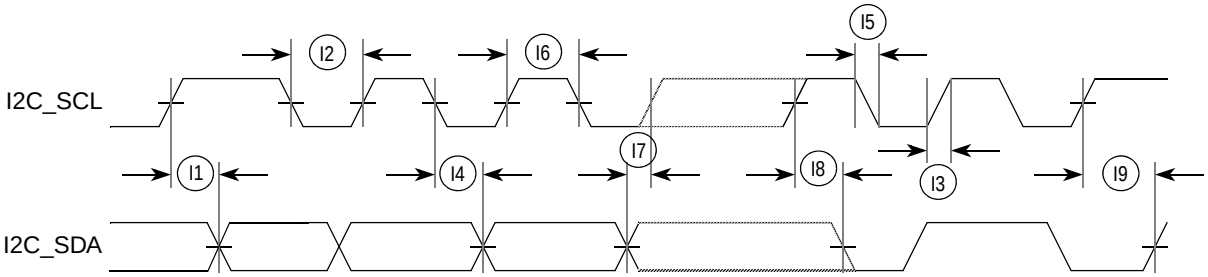


Figure 18. I²C Input/Output Timings

5.13 Fast Ethernet Timing Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

5.13.1 Receive Signal Timing Specifications

The following timing specs meet the requirements for MII and 7-Wire style interfaces for a range of transceiver devices.

Table 20. Receive Signal Timing

Num	Characteristic	MII Mode		RMII Mode		Unit
		Min	Max	Min	Max	
—	RXCLK frequency	—	25	—	50	MHz
E1	RXD[n:0], RXDV, RXER to RXCLK setup[1]	5	—	4	—	ns
E2	RXCLK to RXD[n:0], RXDV, RXER hold[1]	5	—	2	—	ns
E3	RXCLK pulse width high	35%	65%	35%	65%	RXCLK period
E4	RXCLK pulse width low	35%	65%	35%	65%	RXCLK period

1 In MII mode, n = 3; In RMII mode, n = 1

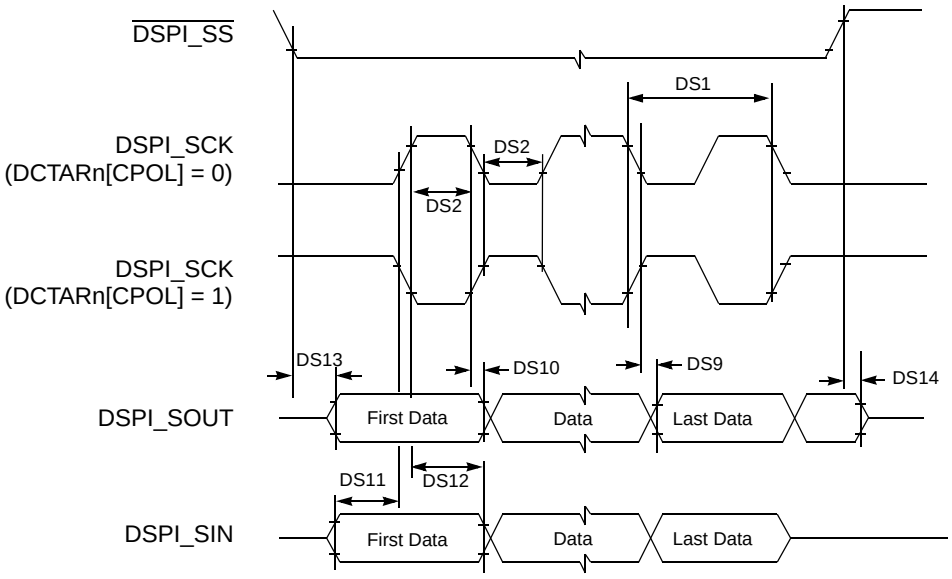


Figure 24. DSPI Classic SPI Timing—Slave Mode

5.17 SBF Timing Specifications

The Serial Boot Facility (SBF) provides a means to read configuration information and system boot code from a broad array of SPI-compatible EEPROMs, flashes, FRAMs, nVSRAMs, etc. Table 27 provides the AC timing specifications for the SBF.

Table 27. SBF AC Timing Specifications

Name	Characteristic	Symbol	Min	Max	Unit	Notes
SB1	SBF_CK Cycle Time	t_{SBFCK}	40	—	ns	[1]
SB2	SBF_CK High/Low Time	—	30%	—	t_{SBFCK}	
SB3	$\overline{\text{SBF\_CS}}$ to SBF_CK delay	—	t_{SBFCK} - 2.0	—	ns	
SB4	SBF_CK to $\overline{\text{SBF\_CS}}$ delay	—	t_{SBFCK} - 2.0	—	ns	
SB5	SBF_CK to SBF_DO valid	—	-5	—	ns	
SB6	SBF_CK to SBF_DO invalid	—	5	—	ns	
SB7	SBF_DI to SBF_SCK input setup	—	10	—	ns	
SB8	SBF_CK to SBF_DI input hold	—	0	—	ns	

[1] At reset, the SBF_CK cycle time is $t_{REF} \times 67$. The first byte of data read from the serial memory contains a divider value that is used to set the SBF_CK cycle time for the duration of the serial boot process.

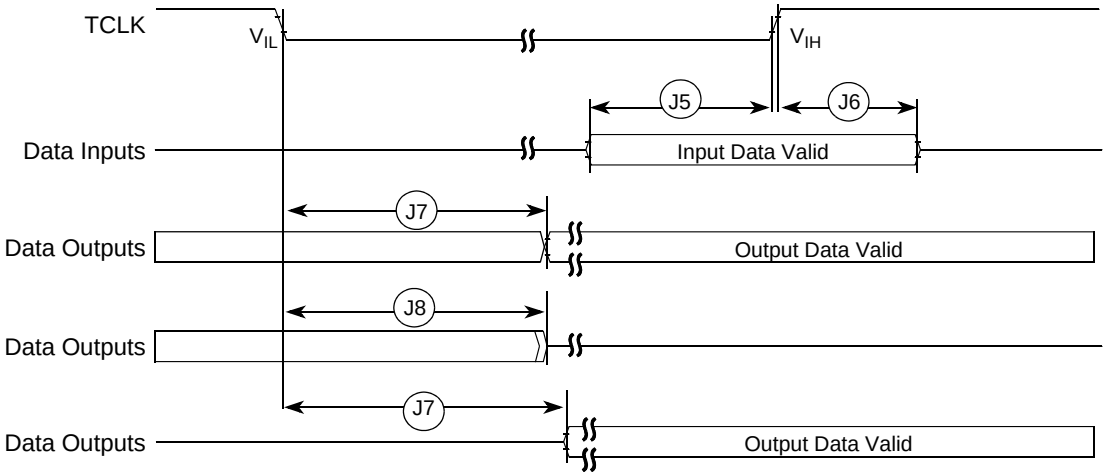


Figure 28. Boundary Scan (JTAG) Timing

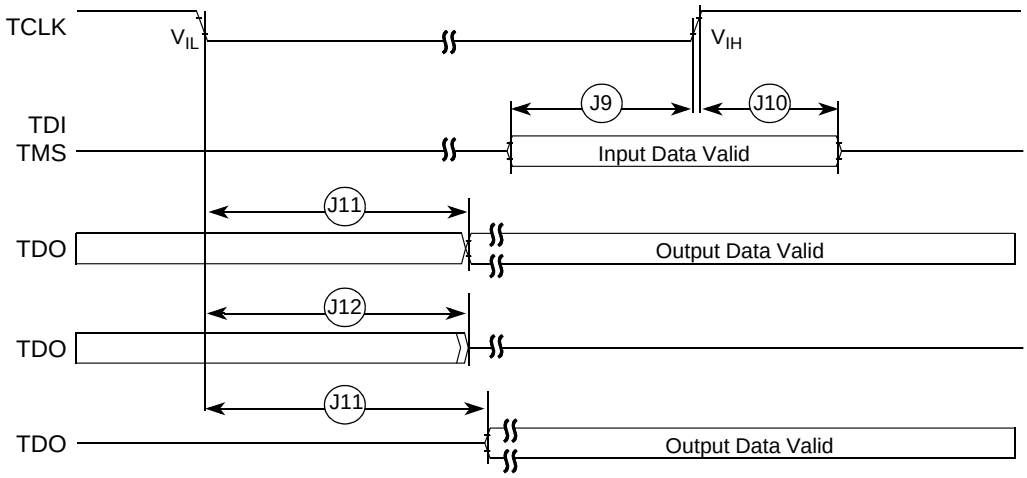


Figure 29. Test Access Port Timing

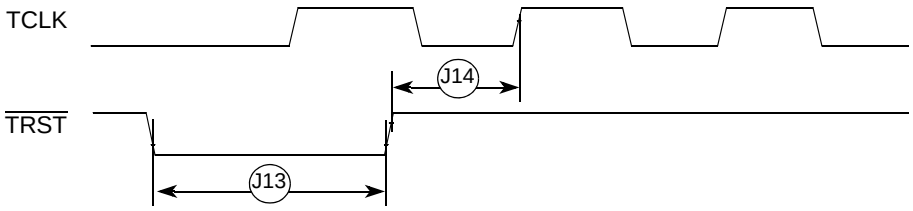


Figure 30. $\overline{\text{TRST}}$ Timing

5.20 Debug AC Timing Specifications

Table 30 lists specifications for the debug AC timing parameters shown in Figure 31 and Table 32.

Table 30. Debug AC Timing Specification

Num	Characteristic	Min	Max	Units
D0	PSTCLK cycle time	1	1	t_{SYS}
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	1.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4[1]	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

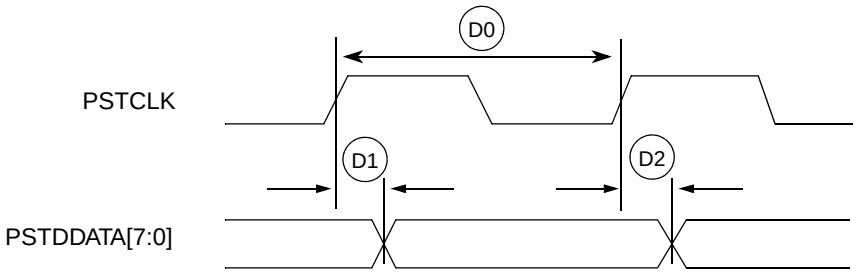


Figure 31. Real-Time Trace AC Timing

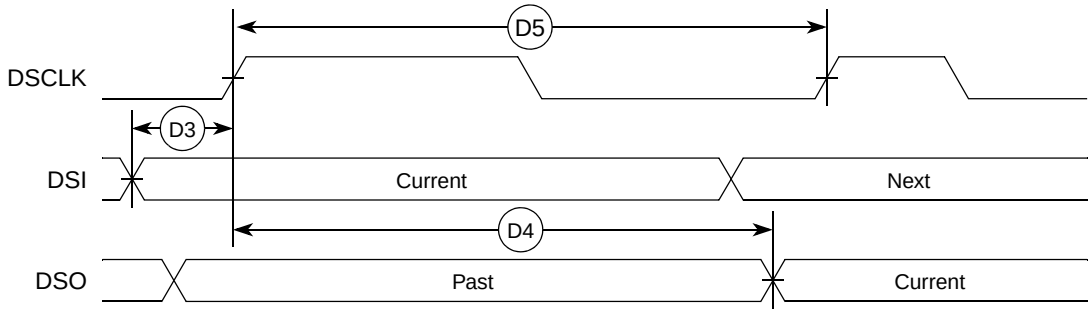


Figure 32. BDM Serial Port AC Timing

9 Revision History

Table 34 summarizes revisions to this document.

Table 34. Revision History

Rev. No.	Date	Summary of Changes
0	Sept 17, 2007	Initial public release.
1	Feb 15, 2008	Corrected VSS pin locations in MCF5445*x* signal information and muxing table for the 360 TEPBGA package: changed "...M9, M16, M17..." to "...M9–M14, M16..." Updated FlexBus read and write timing diagrams and added two notes before them. Change FB_A[23:0] to FB_A[31:0] in FlexBus read and write timing diagrams. Added power consumption section.
2	May 1, 2008	In Family Configurations table, added PCI as feature on 256-pin devices. On these devices the PCI_AD bus is limited to 24-bits. In Absolute Maximum Ratings table, changed $RTCV_{DD}$ specification from "-0.3 to +4.0" to "-0.5 to +2.0". In DC Electrical Specifications table: • Changed $RTCV_{DD}$ specification from 3.0–3.6 to 1.35–1.65. • Changed High Impedance (Off-State) Leakage Current (I_{OZ}) specification from ±1 to ±10μA, and added footnote to this spec: "Worst-case tristate leakage current with only one I/O pin high. Since all I/Os share power when high, the leakage current is distributed among them. With all I/Os high, this spec reduces to ±2 μA min/max."
3	Dec 1, 2008	Changed "360PBGA" heading to "360 TEPBGA" in Table 6. Changed the following specs in Table 13: • Minimum frequency of operation from — to 60MHz. • Maximum clock period from — to 16.67 ns.
4	Apr 12, 2009	Rescinded previous errata, the 256-pin devices do not contain the PCI bus controller: • In Table 4, in PCI_AD*n* signal section, added a separate row for each package, with PCI_AD*n* signals shown as — for 256-pin devices. • In Figure 5, changed the PCI_AD*n* pins to their alternative function, FB_A*n*.
5	Apr 27, 2009	In Table 2 changed MCF54450VM180 to MCF54450CVM180 and changed it's temperature entry from "0° to +70° C" to "–40° to +85° C".
6	Oct 15, 2009	In Table 8 changed Input Leakage Current (I_{in}) from ±1.0 to ±2.5μA.
7	Oct 18, 2011	In Table 2, added MCF54452YVR200 part number, with temperature range from –40° to +105° C. In Table 8, added Input Leakage Current (I_{in}) values for MCF54452YVR200 part number.
8	Jan 18, 2012	In Table 4, added pin N7 in the VSS pin list for the 360 TEPBGA.