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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	MAXQ20S
Core Size	16-Bit
Speed	12MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	16
Program Memory Size	80KB (40K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-20°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	25-WFBGA, WLBGA
Supplier Device Package	25-WLP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq614v-2541-t

16-Bit Microcontroller with Infrared Module

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{DD} with Respect to GND -0.3V to +3.6V
 Voltage Range on Any Lead with
 Respect to GND Except V_{DD} -0.3V to ($V_{DD} + 0.5V$)

Operating Temperature Range -20°C to +70°C
 Storage Temperature Range -65°C to +150°C
 Soldering Temperature (reflow) +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

($V_{DD} = V_{RST}$ to 3.6V, $T_A = -20^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V _{DD}			V _{RST}		3.6	V
1.8V Internal Regulator	V _{REG18}			1.62	1.8	1.98	V
Power-Fail Warning Voltage for Supply	V _{PFW}	Monitors V _{DD} (Note 2)		1.75	1.8	1.85	V
Power-Fail Reset Voltage	V _{RST}	Monitors V _{DD} (Note 3)		1.64	1.67	1.70	V
POR Voltage	V _{POR}	Monitors V _{DD}		1.0		1.42	V
RAM Data-Retention Voltage					1.0		V
Active Current	I _{DD_1}	Sysclk = 12MHz (Note 5)			2.5	3.75	mA
Stop-Mode Current	I _{S1}	Power-fail off	T _A = +25°C		0.15	2.0	μA
			T _A = 0°C +70°C		0.15	8	
	I _{S2}	Power-fail on	T _A = +25°C		22	31	
			T _A = 0°C to +70°C		27.6	38	
Current Consumption During Power-Fail	I _{PFR}	(Note 6)		[(3 × I _{S2}) + ((PCI - 3) × (I _{S1} + I _{NANO}))]/PCI			μA
Power Consumption During POR	I _{POR}	(Note 7)		100			nA
Stop-Mode Resume Time	t _{ON}			375 + (8192 × t _{HFXIN})			μs
Power-Fail Monitor Startup Time	t _{PFM_ON}	(Note 4)		150			μs
Power-Fail Warning Detection Time	t _{PFW}	(Note 8)		10			μs
Input Low Voltage for IRTX, IRRX, $\overline{\text{RESET}}$, and All Port Pins	V _{IL}			V _{GND}	0.3 × V _{DD}		V
Input High Voltage for IRTX, IRRX, $\overline{\text{RESET}}$, and All Port Pins	V _{IH}			0.7 × V _{DD}	V _{DD}		V
Input Hysteresis (Schmitt)	V _{IHYS}	V _{DD} = 3.3V, T _A = +25°C		300			mV
Input Low Voltage for HFXIN	V _{IL_HFXIN}			V _{GND}	0.3 × V _{DD}		V
Input High Voltage for HFXIN	V _{IH_HFXIN}			0.7 × V _{DD}	V _{DD}		V
IRRX Input Filter Pulse-Width Reject	t _{IRRX_R}			50			ns
IRRX Input Filter Pulse-Width Accept	t _{IRRX_A}			300			ns

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RECOMMENDED OPERATING CONDITIONS (continued)

($V_{DD} = V_{RST}$ to 3.6V, $T_A = -20^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Voltage for IRTX	V _{OL_IRTX}	V _{DD} = 3.6V, I _{OL} = 25mA (Note 4)			1.0	V
		V _{DD} = 2.35V, I _{OL} = 10mA (Note 4)			1.0	
		V _{DD} = 1.85V, I _{OL} = 4.5mA			1.0	
Output Low Voltage for $\overline{\text{RESET}}$ and All Port Pins (Note 9)	V _{OL}	V _{DD} = 3.6V, I _{OL} = 11mA (Note 4)		0.4	0.5	V
		V _{DD} = 2.35V, I _{OL} = 8mA (Note 4)		0.4	0.5	
		V _{DD} = 1.85V, I _{OL} = 4.5mA		0.4	0.5	
Output High Voltage for IRTX and All Port Pins	V _{OH}	I _{OH} = -2mA, V _{DD} = 1.85V	V _{DD} - 0.5		V _{DD}	V
Input/Output Pin Capacitance for All Port Pins	C _{IO}	(Note 4)		10		pF
Input Leakage Current	I _L	Internal pullup disabled	-100		+100	nA
Input Pullup Resistor for $\overline{\text{RESET}}$, IRTX, IRRX, P0, P1, P2	R _{PU}	V _{DD} = 3.0V, V _{OL} = 0.4V (Note 4)	16	28	39	kΩ
		V _{DD} = 2.0V, V _{OL} = 0.4V	17	30	41	
EXTERNAL CRYSTAL/RESONATOR						
Crystal/Resonator	f _{HFXIN}		1		12	MHz
Crystal/Resonator Period	t _{HFXIN}			1/f _{HFXIN}		ns
Crystal/Resonator Warmup Time	t _{XTAL_RDY}	From initial oscillation		8192 x t _{HFXIN}		ms
Oscillator Feedback Resistor	R _{OSCF}	(Note 4)	0.5	1.0	1.5	MΩ
EXTERNAL CLOCK INPUT						
External Clock Frequency	f _{XCLK}		DC		12	MHz
External Clock Period	t _{XCLK}			1/f _{XCLK}		ns
System Clock Frequency	f _{CK}			f _{HFXIN}		MHz
		HFXOUT = GND		f _{XCLK}		
System Clock Period	t _{CK}			1/f _{CK}		ns
NANOPOWER RING						
Nanopower Ring Frequency	f _{NANO}	T _A = +25°C	3.0	8.0	20.0	kHz
		T _A = +25°C, V _{DD} = POR voltage (Note 4)	1.7	2.4		
Nanopower Ring Current	I _{NANO}	Typical at V _{DD} = 1.64V, T _A = +25°C (Note 4)		40	400	nA
FLASH MEMORY (Note 10)						
System Clock During Flash Programming/Erase	f _{FPSYSCLK}		6			MHz
Flash Erase Time	t _{ME}	Mass erase	20		40	ms
	t _{ERASE}	Page erase	20		40	

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RECOMMENDED OPERATING CONDITIONS (continued)

($V_{DD} = V_{RST}$ to 3.6V, $T_A = -20^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Flash Programming Time per Word	t_{PROG}	(Note 11)	20		100	μs
Write/Erase Cycles			20,000			Cycles
Data Retention		$T_A = +25^{\circ}\text{C}$	100			Years
WAKE-UP TIMER						
Wake-Up Timer Interval	t_{WAKEUP}		$1/f_{\text{NANO}}$		65,535/ f_{NANO}	s
IR						
Carrier Frequency	f_{IR}	(Note 4)			$f_{\text{CK}}/2$	Hz

Note 1: Specifications to -20°C are guaranteed by design and are not production tested. Typical = $+25^{\circ}\text{C}$, $V_{DD} = +3.3\text{V}$, unless otherwise noted.

Note 2: V_{PFW} can be programmed to the following nominal voltage trip points: 1.8V, 1.9V, 2.55V, and $2.75\text{V} \pm 3\%$. The values listed in the [Recommended Operating Conditions](#) table are for the default configuration of 1.8V typical.

Note 3: The power-fail reset and POR detectors are designed to operate in tandem to ensure that one or both of these signals is active at all times when $V_{DD} < V_{RST}$, ensuring the device maintains the reset state until minimum operating voltage is achieved.

Note 4: Guaranteed by design and not production tested.

Note 5: Measured on the V_{DD} pin and the device not in reset. All inputs are connected to GND or V_{DD} . Outputs do not source/sink any current. The device is executing code from flash memory.

Note 6: The power-check interval (PCI) can be set to always on, or to 1024, 2048, or 4096 nanopower ring clock cycles.

Note 7: Current consumption during POR when powering up while V_{DD} is less than the POR release voltage.

Note 8: The typical amount of time that V_{DD} must be below V_{PFW} before a power-fail event is detected; refer to the *MAXQ610 User's Guide* for details.

Note 9: The maximum total current, $I_{\text{OH(MAX)}}$ and $I_{\text{OL(MAX)}}$, for all listed outputs combined should not exceed 32mA to satisfy the maximum specified voltage drop. This does not include the IRTX output.

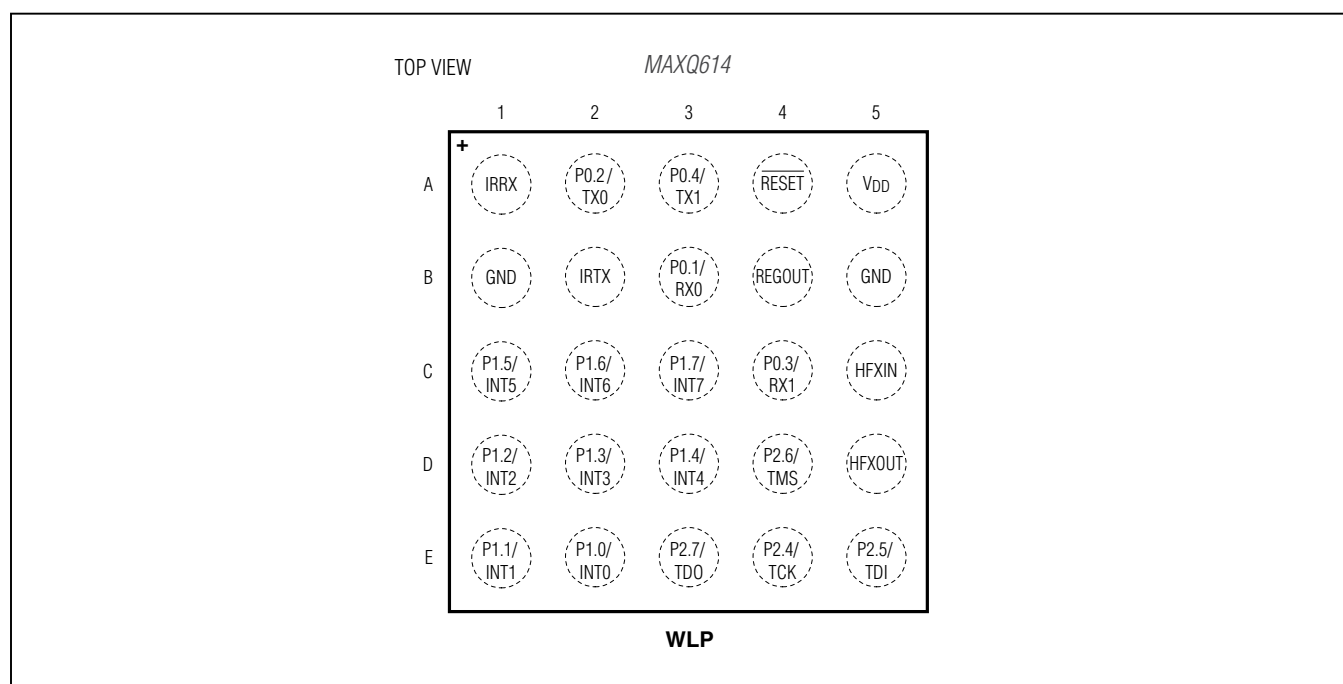
Note 10: It is not recommended to write to flash memory when the supply voltage drops below the power-fail warning levels as there is uncertainty in the duration of continuous power supply. The user application should check the status of the power-fail warning flag before writing to flash to ensure complete write operations.

Note 11: Programming time does not include overhead associated with utility ROM interface.

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Bump Configuration



Bump Description

BUMP	NAME	FUNCTION
POWER PINS		
A5	V _{DD}	Supply Voltage
B1, B5	GND	Ground. Connect directly to the ground plane.
B4	REGOUT	1.8V Regulator Output. This pin must be connected to ground through a 1.0μF external ceramic-chip capacitor. The capacitor must be placed as close as possible to this pin. No devices other than the capacitor should be connected to this pin.
RESET PINS		
A4	RESET	Digital, Active-Low Reset Input/Output. The device remains in reset as long as this pin is low and begins executing from the utility ROM at address 8000h when this pin returns to a high state. The pin includes pullup current source; if this pin is driven by an external device, it should be driven by an open-drain source capable of sinking in excess of 4mA. This pin can be left unconnected if there is no need to place the device in a reset state using an external signal. This pin is driven low as an output when an internal reset condition occurs.
CLOCK PINS		
C5	HFXIN	High-Frequency Crystal Input. Connect an external crystal or resonator between HFXIN and HFXOUT for use as the high-frequency system clock. Alternatively, HFXIN is the input for an external, high-frequency clock source when HFXOUT is connected to ground. It is recommended that a duty cycle between 45% and 55% be used if an external clock source is supplied.
D5	HFXOUT	

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Bump Description (continued)

BUMP	NAME	FUNCTION	
IR FUNCTION PINS			
B2	IRTX	IR Transmit Output. IR transmission pin capable of sinking 25mA. This pin defaults to a high-impedance input with the weak pullup disabled during all forms of reset. Software must configure this pin after release from reset to remove the high-impedance input condition.	
A1	IRRX	IR Receive Input. This pin defaults to a high-impedance input with the weak pullup disabled during all forms of reset. Software must configure this pin after release from reset to remove the high-impedance input condition.	
GENERAL-PURPOSE I/O AND SPECIAL FUNCTION PINS			
		Port 0 General-Purpose, Digital I/O Pins. These port pins function as general-purpose I/O pins with their input and output states controlled by the PD0, PO0, and PI0 registers. All port pins default to high-impedance mode after a reset. Software must configure these pins after release from reset to remove the high-impedance condition. All special functions must be enabled from software before they can be used.	
		GPIO PORT PIN	SPECIAL FUNCTION
B3	P0.1/RX0	P0.1	USART 0 Receive
A2	P0.2/TX0	P0.2	USART 0 Transmit
C4	P0.3/RX1	P0.3	USART 1 Receive
A3	P0.4/TX1	P0.4	USART 1 Transmit
		Port 1 General-Purpose, Digital I/O Pins with Interrupt Capability. These port pins function as general-purpose I/O pins with their input and output states controlled by the PD1, PO1, and PI1 registers. All port pins default to high-impedance mode after a reset. Software must configure these pins after release from reset to remove the high-impedance condition. All external interrupts must be enabled from software before they can be used.	
		GPIO PORT PIN	EXTERNAL INTERRUPT
E2	P1.0/INT0	P1.0	INT0
E1	P1.1/INT1	P1.1	INT1
D1	P1.2/INT2	P1.2	INT2
D2	P1.3/INT3	P1.3	INT3
D3	P1.4/INT4	P1.4	INT4
C1	P1.5/INT5	P1.5	INT5
C2	P1.6/INT6	P1.6	INT6
C3	P1.7/INT7	P1.7	INT7
		Port 2 General-Purpose, Digital I/O Pins. These port pins function as general-purpose I/O pins with their input and output states controlled by the PD2, PO2, and PI2 registers. All port pins default to high-impedance mode after a reset. Software must configure these pins after release from reset to remove the high-impedance condition. All special functions must be enabled from software before they can be used.	
		GPIO PORT PIN	SPECIAL FUNCTION
E4	P2.4/TCK	P2.4	JTAG: Test Clock
E5	P2.5/TDI	P2.5	JTAG: Test Data In
D4	P2.6/TMS	P2.6	JTAG: Test Mode Select
E3	P2.7/TDO	P2.7	JTAG: Test Data Out

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Detailed Description

The MAXQ614 provides integrated, low-cost solutions that simplify the design of IR communications equipment such as universal remote controls. Standard features include the highly optimized, single-cycle, MAXQ, 16-bit RISC core; 80KB flash memory; 2KB data RAM; soft stack; 16 general-purpose registers; and three data pointers. The MAXQ core has the industry's best MIPS/mA rating, allowing developers to achieve the same performance as competing microcontrollers at substantially lower clock rates. Lower active-mode current combined with the even lower MAXQ614 stop-mode current (0.2μA typ) results in increased battery life. Application-specific peripherals include flexible timers for generating IR carrier frequencies and modulation. A high-current IR drive pin capable of sinking up to 25mA current and output pins capable of sinking up to 5mA are ideal for IR applications. It also includes general-purpose I/O pins ideal for keypad matrix input, and a power-fail-detection circuit to notify the application when the supply voltage is nearing the microcontroller's minimum operating voltage.

At the heart of the device is the MAXQ 16-bit, RISC core. Operating from DC to 12MHz, almost all instructions execute in a single clock cycle (83.3ns at 12MHz), enabling nearly 12MIPS true-code operation. When active device operation is not required, an ultra-low-power stop mode can be invoked from software, resulting in quiescent current consumption of less than 0.2μA (typ) and 2.0μA (max). The combination of high-performance instructions and ultra-low stop-mode current increases battery life over competing microcontrollers. An integrated POR circuit with brownout support resets the device to a known condition following a power-up cycle or brownout condition. Additionally, a power-fail warning flag is set, and a power-fail interrupt can be generated when the system

voltage falls below the power-fail warning voltage, V_{PFW} . The power-fail warning feature allows the application to notify the user that the system supply is low and appropriate action should be taken.

Microprocessor

The device is based on Maxim's low-power, 16-bit MAXQ family of RISC cores. The core supports the Harvard memory architecture with separate 16-bit program and data address buses. A fixed 16-bit instruction word is standard, but data can be arranged in 8 or 16 bits. The MAXQ core in the device is implemented as a pipelined processor with performance approaching 1MIPS per MHz. The 16-bit data path is implemented around register modules, and each register module contributes specific functions to the core. The accumulator module consists of sixteen 16-bit registers and is tightly coupled with the arithmetic logic unit (ALU). A configurable soft stack supports program flow.

Execution of instructions is triggered by data transfer between functional register modules or between a functional register module and memory. Because data movement involves only source and destination modules, circuit switching activities are limited to active modules only. For power-conscious applications, this approach localizes power dissipation and minimizes switching noise. The modular architecture also provides a maximum of flexibility and reusability that are important for a microprocessor used in embedded applications.

The MAXQ instruction set is highly orthogonal. All arithmetical and logical operations can use any register in conjunction with the accumulator. Data movement is supported from any register to any other register. Memory is accessed through specific data-pointer registers with autoincrement/decrement support.

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Memory

The microcontroller incorporates several memory types:

- 80KB flash memory
- 2KB SRAM data memory
- 1.5KB utility ROM
- Soft stack

Stack Memory

The device provides a soft stack that can be used to store program return addresses (for subroutine calls and interrupt handling) and other general-purpose data. This soft stack is located in the 2KB SRAM data memory, which means that the SRAM data memory must be shared between the soft stack and general-purpose application data storage. However, the location and size of the soft stack is determined by the user, providing maximum flexibility when allocating resources for a particular application. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and when an interrupt is serviced. An application can also store and retrieve values explicitly using the stack by means of the PUSH, POP, and POPI instructions.

The SP pointer indicates the current top of the stack, which initializes by default to the top of the SRAM data memory. As values are pushed onto the stack, the SP pointer decrements, which means that the stack grows downward towards the bottom (lowest address) of the data memory. Popping values off the stack causes the SP pointer value to increase. Refer to the *MAXQ610 User's Guide* for more details.

Utility ROM

The utility ROM is a 1.5KB block of internal ROM memory located in program space beginning at address 8000h. This ROM includes the following routines:

- Production test routines (internal memory tests, memory loader, etc.), which are used for internal testing

only, and are generally of no use to the end-application developer

- User-callable routines for buffer copying and fast table lookup (more information on these routines can be found in the *MAXQ610 User's Guide*)

Following any reset, execution begins in the utility ROM at address 8000h. At this point, unless test mode has been invoked (which requires special programming through the JTAG interface), the utility ROM in the device always automatically jumps to location 0000h, which is the beginning of user application code.

Watchdog Timer

The internal watchdog timer greatly increases system reliability. The timer resets the device if software execution is disturbed. The watchdog timer is a free-running counter designed to be periodically reset by the application software. If software is operating correctly, the counter is periodically reset and never reaches its maximum count. However, if software operation is interrupted, the timer does not reset, triggering a system reset and optionally a watchdog timer interrupt. This protects the system against electrical noise or electrostatic discharge (ESD) upsets that could cause uncontrolled processor operation. The internal watchdog timer is an upgrade to older designs with external watchdog devices, reducing system cost and simultaneously increasing reliability.

The watchdog timer functions as the source of both the watchdog timer timeout and the watchdog timer reset. The timeout period can be programmed in a range of 2^{15} to 2^{24} system clock cycles. An interrupt is generated when the timeout period expires if the interrupt is enabled. All watchdog timer resets follow the programmed interrupt timeouts by 512 system clock cycles. If the watchdog timer is not restarted for another full interval in this time period, a system reset occurs when the reset timeout expires. See [Table 1](#).

Table 1. Watchdog Interrupt Timeout (Sysclk = 12MHz, CD[1:0] = 00)

WD[1:0]	WATCHDOG CLOCK	WATCHDOG INTERRUPT TIMEOUT	WATCHDOG RESET AFTER WATCHDOG INTERRUPT (μs)
00	Sysclk/ 2^{15}	2.7ms	42.7
01	Sysclk/ 2^{18}	21.9ms	42.7
10	Sysclk/ 2^{21}	174.7ms	42.7
11	Sysclk/ 2^{24}	1.4s	42.7

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IR Carrier Generation and Modulation Timer

The dedicated IR timer/counter module simplifies low-speed infrared (IR) communication. The IR timer implements two pins (IRTX and IRRX) for supporting IR transmit and receive, respectively. The IRTX pin has no corresponding port pin designation, so the standard PD, PO, and PI port control status bits are not present. However, the IRTX pin output can be manipulated high or low using the PWCN.IRTXOUT and PWCN.IRTXOE bits when the IR timer is not enabled (i.e., IREN = 0).

The IR timer is composed of a carrier generator and a carrier modulator. The carrier generation module uses the 16-bit IR carrier register (IRCA) to define the high and low time of the carrier through the IR carrier high byte (IRCAH) and IR carrier low byte (IRCAL). The carrier modulator uses the IR data bit (IRDATA) and IR modulator time register (IRMT) to determine whether the carrier or the idle condition is present on IRTX.

The IR timer is enabled when the IR enable bit (IREN) is set to 1. The IR Value register (IRV) defines the beginning value for the carrier modulator. During transmission, the IRV register is initially loaded with the IRMT value and begins down counting towards 0000h, whereas in receive mode it counts upward from the initial IRV register value. During the receive operation, the IRV register can be configured to reload with 0000h when capture occurs on detection of selected edges or can be allowed to continue free-running throughout the receive operation. An overflow occurs when the IR timer value rolls over from 0FFFFh to 0000h. The IR overflow flag (IROV) is set to 1 and an interrupt is generated if enabled (IRIE = 1).

Carrier Generation Module

The IRCAH byte defines the carrier high time in terms of the number of IR input clocks, whereas the IRCAL byte defines the carrier low time.

- IR Input Clock (f_{IRCLK}) = $f_{SYS}/2^{IRDIV[1:0]}$
- Carrier Frequency ($f_{CARRIER}$) = $f_{IRCLK}/(IRCAH + IRCAL + 2)$
- Carrier High Time = $IRCAH + 1$
- Carrier Low Time = $IRCAL + 1$
- Carrier Duty Cycle = $(IRCAH + 1)/(IRCAH + IRCAL + 2)$

During transmission, the IRCA register is latched for each IRV down-count interval, and is sampled along with the IRTXPOL and IRDATA bits at the beginning of each new IRV down-count interval so that duty-cycle variation and

frequency shifting is possible from one interval to the next, which is illustrated in [Figure 1](#).

[Figure 2](#) illustrates the basic carrier generation and its path to the IRTX output pin. The IR transmit polarity bit (IRTXPOL) defines the starting/idle state and the carrier polarity of the IRTX pin when the IR timer is enabled.

IR Transmission

During IR transmission (IRMODE = 1), the carrier generator creates the appropriate carrier waveform, while the carrier modulator performs the modulation. The carrier modulation can be performed as a function of carrier cycles or IRCLK cycles dependent on the setting of the IRCFME bit. When IRCFME = 0, the IRV down counter is clocked by the carrier frequency and thus the modulation is a function of carrier cycles. When IRCFME = 1, the IRV down counter is clocked by IRCLK, allowing carrier modulation timing with IRCLK resolution.

The IRTXPOL bit defines the starting/idle state as well as the carrier polarity for the IRTX pin. If IRTXPOL = 1, the IRTX pin is set to a logic-high when the IR timer module is enabled. If IRTXPOL = 0, the IRTX pin is set to a logic-low when the IR timer is enabled.

A separate register bit, IR data (IRDATA), is used to determine whether the carrier generator output is output to the IRTX pin for the next IRMT carrier cycles. When IRDATA = 1, the carrier waveform (or inversion of this waveform if IRTXPOL = 1) is output on the IRTX pin during the next IRMT cycles. When IRDATA = 0, the idle condition, as defined by IRTXPOL, is output on the IRTX pin during the next IRMT cycles.

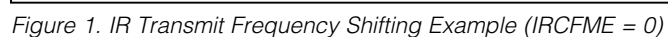
The IR timer acts as a down counter in transmit mode. An IR transmission starts when the IREN bit is set to 1 when IRMODE = 1; when the IRMODE bit is set to 1 when IREN = 1; or when IREN and IRMODE are both set to 1 in the same instruction. The IRMT and IRCA registers, along with the IRDATA and IRTXPOL bits, are sampled at the beginning of the transmit process and every time the IR timer value reload its value. When the IRV reaches 0000h value, on the next carrier clock, it does the following:

- 1) Reloads IRV with IRMT.
- 2) Samples IRCA, IRDATA, and IRTXPOL.
- 3) Generates IRTX accordingly.
- 4) Sets IRIF to 1.
- 5) Generates an interrupt to the CPU if enabled (IRIE = 1).

To terminate the current transmission, the user can switch to receive mode (IRMODE = 0) or clear IREN to 0.

$$\text{Carrier Modulation Time} = \text{IRMT} + 1 \text{ carrier cycles}$$

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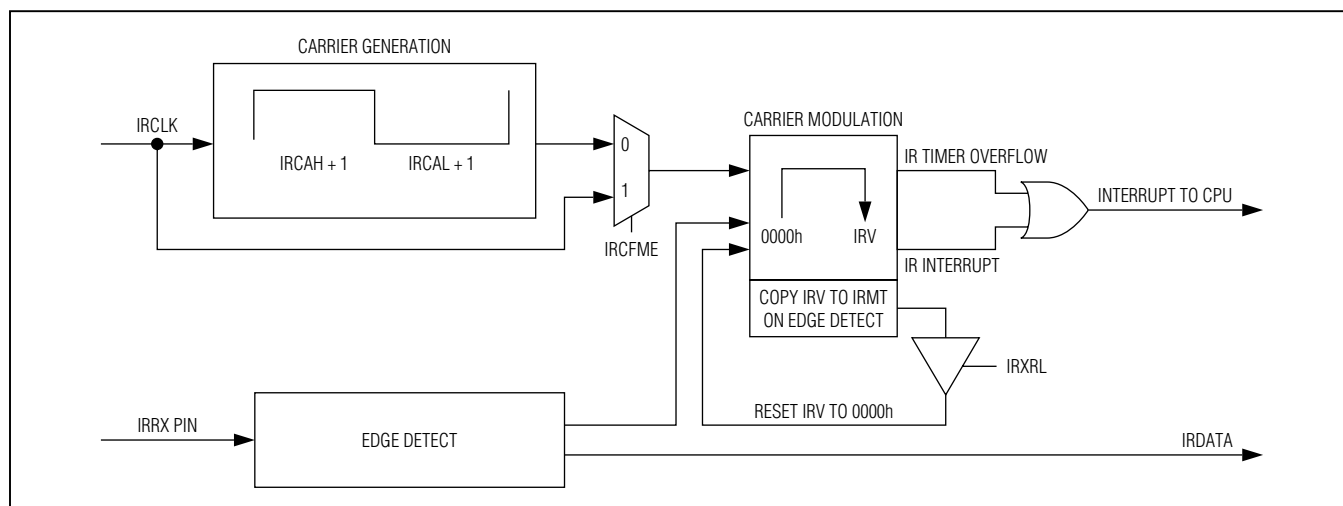


Figure 3. IR Capture

IR Receive

When configured in receive mode ($\text{IRMODE} = 0$), the IR hardware supports the IRRX capture function. The $\text{IRRXSEL}[1:0]$ bits define which edge(s) of the IRRX pin should trigger the IR timer capture function.

The IR module starts operating in the receive mode when $\text{IRMODE} = 0$ and $\text{IREN} = 1$. Once started, the IR timer (IRV) starts up counting from 0000h when a qualified capture event as defined by IRRXSEL happens. The IRV register is, by default, counting carrier cycles as defined by the IRCA register. However, the IR carrier frequency detect (IRCFME) bit can be set to 1 to allow clocking of the IRV register directly with the IRCLK for finer resolution. When $\text{IRCFME} = 0$, the IRCA defined carrier is counted by IRV. When $\text{IRCFME} = 1$, the IRCLK clocks the IRV register.

On the next qualified event, the IR module does the following:

- 1) Captures the IRRX pin state and transfers its value to IRDATA. If a falling edge occurs, $\text{IRDATA} = 0$. If a rising edge occurs, $\text{IRDATA} = 1$.
- 2) Transfers its current IRV value to the IRMT.
- 3) Resets IRV content to 0000h (if $\text{IRXRL} = 1$).
- 4) Continues counting again until the next qualified event.

If the IR timer value rolls over from 0FFFFh to 0000h before a qualified event happens, the IR timer overflow (IROV) flag is set to 1 and an interrupt is generated, if

enabled. The IR module continues to operate in receive mode until it is stopped by switching into transmit mode ($\text{IRMODE} = 1$) or clearing $\text{IREN} = 0$.

Carrier Burst-Count Mode

A special mode reduces the CPU processing burden when performing IR learning functions. Typically, when operating in an IR learning capacity, some number of carrier cycles are examined for frequency determination. Once the frequency has been determined, the IR receive function can be reduced to counting the number of carrier pulses in the burst and the duration of the combined mark-space time within the burst. To simplify this process, the receive burst-count mode (as enabled by the RXBCNT bit) can be used. When $\text{RXBCNT} = 0$, the standard IR receive capture functionality is in place. When $\text{RXBCNT} = 1$, the IRV capture operation is disabled and the interrupt flag associated with the capture no longer denotes a capture. In the carrier burst-count mode, the IRMT register only counts qualified edges. The IRIF interrupt flag (normally used to signal a capture when $\text{RXBCNT} = 0$) now becomes set if two IRCA cycles elapse without getting a qualified edge. The IRIF interrupt flag thus denotes absence of the carrier and the beginning of a space in the receive signal. When the RXBCNT bit is changed from 0 to 1, the IRMT register is set to 0001h. The IRCFME bit is still used to define whether the IRV register is counting system IRCLK clocks or IRCA-defined carrier cycles. The IRXRL bit defines whether the IRV register is reloaded with 0000h on detection of

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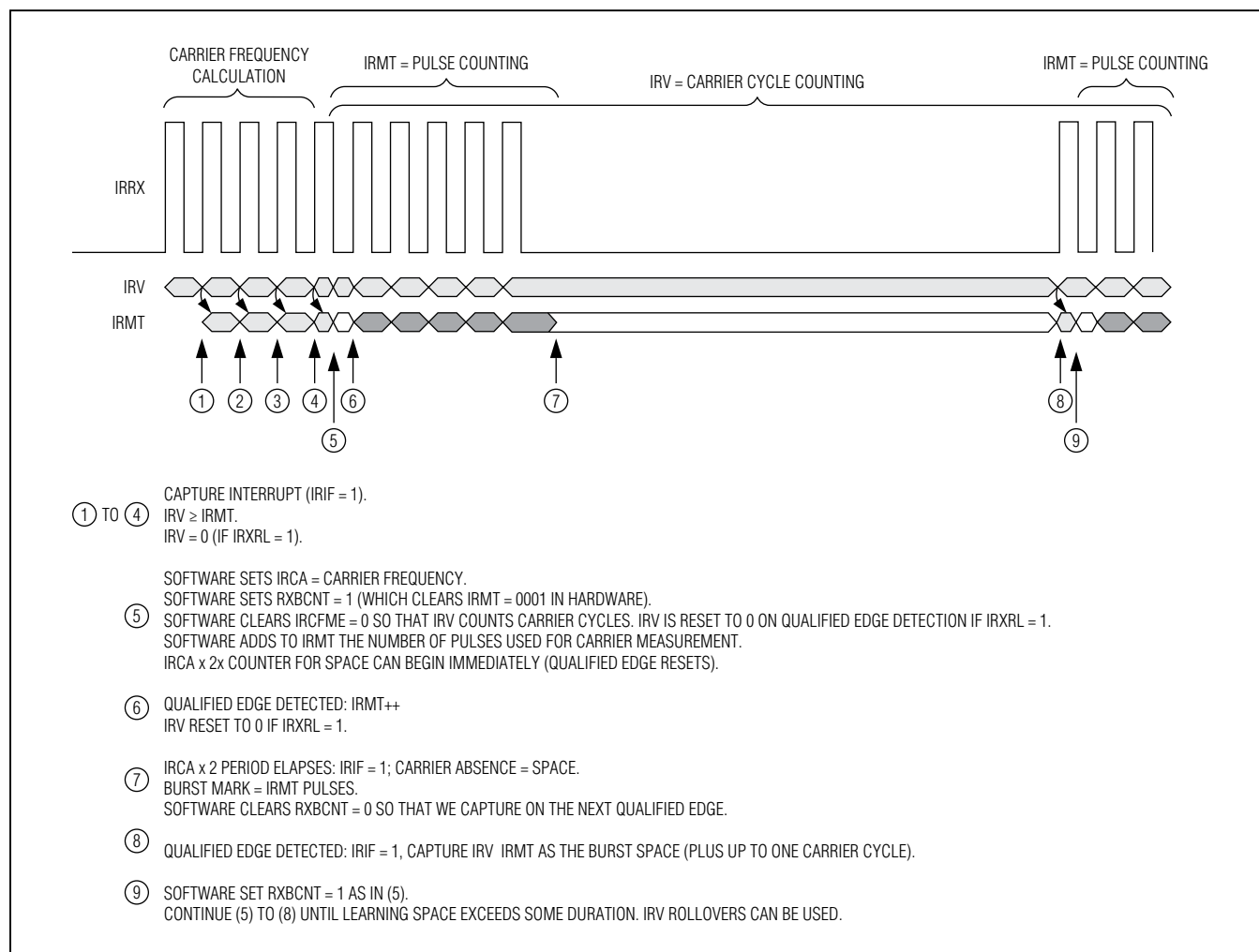


Figure 4. Receive Burst-Count Example

a qualified edge (per the IRXSEL[1:0] bits). [Figure 4](#) and the descriptive sequence embedded in the figure illustrate the expected usage of the receive burst-count mode.

16-Bit Timers/Counters

The microcontroller provides two timers/counters that support the following functions:

- 16-bit timer/counter

- 16-bit up/down autoreload
- Counter function of external pulse
- 16-bit timer with capture
- 16-bit timer with compare
- Input/output enhancements for pulse-width modulation
- Set/reset/toggle output state on comparator match
- Prescaler with 2^n divider (for $n = 0, 2, 4, 6, 8, 10$)

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USART

The device provides two USART peripherals with the following features:

- 2-wire interface
- Full-duplex operation for asynchronous data transfers
- Half-duplex operation for synchronous data transfers
- Programmable interrupt when transmit or receive data operation completes
- Independent programmable baud-rate generator
- Optional 9th bit parity support
- Start/stop bit support

General-Purpose I/O

The microcontroller provides port pins for general-purpose I/O that have the following features:

- CMOS output drivers
- Schmitt trigger inputs
- Optional weak pullup to V_{DD} when operating in input mode

While the microcontroller is in a reset state, all port pins become high impedance with both weak pullups and input buffers disabled, unless otherwise noted.

From a software perspective, each port appears as a group of peripheral registers with unique addresses. Special function pins can also be used as general-purpose I/O pins when the special functions are disabled. For a detailed description of the special functions available for each pin, refer to the *MAXQ610 User's Guide*.

On-Chip Oscillator

An external quartz crystal or a ceramic resonator can be connected between HFXIN and HFXOUT, as illustrated in [Figure 5](#).

Noise at HFXIN and HFXOUT can adversely affect on-chip clock timing. It is good design practice to place the crystal and capacitors near the oscillator circuitry and connect HFXIN and HFXOUT to ground with a direct short trace. The typical values of external capacitors vary with the type of crystal to be used and should be initially selected based on load capacitance as suggested by the manufacturer.

Operating Modes

The lowest power mode of operation is stop mode. In this mode, CPU state and memories are preserved, but the CPU is not actively running. Wake-up sources include external I/O interrupts, the power-fail warning interrupt, wake-up timer, or a power-fail reset. Any time the microcontroller is in a state where code does not need to be executed, the user software can put the device into stop mode. The nanopower ring oscillator is an internal ultra-low-power (400nA) 8kHz ring oscillator that can be used to drive a wake-up timer that exits stop mode. The wake-up timer is programmable by software in steps of 125μs up to approximately 8s.

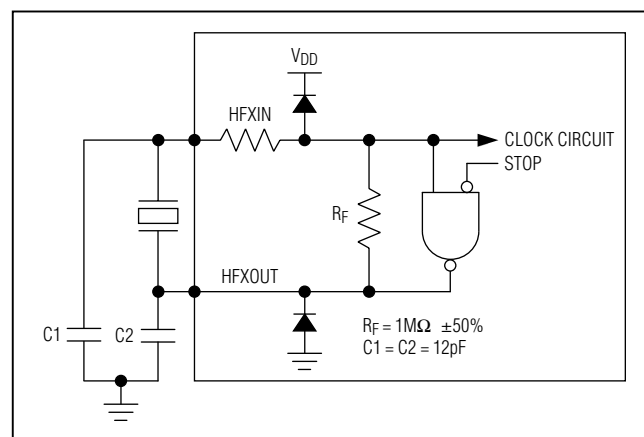


Figure 5. On-Chip Oscillator

Table 2. USART Mode Details

MODE	TYPE	START BITS	DATA BITS	STOP BITS
Mode 0	Synchronous	N/A	8	N/A
Mode 1	Asynchronous	1	8	1
Mode 2	Asynchronous	1	8 + 1	1
Mode 3	Asynchronous	1	8 + 1	1

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The MAXQ614 is a reduced pin count version of the MAXQ618 microcontroller. To ensure all nonbonded output pins power up in a known state and to prevent unnecessary leakage during stop mode, the following port pins should be set as inputs with weak pullup in application software when the device exits a power-on reset condition:

- P0.5, P0.6, P0.7
- P0.0
- P2.0 to P2.3
- P3.0 to P3.7

The power-fail monitor is always on during normal operation. However, it can be selectively disabled during stop mode to minimize power consumption. This feature is enabled using the power-fail monitor disable (PFD) bit in the PWCN register. The reset default state for the PFD bit is 1, which disables the power-fail monitor function during stop mode. If power-fail monitoring is disabled (PFD = 1) during stop mode, the circuitry responsible for generating a power-fail warning or reset is shut down and neither condition is detected. Thus, the $V_{DD} < V_{RST}$ condition does not invoke a reset state.

Power-Fail Detection

Figure 6, Figure 7, Figure 8 show the power-fail detection and response during normal and stop-mode operation. If a reset is caused by a power-fail, the power-fail monitor can be set to one of the following intervals:

- Always on—continuous monitoring
- 2¹¹ nanopower ring oscillator clocks (~256ms)
- 2¹² nanopower ring oscillator clocks (~512ms)
- 2¹³ nanopower ring oscillator clocks (~1.024s)

In the case where the power-fail circuitry is periodically turned on, the power-fail detection is turned on for two nanopower ring-oscillator cycles. If $V_{DD} > V_{RST}$ during detection, V_{DD} is monitored for an additional nanopower ring-oscillator period. If V_{DD} remains above V_{RST} for the third nanopower ring period, the CPU exits the reset state and resumes normal operation from utility ROM at 8000h after satisfying the crystal warmup period.

If a reset is generated by any other event, such as the RESET pin being driven low externally or the watch-dog timer, the power-fail, internal regulator, and crystal remain on during the CPU reset. In these cases, the CPU exits the reset state in less than 20 crystal cycles after the reset source is removed.

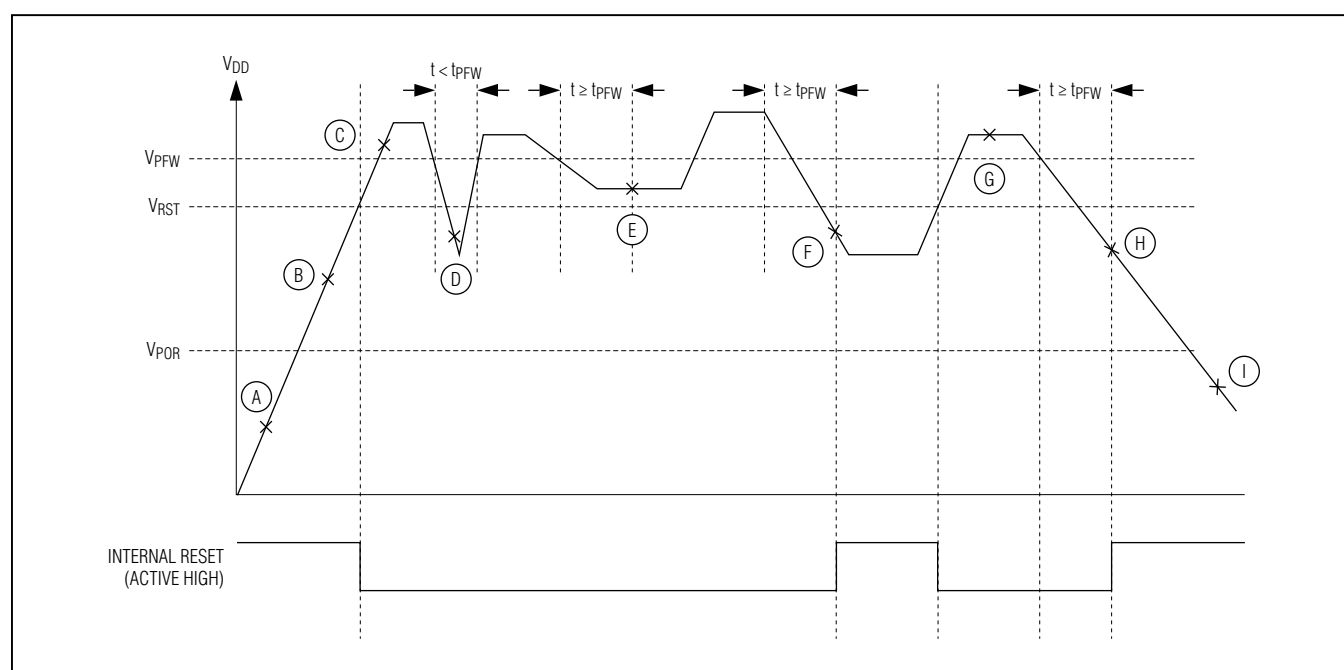


Figure 6. Power-Fail Detection During Normal Operation

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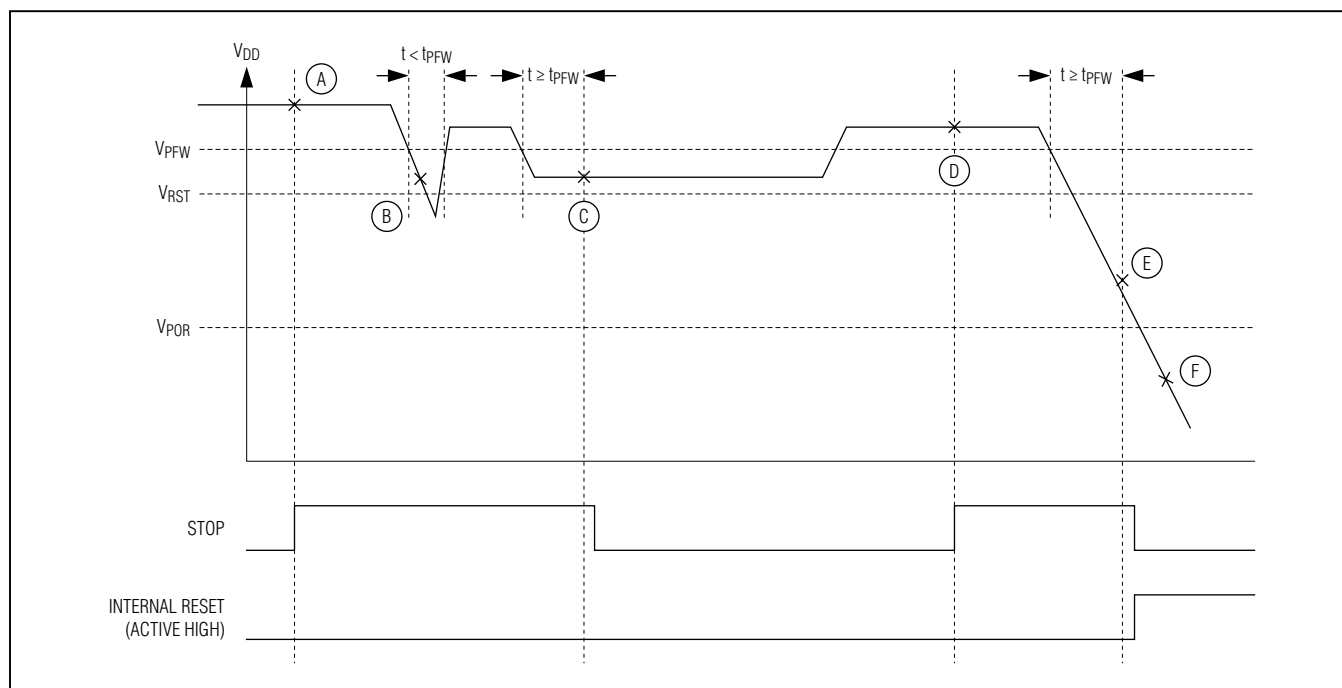


Figure 7. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

Table 4. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	On	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
B	On	Off	Off	Yes	Power drop too short. Power-fail not detected.
C	On	On	On	Yes	$V_{RST} < V_{DD} < V_{PPFW}$. Power-fail warning detected. Turn on regulator and crystal. Crystal warmup time, t_{XTAL_RDY} . Exit stop mode.
D	On	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
E	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor turns on periodically.
F	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

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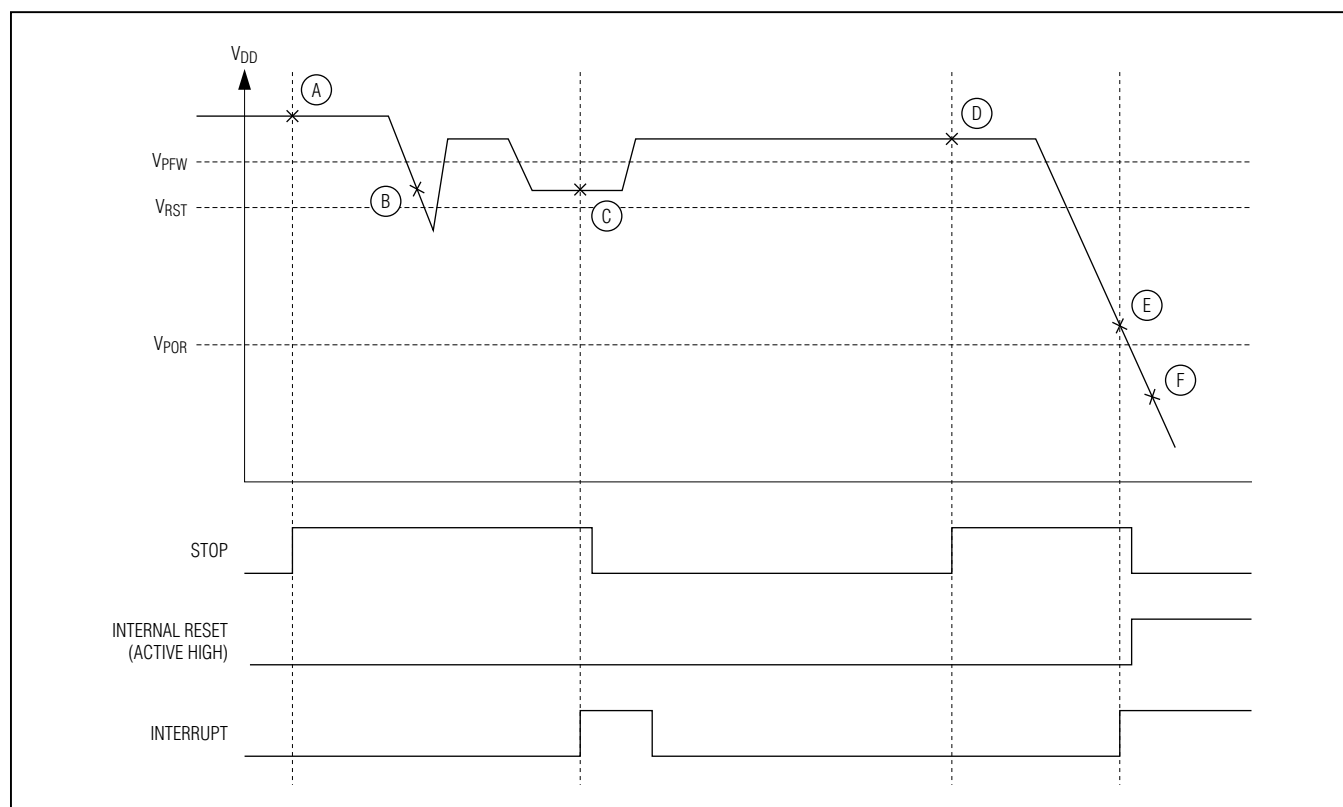


Figure 8. Stop Mode Power-Fail Detection with Power-Fail Monitor Disabled

Table 5. Stop Mode Power-Fail Detection States with Power-Fail Monitor Disabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	Off	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
B	Off	Off	Off	Yes	$V_{DD} < V_{PFW}$. Power-fail not detected because the power-fail monitor is disabled.
C	On	On	On	Yes	$V_{RST} < V_{DD} < V_{PFW}$. An interrupt occurs that causes the CPU to exit stop mode. Power-fail monitor is turned on, detects a power-fail warning, and sets the power-fail interrupt flag. Turn on regulator and crystal. Crystal warmup time, t_{XTAL_RDY} . On stop mode exit, CPU vectors to the higher priority of power-fail and the interrupt that causes stop mode exit.

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Table 5. Stop Mode Power-Fail Detection States with Power-Fail Monitor Disabled (continued)

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
D	Off	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
E	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. An interrupt occurs that causes the CPU to exit stop mode. Power-fail monitor is turned on, detects a power-fail, and puts CPU in reset. Power-fail monitor is turned on periodically.
F	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

Applications Information

The low-power, high-performance RISC architecture of this device makes it an excellent fit for many portable or battery-powered applications. It is ideally suited for applications such as universal remote controls that require the cost-effective integration of IR transmit/receive capability.

Grounds and Bypassing

Careful PCB layout significantly minimizes system-level digital noise that could interact with the microcontroller or peripheral components. The use of multilayer boards is essential to allow the use of dedicated power planes. The area under any digital components should be a continuous ground plane if possible. Keep bypass capacitor leads short for best noise rejection and place the capacitors as close as possible to the leads of the devices.

CMOS design guidelines for any semiconductor require that no pin be taken above V_{DD} or below GND. Violation of this guideline can result in a hard failure (damage to the silicon inside the device) or a soft failure (unintentional modification of memory contents). Voltage spikes above or below the device's absolute maximum ratings can potentially cause a devastating IC latchup.

Microcontrollers commonly experience negative voltage spikes through either their power pins or general-purpose I/O pins. Negative voltage spikes on power pins are especially problematic as they directly couple to the internal power buses. Devices such as keypads can conduct electrostatic discharges directly into the microcontroller and seriously damage the device. System designers must protect components against these transients that can corrupt system memory.

Additional Documentation

Designers must have the following documents to fully use all the features of this device. This data sheet contains pin descriptions, feature overviews, and electrical specifications. Errata sheets contain deviations from published specifications. The user's guides offer detailed information about device features and operation.

- This MAXQ614 data sheet, which contains electrical/timing specifications, pin descriptions, and package information.
- The MAXQ614 revision-specific errata sheet (www.maximintegrated.com/errata).
- The MAXQ610 User's Guide, which contains detailed information on features and operation, including programming.

MAXQ614

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Deviations from the MAXQ610 User's Guide for the MAXQ614

The MAXQ610 User's Guide contains all the information that is needed to develop application code for the MAXQ614 microcontroller. However, even though the MAXQ610 and the MAXQ614 are largely code-compatible, there are certain differences between the two devices that must be kept in mind when referring to the MAXQ610 User's Guide.

The following registers on the MAXQ610 (which are described in the MAXQ610 User's Guide) do not exist on the MAXQ614, and all references to them should be disregarded:

- Port 4 Output Register (PO4)
- Port 4 Direction Register (PD4)
- Port 4 Input Register (PI4)

Development and Technical Support

Maxim and third-party suppliers provide a variety of highly versatile, affordably priced development tools for this microcontroller, including the following:

- Compilers
- In-circuit emulators
- Integrated Development Environments (IDEs)
- Serial-to-JTAG and USB-to-JTAG interface boards for programming and debugging (for microcontrollers with rewritable memory)

A partial list of development tool vendors can be found at www.maximintegrated.com/MAXQ_tools.

For technical support, go to <https://support.maximintegrated.com/micro>.

Ordering Information/Selector Guide

PART	TEMP RANGE	OPERATING VOLTAGE (V)	PROGRAM MEMORY (KB)	DATA MEMORY (KB)	GPIO	PIN-PACKAGE
MAXQ614V-XXXX+T	-20°C to +70°C	1.7 to 3.6	80 Flash	2	16	25 WLP

Note: The 4-digit suffix “-XXXX” indicates a device preprogrammed at Maxim with proprietary customer-supplied software. For more information on factory preprogramming of these devices, contact Maxim at <https://support.maximintegrated.com/micro>.

+Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
25 WLP	W251A2+1	21-0630	Refer to Application Note 1891

MAXQ614

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/12	Initial release	—
1	9/12	Changed the operating temperature range from 0°C to +70°C to -20°C to +70°C	1, 4, 5, 21
2	10/12	Added MAXQ614V-L000+T to <i>Ordering Information</i>	21



Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

Maxim Integrated 160 Rio Robles, San Jose, CA 95134 USA 1-408-601-1000

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