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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

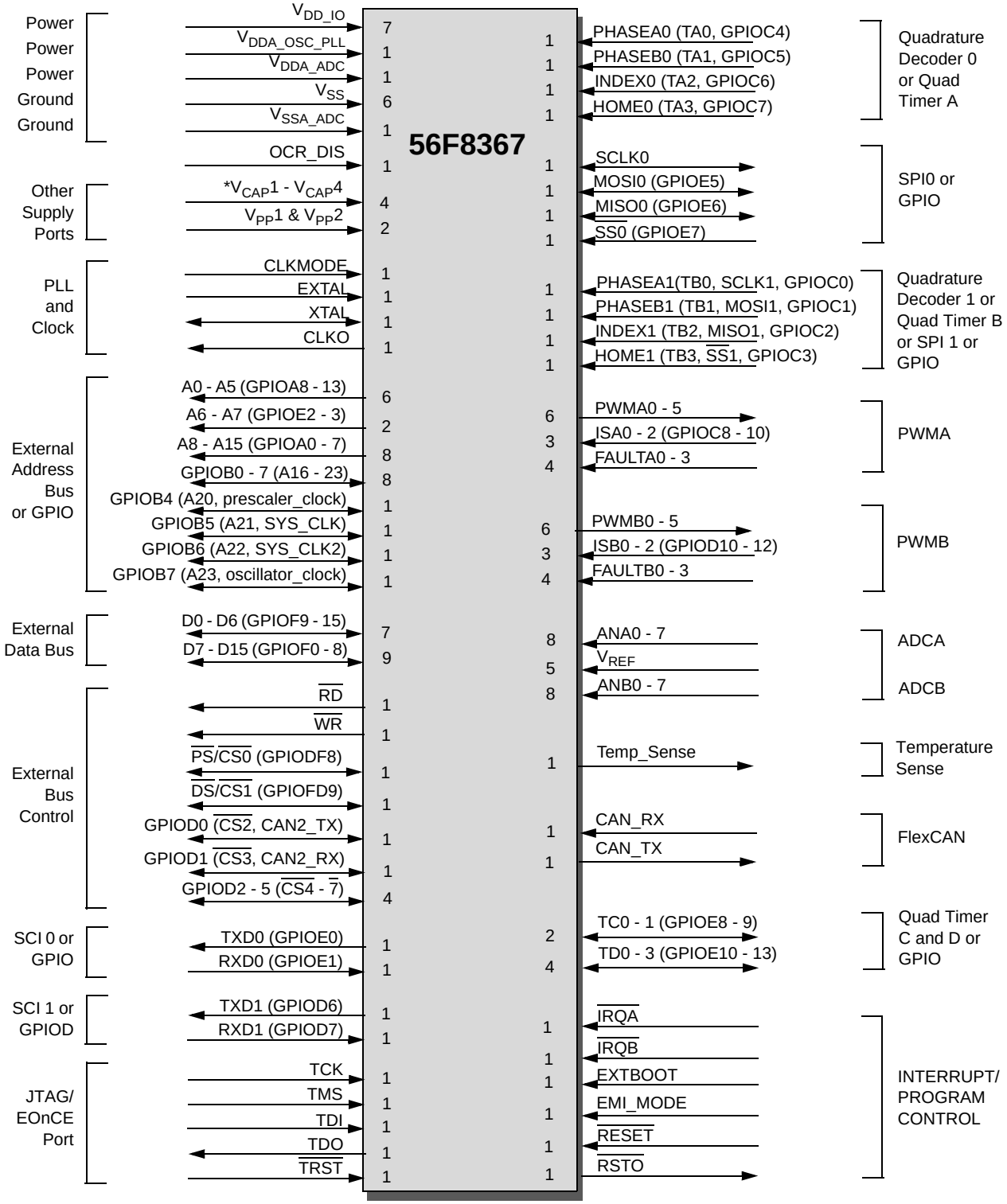
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	76
Program Memory Size	512KB (256K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	18K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LQFP
Supplier Device Package	160-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8367mpye

Table 1-2 Bus Signal Names

Name	Function
Program Memory Interface	
pdb_m[15:0]	Program data bus for instruction word fetches or read operations.
cdbw[15:0]	Primary core data bus used for program memory writes. (Only these 16 bits of the cdbw[31:0] bus are used for writes to program memory.)
pab[20:0]	Program memory address bus. Data is returned on pdb_m bus.
Primary Data Memory Interface Bus	
cdbr_m[31:0]	Primary core data bus for memory reads. Addressed via xab1 bus.
cdbw[31:0]	Primary core data bus for memory writes. Addressed via xab1 bus.
xab1[23:0]	Primary data address bus. Capable of addressing bytes[1], words, and long data types. Data is written on cdbw and returned on cdbr_m. Also used to access memory-mapped I/O.
Secondary Data Memory Interface	
xdb2_m[15:0]	Secondary data bus used for secondary data address bus xab2 in the dual memory reads.
xab2[23:0]	Secondary data address bus used for the second of two simultaneous accesses. Capable of addressing only words. Data is returned on xdb2_m.
Peripheral Interface Bus	
IPBus [15:0]	Peripheral bus accesses all on-chip peripherals registers. This bus operates at the same clock rate as the Primary Data Memory and therefore generates no delays when accessing the processor. Write data is obtained from cdbw. Read data is provided to cdbr_m.

1. Byte accesses can only occur in the bottom half of the memory address space. The MSB of the address will be forced to 0.



* When the on-chip regulator is disabled, these four pins become 2.5V V_{DD_CORE}.

Figure 2-1 56F8367 Signals Identified by Functional Group[1] (160-pin LQFP)

1. Alternate pin functionality is shown in parenthesis; pin direction/type shown is the default functionality.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
GPIOB0 **(A16)**	33	L1	Schmitt Input/ Output Output	Input, pull-up enabled	**Port B GPIO** — These four GPIO pins can be programmed as input or output pins. **Address Bus** — A16 - A19 specify one of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A16 - A19 and EMI control signals are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. After reset, the startup state of GPIOB0 - GPIOB3 (GPIO or address) is determined as a function of EXTBOOT, EMI_MODE and the Flash security setting. See **Table 4-4** for further information on when this pin is configured as an address pin at reset. In all cases, this state may be changed by writing to GPIOB_PER. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOB_PUR register.
GPIOB1 **(A17)**	34	L3			
GPIOB2 **(A18)**	35	L2			
GPIOB3 **(A19)**	36	M1			
GPIOB4 **(A20)**	37	M2	Schmitt Input/ Output Output	Input, pull-up enabled	**Port B GPIO** — These four GPIO pins can be programmed as input or output pins. **Address Bus** — A20 - A23 specify one of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A20–A23 and EMI control signals are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. **Clock Outputs** — can be used to monitor the prescaler_clock, SYS_CLK, SYS_CLK2 or oscillator_clock on GPIOB4 through GPIOB7, respectively. After reset, the default state is GPIO. These pins can also be used to extend the external address bus to its full length or to view any of several system clocks. In these cases, the GPIO_B_PER can be used to individually disable the GPIO. The CLKOSR register in the SIM (see **Part 6.5.7**) can then be used to choose between address and clock functions.
(prescaler_ clock)			Output		
GPIOB5 **(A21)** **(SYS_CLK)**	46	N4			
GPIOB6 **(A22)** **(SYS_CLK2)**	47	P3			
GPIOB7 **(A23)** **(oscillator_ clock)**	48	M4			

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
INDEX0 **(TA2)** **(GPOPC6)**	157	A1	Schmitt Input Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**Index** — Quadrature Decoder 0, INDEX input **TA2** — Timer A, Channel 2 **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is INDEX0. To deactivate the internal pull-up resistor, clear bit 6 of the GPIOC_PUR register.
HOME0 **(TA3)** **(GPIOC7)**	158	B3	Schmitt Input Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**Home** — Quadrature Decoder 0, HOME input **TA3** — Timer A, Channel 3 **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is HOME0. To deactivate the internal pull-up resistor, clear bit 7 of the GPIOC_PUR register.
SCLK0 **(GPIOE4)**	146	A6	Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**SPI 0 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCLK0. To deactivate the internal pull-up resistor, clear bit 4 in the GPIOE_PUR register.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
PHASEA1	6	C1	Schmitt Input	Input, pull-up enabled	**Phase A1** — Quadrature Decoder 1, PHASEA input for decoder 1.
(TB0)			Schmitt Input/ Output		**TB0** — Timer B, Channel 0
(SCLK1)			Schmitt Input/ Output		**SPI 1 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. To activate the SPI function, set the PHSA_ALT bit in the SIM_GPS register. For details, see **Part 6.5.8**.
(GPIOC0)			Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8367, the default state after reset is PHASEA1. In the 56F8167, the default state is not one of the functions offered and must be reconfigured. To deactivate the internal pull-up resistor, clear bit 0 in the GPIOC_PUR register.
PHASEB1	7	D1	Schmitt Input	Input, pull-up enabled	**Phase B1** — Quadrature Decoder 1, PHASEB input for decoder 1.
(TB1)			Schmitt Input/ Output		**TB1** — Timer B, Channel 1
(MOSI1)			Schmitt Input/ Output		**SPI 1 Master Out/Slave In** — This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data. To activate the SPI function, set the PHSB_ALT bit in the SIM_GPS register. For details, see **Part 6.5.8**.
(GPIOC1)			Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8367, the default state after reset is PHASEB1. In the 56F8167, the default state is not one of the functions offered and must be reconfigured. To deactivate the internal pull-up resistor, clear bit 1 in the GPIOC_PUR register.

Table 4-14 Quad Timer D Registers Address Map (Continued) (TMRD_BASE = $00 F100)

Quad Timer D is NOT available in the 56F8167 device

Register Acronym	Address Offset	Register Description
TMRD3_CMP1	$30	Compare Register 1
TMRD3_CMP2	$31	Compare Register 2
TMRD3_CAP	$32	Capture Register
TMRD3_LOAD	$33	Load Register
TMRD3_HOLD	$34	Hold Register
TMRD3_CNTR	$35	Counter Register
TMRD3_CTRL	$36	Control Register
TMRD3_SCR	$37	Status and Control Register
TMRD3_CMPLD1	$38	Comparator Load Register 1
TMRD3_CMPLD2	$39	Comparator Load Register 2
TMRD3_COMSCR	$3A	Comparator Status and Control Register

Table 4-15 Pulse Width Modulator A Registers Address Map (PWMA_BASE = $00 F140)

PWMA is NOT available in the 56F8167 device

Register Acronym	Address Offset	Register Description
PWMA_PMCTL	$0	Control Register
PWMA_PMFCTL	$1	Fault Control Register
PWMA_PMFSA	$2	Fault Status Acknowledge Register
PWMA_PMOUT	$3	Output Control Register
PWMA_PMCNT	$4	Counter Register
PWMA_PWMCM	$5	Counter Modulo Register
PWMA_PWMVAL0	$6	Value Register 0
PWMA_PWMVAL1	$7	Value Register 1
PWMA_PWMVAL2	$8	Value Register 2
PWMA_PWMVAL3	$9	Value Register 3
PWMA_PWMVAL4	$A	Value Register 4
PWMA_PWMVAL5	$B	Value Register 5
PWMA_PMDEADTM	$C	Dead Time Register
PWMA_PMDISMAP1	$D	Disable Mapping Register 1
PWMA_PMDISMAP2	$E	Disable Mapping Register 2
PWMA_PMCFG	$F	Configure Register
PWMA_PMCCR	$10	Channel Control Register

Table 4-38 FlexCAN Registers Address Map (Continued)
(FC_BASE = $00 F800)
FlexCAN is NOT available in the 56F8167 device

Register Acronym	Address Offset	Register Description
FCMB5_DATA	$6D	Message Buffer 5 Data Register
FCMB5_DATA	$6E	Message Buffer 5 Data Register
		Reserved
FCMB6_CONTROL	$70	Message Buffer 6 Control / Status Register
FCMB6_ID_HIGH	$71	Message Buffer 6 ID High Register
FCMB6_ID_LOW	$72	Message Buffer 6 ID Low Register
FCMB6_DATA	$73	Message Buffer 6 Data Register
FCMB6_DATA	$74	Message Buffer 6 Data Register
FCMB6_DATA	$75	Message Buffer 6 Data Register
FCMB6_DATA	$76	Message Buffer 6 Data Register
		Reserved
FCMB7_CONTROL	$78	Message Buffer 7 Control / Status Register
FCMB7_ID_HIGH	$79	Message Buffer 7 ID High Register
FCMB7_ID_LOW	$7A	Message Buffer 7 ID Low Register
FCMB7_DATA	$7B	Message Buffer 7 Data Register
FCMB7_DATA	$7C	Message Buffer 7 Data Register
FCMB7_DATA	$7D	Message Buffer 7 Data Register
FCMB7_DATA	$7E	Message Buffer 7 Data Register
		Reserved
FCMB8_CONTROL	$80	Message Buffer 8 Control / Status Register
FCMB8_ID_HIGH	$81	Message Buffer 8 ID High Register
FCMB8_ID_LOW	$82	Message Buffer 8 ID Low Register
FCMB8_DATA	$83	Message Buffer 8 Data Register
FCMB8_DATA	$84	Message Buffer 8 Data Register
FCMB8_DATA	$85	Message Buffer 8 Data Register
FCMB8_DATA	$86	Message Buffer 8 Data Register
		Reserved
FCMB9_CONTROL	$88	Message Buffer 9 Control / Status Register
FCMB9_ID_HIGH	$89	Message Buffer 9 ID High Register
FCMB9_ID_LOW	$8A	Message Buffer 9 ID Low Register
FCMB9_DATA	$8B	Message Buffer 9 Data Register
FCMB9_DATA	$8C	Message Buffer 9 Data Register

Table 4-39 FlexCAN2 Registers Address Map (Continued)
(FC2_BASE = $00 FA00)
FlexCAN2 is NOT available in the 56F8167 device

Register Acronym	Address Offset	Register Description
FC2MB11_DATA	$9C	Message Buffer 11 Data Register
FC2MB11_DATA	$9D	Message Buffer 11 Data Register
FC2MB11_DATA	$9E	Message Buffer 11 Data Register
		Reserved
FC2MB12_CONTROL	$A0	Message Buffer 12 Control / Status Register
FC2MB12_ID_HIGH	$A1	Message Buffer 12 ID High Register
FC2MB12_ID_LOW	$A2	Message Buffer 12 ID Low Register
FC2MB12_DATA	$A3	Message Buffer 12 Data Register
FC2MB12_DATA	$A4	Message Buffer 12 Data Register
FC2MB12_DATA	$A5	Message Buffer 12 Data Register
FC2MB12_DATA	$A6	Message Buffer 12 Data Register
		Reserved
FC2MB13_CONTROL	$A8	Message Buffer 13 Control / Status Register
FC2MB13_ID_HIGH	$A9	Message Buffer 13 ID High Register
FC2MB13_ID_LOW	$AA	Message Buffer 13 ID Low Register
FC2MB13_DATA	$AB	Message Buffer 13 Data Register
FC2MB13_DATA	$AC	Message Buffer 13 Data Register
FC2MB13_DATA	$AD	Message Buffer 13 Data Register
FC2MB13_DATA	$AE	Message Buffer 13 Data Register
		Reserved
FC2MB14_CONTROL	$B0	Message Buffer 14 Control / Status Register
FC2MB14_ID_HIGH	$B1	Message Buffer 14 ID High Register
FC2MB14_ID_LOW	$B2	Message Buffer 14 ID Low Register
FC2MB14_DATA	$B3	Message Buffer 14 Data Register
FC2MB14_DATA	$B4	Message Buffer 14 Data Register
FC2MB14_DATA	$B5	Message Buffer 14 Data Register
FC2MB14_DATA	$B6	Message Buffer 14 Data Register
		Reserved
FC2MB15_CONTROL	$B8	Message Buffer 15 Control / Status Register
FC2MB15_ID_HIGH	$B9	Message Buffer 15 ID High Register
FC2MB15_ID_LOW	$BA	Message Buffer 15 ID Low Register
FC2MB15_DATA	$BB	Message Buffer 15 Data Register
FC2MB15_DATA	$BC	Message Buffer 15 Data Register
FC2MB15_DATA	$BD	Message Buffer 15 Data Register

5.6.6.5 Reserved—Bits 7–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.6.6 SCI1 Transmitter Idle Interrupt Priority Level (SCI1_TIDL IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.7 SCI1 Transmitter Empty Interrupt Priority Level (SCI1_XMIT IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.8 SPI0 Transmitter Empty Interrupt Priority Level (SPI_XMIT IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7 Interrupt Priority Register 6 (IPR6)

Base + $6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	TMRC0 IPL		TMRD3 IPL		TMRD2 IPL		TMRD1 IPL		TMRD0 IPL		0	0	DEC0_XIRQ IPL		DEC0_HIRQ IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-9 Interrupt Priority Register 6 (IPR6)

5.6.9.3 Reserved—Bits 11–10

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.9.4 SCI0 Transmitter Idle Interrupt Priority Level (SCI0_TIDL IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.5 SCI0 Transmitter Empty Interrupt Priority Level (SCI0_XMIT IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.6 Timer A, Channel 3 Interrupt Priority Level (TMRA3 IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.7 Timer A, Channel 2 Interrupt Priority Level (TMRA2 IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.8 ADC B Conversion Complete Interrupt Priority Level (ADCB_CC IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.11 Vector Base Address Register (VBA)

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	VECTOR BASE ADDRESS												
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-13 Vector Base Address Register (VBA)

5.6.11.1 Reserved—Bits 15–13

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.11.2 Interrupt Vector Base Address (VECTOR BASE ADDRESS)—Bits 12–0

The contents of this register determine the location of the Vector Address Table. The value in this register is used as the upper 13 bits of the interrupt Vector Address Bus (VAB[20:0]). The lower eight bits are determined based upon the highest-priority interrupt. They are then appended onto VBA before presenting the full VAB to the 56800E core; see **Part 5.3.1** for details.

5.6.12 Fast Interrupt 0 Match Register (FIM0)

Base + $B	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0						
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-14 Fast Interrupt 0 Match Register (FIM0)

5.6.12.1 Reserved—Bits 15–7

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.12.2 Fast Interrupt 0 Vector Number (FAST INTERRUPT 0)—Bits 6–0

This value determines which IRQ will be a Fast Interrupt 0. Fast interrupts vector directly to a service routine based on values in the Fast Interrupt Vector Address registers without having to go to a jump table first; see **Part 5.3.3**. IRQs used as fast interrupts *must* be set to priority level 2. Unexpected results will

occur if a fast interrupt vector is set to any other priority. Fast interrupts automatically become the highest-priority level 2 interrupt, regardless of their location in the interrupt table, prior to being declared as fast interrupt. Fast interrupt 0 has priority over Fast Interrupt 1. To determine the vector number of each IRQ, refer to **Table 4-5**.

5.6.13 Fast Interrupt 0 Vector Address Low Register (FIVAL0)

Base + $C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-15 Fast Interrupt 0 Vector Address Low Register (FIVAL0)

5.6.13.1 Fast Interrupt 0 Vector Address Low (FIVAL0)—Bits 15–0

The lower 16 bits of the vector address are used for Fast Interrupt 0. This register is combined with FIVAH0 to form the 21-bit vector address for Fast Interrupt 0 defined in the FIM0 register.

5.6.14 Fast Interrupt 0 Vector Address High Register (FIVAH0)

Base + $D	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-16 Fast Interrupt 0 Vector Address High Register (FIVAH0)

5.6.14.1 Reserved—Bits 15–5

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.14.2 Fast Interrupt 0 Vector Address High (FIVAH0)—Bits 4–0

The upper five bits of the vector address are used for Fast Interrupt 0. This register is combined with FIVAL0 to form the 21-bit vector address for Fast Interrupt 0 defined in the FIM0 register.

5.6.15 Fast Interrupt 1 Match Register (FIM1)

Base + $E	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1						
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-17 Fast Interrupt 1 Match Register (FIM1)

5.6.15.1 Reserved—Bits 15–7

This bit field is reserved or not implemented. It is read as 0, but cannot be modified by writing.

5.6.15.2 Fast Interrupt 1 Vector Number (FAST INTERRUPT 1)—Bits 6–0

This value determines which IRQ will be a Fast Interrupt 1. Fast interrupts vector directly to a service routine based on values in the Fast Interrupt Vector Address registers without having to go to a jump table first; see **Part 5.3.3**. IRQs used as fast interrupts *must* be set to priority level 2. Unexpected results will occur if a fast interrupt vector is set to any other priority. Fast interrupts automatically become the highest-priority level 2 interrupt, regardless of their location in the interrupt table, prior to being declared as fast interrupt. Fast interrupt 0 has priority over Fast Interrupt 1. To determine the vector number of each IRQ, refer to **Table 4-5**.

5.6.16 Fast Interrupt 1 Vector Address Low Register (FIVAL1)

Base + $F	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FAST INTERRUPT 1 VECTOR ADDRESS LOW															
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-18 Fast Interrupt 1 Vector Address Low Register (FIVAL1)

5.6.16.1 Fast Interrupt 1 Vector Address Low (FIVAL1)—Bits 15–0

The lower 16 bits of vector address are used for Fast Interrupt 1. This register is combined with FIVAH1 to form the 21-bit vector address for Fast Interrupt 1 defined in the FIM1 register.

5.6.17 Fast Interrupt 1 Vector Address High Register (FIVAH1)

Base + $10	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1 VECTOR ADDRESS HIGH				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-19 Fast Interrupt 1 Vector Address High Register (FIVAH1)

5.6.17.1 Reserved—Bits 15–5

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.17.2 Fast Interrupt 1 Vector Address High (FIVAH1)—Bits 4–0

The upper five bits of vector address are used for Fast Interrupt 1. This register is combined with FIVAL1 to form the 21-bit vector address for Fast Interrupt 1 defined in the FIM1 register.

5.6.18 IRQ Pending 0 Register (IRQP0)

Base + $11	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [16:2]															1
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-20 IRQ Pending 0 Register (IRQP0)

5.6.23.2 IRQ Pending (PENDING)—Bits 81–85

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 85.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.24 Reserved—Base + 17

5.6.25 Reserved—Base + 18

5.6.26 Reserved—Base + 19

5.6.27 Reserved—Base + 1A

5.6.28 Reserved—Base + 1B

5.6.29 Reserved—Base + 1C

5.6.30 ITCN Control Register (ICTL)

Base + $1D	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	INT	IPIC		VAB							INT_DIS	1	$\overline{\text{IRQB}}$ STATE	$\overline{\text{IRQA}}$ STATE	$\overline{\text{IRQB}}$ EDG	$\overline{\text{IRQA}}$ EDG
Write																
RESET	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	0

Figure 5-26 ITCN Control Register (ICTL)

5.6.30.1 Interrupt (INT)—Bit 15

This *read-only* bit reflects the state of the interrupt to the 56800E core.

- 0 = No interrupt is being sent to the 56800E core
- 1 = An interrupt is being sent to the 56800E core

5.6.30.2 Interrupt Priority Level (IPIC)—Bits 14–13

These *read-only* bits reflect the state of the new interrupt priority level bits being presented to the 56800E core at the time the last IRQ was taken. This field is only updated when the 56800E core jumps to a new interrupt service routine.

Note: Nested interrupts may cause this field to be updated before the original interrupt service routine can read it.

- 00 = Required nested exception priority levels are 0, 1, 2, or 3
- 01 = Required nested exception priority levels are 1, 2, or 3
- 10 = Required nested exception priority levels are 2 or 3
- 11 = Required nested exception priority level is 3

The upper four bits of the GPIOB register can function as GPIO, [A23:20], or as additional clock output signals. GPIO has priority and is enabled/disabled via the GPIOB_PER. If GPIOB[7:4] are programmed to operate as peripheral outputs, then the choice between [A23:20] and additional clock outputs is done here in the CLKOSR. The default state is for the peripheral function of GPIOB[7:4] to be programmed as [A23:20]. This can be changed by altering [A23:20] as shown in **Figure 6-9**.

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	A23	A22	A21	A20	CLK DIS	CLKOSEL				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Figure 6-9 CLKO Select Register (SIM_CLKOSR)

6.5.7.1 Reserved—Bits 15–10

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.7.2 Alternate GPIOB Peripheral Function for A23 (A23)—Bit 9

- 0 = Peripheral output function of GPIOB7 is defined to be A23
- 1 = Peripheral output function of GPIOB7 is defined to be the oscillator_clock (MSTR_OSC in **Figure 3-4**)

6.5.7.3 Alternate GPIOB Peripheral Function for A22 (A22)—Bit 8

- 0 = Peripheral output function of GPIOB6 is defined to be A22
- 1 = Peripheral output function of GPIOB6 is defined to be SYS_CLK2

6.5.7.4 Alternate GPIOB Peripheral Function for A21 (A21)—Bit 7

- 0 = Peripheral output function of GPIOB5 is defined to be A21
- 1 = Peripheral output function of GPIOB5 is defined to be SYS_CLK

6.5.7.5 Alternate GPIOB Peripheral Function fpr A20 (A20)—Bit 6

- 0 = Peripheral output function of GPIOB4 is defined to be A20
- 1 = Peripheral output function of GPIOB4 is defined to be the prescaler_clock (FREF in **Figure 3-4**)

6.5.7.6 Clockout Disable (CLKDIS)—Bit 5

- 0 = CLKOUT output is enabled and will output the signal indicated by CLKOSEL
- 1 = CLKOUT is tri-stated

6.5.7.7 CLockout Select (CLKOSEL)—Bits 4–0

Selects clock to be muxed out on the CLKO pin.

- 00000 = SYS_CLK (from OCCS - DEFAULT)
- 00001 = Reserved for factory test—56800E clock
- 00010 = Reserved for factory test—XRAM clock
- 00011 = Reserved for factory test—PFLASH odd clock

Table 10-15 Crystal Oscillator Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Quiescent Current, power-down mode	I_{PD}	—	0	1	μA

10.8 External Memory Interface Timing

The External Memory Interface is designed to access static memory and peripheral devices. **Figure 10-5** shows sample timing and parameters that are detailed in **Table 10-16**.

The timing of each parameter consists of both a fixed delay portion and a clock related portion, as well as user controlled wait states. The equation:

$$t = D + P * (M + W)$$

should be used to determine the actual time of each parameter. The terms in this equation are defined as:

- t = Parameter delay time
- D = Fixed portion of the delay, due to on-chip path delays
- P = Period of the system clock, which determines the execution rate of the part (i.e., when the device is operating at 60MHz, P = 16.67 ns)
- M = Fixed portion of a clock period inherent in the design; this number is adjusted to account for possible derating of clock duty cycle
- W = Sum of the applicable wait state controls. The “Wait State Controls” column of **Table 10-16** shows the applicable controls for each parameter and the EMI chapter of the **56F8300 Peripheral User Manual** details what each wait state field controls.

When using the XTAL clock input directly as the chip clock without prescaling (ZSRC selects prescaler clock and prescaler set to ÷ 1), the EMI quadrature clock is generated using both edges of the EXTAL clock input. In this situation only, parameter values must be adjusted for the duty cycle at XTAL. DCAOE and DCAEO are used to make this duty cycle adjustment where needed.

DCAOE and DCAEO are calculated as follows:

DCAOE = 0.5 - MAX XTAL duty cycle, if ZSRC selects prescaler clock and the prescaler is set to ÷ 1
= 0.0 all other cases

DCAEO = MIN XTAL duty cycle - 0.5, if ZSRC selects prescaler clock and the prescaler is set to ÷ 1
= 0.0 all other cases

Example of DCAOE and DCAEO calculation:

Assuming prescaler is set for ÷ 1 and prescaler clock is selected by ZSRC, if XTAL duty cycle ranges between 45% and 60% high;

DCAOE = .50 - .60 = - 0.1
DCAEO = .45 - .50 = - 0.05

The timing of write cycles is different when WWS = 0 than when WWS > 0. Therefore, some parameters contain two sets of numbers to account for this difference. Use the “Wait States Configuration” column of **Table 10-16** to make the appropriate selection.

10.14 Controller Area Network (CAN) Timing

Note: *CAN is not available in the 56F8167 device.*

Table 10-22 CAN Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud Rate	BR_{CAN}	—	1	Mbps	—
Bus Wake Up detection	T_{WAKEUP}	5	—	µs	10-19

1. Parameters listed are guaranteed by design

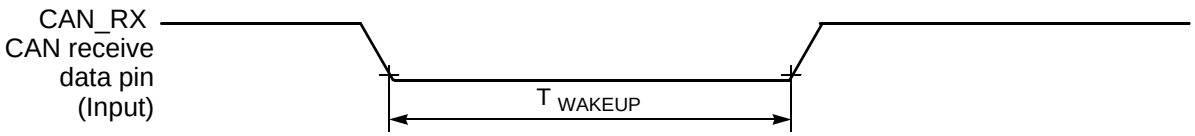


Figure 10-19 Bus Wakeup Detection

10.15 JTAG Timing

Table 10-23 JTAG Timing

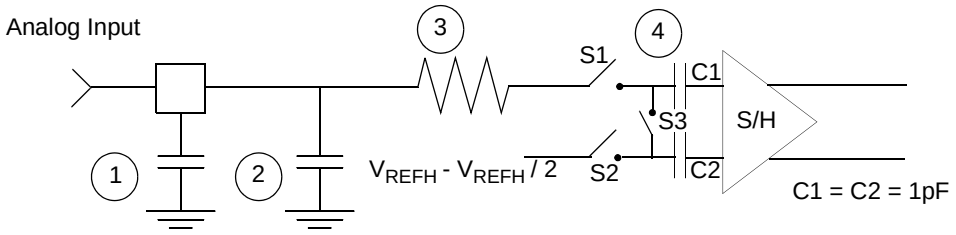
Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation using EOnCE[1]	f_{OP}	DC	SYS_CLK/8	MHz	10-20
TCK frequency of operation not using EOnCE[1]	f_{OP}	DC	SYS_CLK/4	MHz	10-20
TCK clock pulse width	t_{PW}	50	—	ns	10-20
TMS, TDI data set-up time	t_{DS}	5	—	ns	10-21
TMS, TDI data hold time	t_{DH}	5	—	ns	10-21
TCK low to TDO data valid	t_{DV}	—	30	ns	10-21
TCK low to TDO tri-state	t_{TS}	—	30	ns	10-21
$\overline{\text{TRST}}$ assertion time	t_{TRST}	$2T$[2]	—	ns	10-22

1. TCK frequency of operation must be less than 1/8 the processor rate.
2. T = processor clock period (nominally 1/60MHz)

10.17 Equivalent Circuit for ADC Inputs

Figure 10-24 illustrates the ADC input circuit during sample & hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed & S3 is open, one input of the sample and hold circuit moves to V_{REFH} - V_{REFH} / 2, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about V_{REFH} - V_{REFH} / 2. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). Note that there are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase.

One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pf
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pf
3. Equivalent resistance for the ESD isolation resistor and the channel select mux; 500 ohms
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1pf

Figure 10-24 Equivalent Circuit for A/D Loading

10.18 Power Consumption

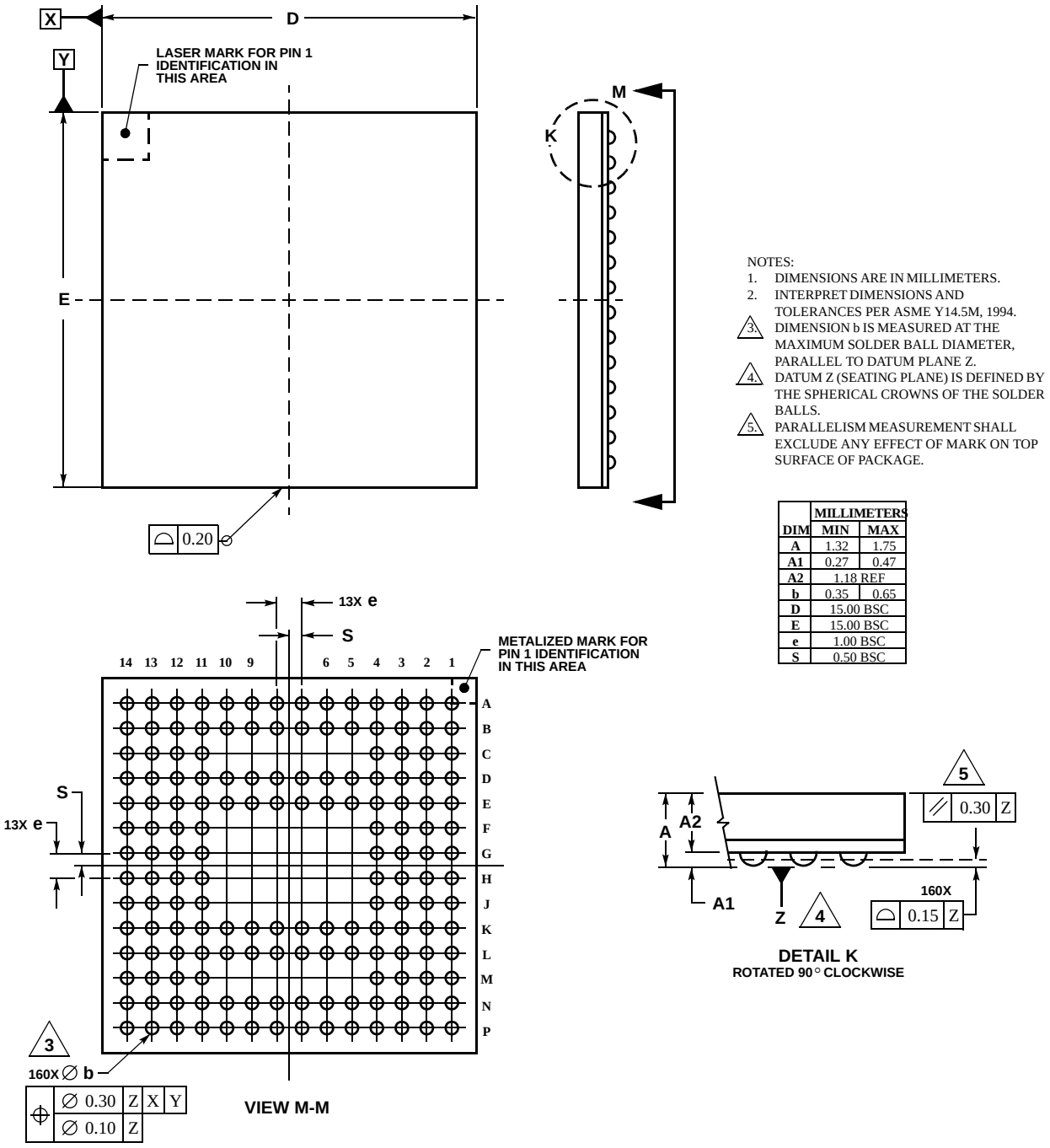
This section provides additional detail which can be used to optimize power consumption for a given application.

Power consumption is given by the following equation:

Total power = A: internal [static component]
+B: internal [state-dependent component]
+C: internal [dynamic component]
+D: external [dynamic component]
+E: external [static]

A, the internal [static component], is comprised of the DC bias currents for the oscillator, leakage current, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

B, the internal [state-dependent component], reflects the supply current required by certain on-chip resources only when those resources are in use. These include RAM, Flash memory and the ADCs.



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.32	1.75
A1	0.27	0.47
A2	1.18 REF	
b	0.35	0.65
D	15.00 BSC	
E	15.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

CASE 1268-01
ISSUE O

Figure 11-3 160 MAPBGA Mechanical Information

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

12.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the hybrid controller, and from the board ground to each V_{SS} (GND) pin
- The minimum bypass requirement is to place six 0.01–0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including $V_{DDA}/V_{SSA.}$ Ceramic and tantalum capacitors tend to provide better performance tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are less than 0.5 inch per capacitor lead
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{DD} and V_{SS}
- Bypass the V_{DD} and V_{SS} layers of the PCB with approximately 100µF, preferably with a high-grade capacitor such as a tantalum capacitor
- Because the device’s output signals have fast rise and fall times, PCB trace lengths should be minimal