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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	76
Program Memory Size	512KB (256K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	18K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LQFP
Supplier Device Package	160-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8367vpye

1.1.3 Memory

Note: *Features in italics are NOT available in the 56F8167 device.*

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security protection feature
- On-chip memory, including a low-cost, high-volume Flash solution
  - 512KB of Program Flash
  - *4KB of Program RAM*
  - *32KB of Data Flash*
  - 32KB of Data RAM
  - 32KB of Boot Flash
- Off-chip memory expansion capabilities provide a simple method for interfacing additional external memory and/or peripheral devices
  - Access up to 4MB of external program memory or 32MB of external data memory
  - Chip select logic for glueless interface to ROM and SRAM
- EEPROM emulation capability

1.1.4 Peripheral Circuits

Note: *Features in italics are NOT available in the 56F8167 device.*

- Pulse Width Modulator:
  - In the 56F8367, two Pulse Width Modulator modules, each with six PWM outputs, three Current Sense inputs, and three Fault inputs; fault-tolerant design with dead time insertion; supports both center-aligned and edge-aligned modes
  - In the 56F8167, one Pulse Width Modulator module, with six PWM outputs, three Current Sense inputs, and three Fault inputs; fault-tolerant design with dead time insertion; supports both center-aligned and edge-aligned modes
- Four 12-bit, Analog-to-Digital Converters (ADCs), which support four simultaneous conversions with quad, 4-pin multiplexed inputs; ADC and PWM modules can be synchronized through Timer C, channels 2 and 3
- Quadrature Decoder:
  - In the 56F8367, two four-input Quadrature Decoders or two additional Quad Timers
  - In the 56F8167, one four-input Quadrature Decoder, which works in conjunction with Quad Timer A
- *Temperature Sensor can be connected, on the board, to any of the ADC inputs to monitor the on-chip temperature*
- Quad Timer:
  - In the 56F8367, four dedicated general-purpose Quad Timers totaling six dedicated pins: Timer C with two pins and Timer D with four pins
  - In the 56F8167, two general-purpose Quad Timers; Timer A works in conjunction with Quadrature Decoder 0 or GPIO and Timer C works in conjunction with GPIO
- *Up to two FlexCAN (CAN Version 2.0 B-compliant) modules with 2-pin port for transmit and receive*

Table 1-2 Bus Signal Names

Name	Function
Program Memory Interface	
pdb_m[15:0]	Program data bus for instruction word fetches or read operations.
cdbw[15:0]	Primary core data bus used for program memory writes. (Only these 16 bits of the cdbw[31:0] bus are used for writes to program memory.)
pab[20:0]	Program memory address bus. Data is returned on pdb_m bus.
Primary Data Memory Interface Bus	
cdbr_m[31:0]	Primary core data bus for memory reads. Addressed via xab1 bus.
cdbw[31:0]	Primary core data bus for memory writes. Addressed via xab1 bus.
xab1[23:0]	Primary data address bus. Capable of addressing bytes[1], words, and long data types. Data is written on cdbw and returned on cdbr_m. Also used to access memory-mapped I/O.
Secondary Data Memory Interface	
xdb2_m[15:0]	Secondary data bus used for secondary data address bus xab2 in the dual memory reads.
xab2[23:0]	Secondary data address bus used for the second of two simultaneous accesses. Capable of addressing only words. Data is returned on xdb2_m.
Peripheral Interface Bus	
IPBus [15:0]	Peripheral bus accesses all on-chip peripherals registers. This bus operates at the same clock rate as the Primary Data Memory and therefore generates no delays when accessing the processor. Write data is obtained from cdbw. Read data is provided to cdbr_m.

1. Byte accesses can only occur in the bottom half of the memory address space. The MSB of the address will be forced to 0.

1.5 Product Documentation

The documents in **Table 1-2** are required for a complete description and proper design with the 56F8367/56F8167 devices. Documentation is available from local Freescale distributors, Freescale semiconductor sales offices, Freescale Literature Distribution Centers, or online at **http://www.freescale.com**.

Table 1-3 Chip Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, and 16-bit controller core processor and the instruction set	DSP56800EERM
56F8300 Peripheral User Manual	Detailed description of peripherals of the 56F8300 devices	MC56F8300UM
56F8300 SCI/CAN Bootloader User Manual	Detailed description of the SCI/CAN Bootloaders 56F8300 family of devices	MC56F83xxBLUM
56F8367/56F8167 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F8367
Errata	Details any chip issues that might be present	MC56F8367E MC56F8167E

1.6 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
“asserted”	A high true (active high) signal is high or a low true (active low) signal is low.
“deasserted”	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for VIL, VOL, VIH, and VOH are defined by individual product specifications.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
A6	17	G1	Output	In reset, output is disabled, pull-up is enabled	**Address Bus** — A6 - A7 specify two of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A6 - A7 and EMI control signals are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. **Port E GPIO** — These two GPIO pins can be individually programmed as input or output pins. After reset, the default state is Address Bus. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOE_PUR register. Example: GPIOE2, clear bit 2 in the GPIOE_PUR register.
(GPIOE2)					
A7 (GPIOE3)	18	G3	Schmitt Input/ Output		
A8	19	G2	Output	In reset, output is disabled, pull-up is enabled	**Address Bus**— A8 - A15 specify eight of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A8 - A15 and EMI control signals are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. **Port A GPIO** — These eight GPIO pins can be individually programmed as input or output pins. After reset, the default state is Address Bus. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOA_PUR register. Example: GPIOA0, clear bit 0 in the GPIOA_PUR register.
(GPIOA0)					
A9 (GPIOA1)	20	H1	Schmitt Input/ Output		
A10 (GPIOA2)	21	H2			
A11 (GPIOA3)	22	H4			
A12 (GPIOA4)	23	H3			
A13 (GPIOA5)	24	J1			
A14 (GPIOA6)	25	J2			
A15 (GPIOA7)	26	J3			

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
D7 **(GPIOF0)**	28	K1	Input/ Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Data Bus** — D7 - D15 specify part of the data for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), D7 - D15 are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. **Port F GPIO** — These nine GPIO pins can be individually programmed as input or output pins. At reset, these pins default to Data Bus functionality. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOF_PUR register. Example: GPIOF0, clear bit 0 in the GPIOF_PUR register.
D8 (GPIOF1)	29	K3			
D9 (GPIOF2)	30	K2			
D10 (GPIOF3)	32	K4			
D11 (GPIOF4)	149	A5			
D12 (GPIOF5)	150	A4			
D13 (GPIOF6)	151	B5			
D14 (GPIOF7)	152	C4			
D15 (GPIOF8)	153	A3			
$\overline{\text{RD}}$	52	P5	Output	In reset, output is disabled, pull-up is enabled	**Read Enable** — $\overline{\text{RD}}$ is asserted during external memory read cycles. When $\overline{\text{RD}}$ is asserted low, pins D0 - D15 become inputs and an external device is enabled onto the data bus. When $\overline{\text{RD}}$ is deasserted high, the external data is latched inside the device. When $\overline{\text{RD}}$ is asserted, it qualifies the A0 - A23, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{CS}}$n pins. $\overline{\text{RD}}$ can be connected directly to the $\overline{\text{OE}}$ pin of a static RAM or ROM. Depending upon the state of the DRV bit in the EMI bus control register (BCR), $\overline{\text{RD}}$ is tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. To deactivate the internal pull-up resistor, set the CTRL bit in the SIM_PUDR register.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
TXD1 **(GPIOD6)**	49	P4	Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Transmit Data** — SCI1 transmit data output **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI output. To deactivate the internal pull-up resistor, clear bit 6 in the GPIOD_PUR register.
RXD1 **(GPIOD7)**	50	N5	Input Input/ Output	Input, pull-up enabled	**Receive Data** — SCI1 receive data input **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI input. To deactivate the internal pull-up resistor, clear bit 7 in the GPIOD_PUR register.
TCK	137	D8	Schmitt Input	Input, pulled low internally	**Test Clock Input** — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pull-down resistor.
TMS	138	A8	Schmitt Input	Input, pulled high internally	**Test Mode Select Input** — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. To deactivate the internal pull-up resistor, set the JTAG bit in the SIM_PUDR register. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
TDI	139	B8	Schmitt Input	Input, pulled high internally	**Test Data Input** — This input pin provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. To deactivate the internal pull-up resistor, set the JTAG bit in the SIM_PUDR register.
TDO	140	D7	Output	In reset, output is disabled, pull-up is enabled	**Test Data Output** — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
MOSI0 **(GPIOE5)**	148	B6	Input/ Output Input/ Output	In reset, output is disabled, pull-up is enabled	**SPI 0 Master Out/Slave In** — This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data. **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is MOSI0. To deactivate the internal pull-up resistor, clear bit 5 in the GPIOE_PUR register.
MISO0 **(GPIOE6)**	147	D4	Input/ Output Input/ Output	Input, pull-up enabled	**SPI 0 Master In/Slave Out** — This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. The slave device places data on the MISO line a half-cycle before the clock edge the master device uses to latch the data. **Port E GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is MISO0. To deactivate the internal pull-up resistor, clear bit 6 in the GPIOE_PUR register.
$\overline{\text{SS0}}$ **(GPIOE7)**	145	D5	Input Input/ Output	Input, pull-up enabled	**SPI 0 Slave Selec**t — $\overline{\text{SS0}}$ is used in slave mode to indicate to the SPI module that the current transfer is to be received. **Port E GPIO** — This GPIO pin can be individually programmed as input or output pin. After reset, the default state is $\overline{\text{SS0}}$. To deactivate the internal pull-up resistor, clear bit 7 in the GPIOE_PUR register.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
ISB0 **(GPIOD10)**	61	N8	Schmitt Input Schmitt Input/ Output	Input, pull-up enabled	**ISB0 - 2** — These three input current status pins are used for top/bottom pulse width correction in complementary channel operation for PWMB. **Port D GPIO** — These GPIO pins can be individually programmed as input or output pins. At reset, these pins default to ISB functionality. To deactivate the internal pull-up resistor, clear the appropriate bit of the GPIOD_PUR register. For details, see **Part 6.5.8**.
ISB1 (GPIOD11)	63	L8			
ISB2 (GPIOD12)	64	P8			
FAULTB0	67	N9	Schmitt Input	Input, pull-up enabled	**FAULTB0 - 3** — These four fault input pins are used for disabling selected PWMB outputs in cases where fault conditions originate off-chip. To deactivate the internal pull-up resistor, set the PWMB bit in the SIM_PUDR register. For details, see **Part 6.5.8**.
FAULTB1	68	L9			
FAULTB2	69	L10			
FAULTB3	72	P11			
ANA0	100	G13	Input	Analog Input	**ANA0 - 3** — Analog inputs to ADC A, channel 0
ANA1	101	H13			
ANA2	102	G12			
ANA3	103	F13			
ANA4	104	F12	Input	Analog Input	**ANA4 - 7** — Analog inputs to ADC A, channel 1
ANA5	105	H14			
ANA6	106	G14			
ANA7	107	E13			
V_{REFH}	113	D14	Input	Analog Input	**V_{REFH}** — Analog Reference Voltage High. V_{REFH} must be less than or equal to V_{DDA_ADC}.
V_{REFP}	112	D13	Input/ Output	Analog Input/ Output	**V_{REFP}, V_{REFMID} & V_{REFN}** — Internal pins for voltage reference which are brought off-chip so they can be bypassed. Connect to a 0.1µF low ESR capacitor.
V_{REFMID}	111	E14			
V_{REFN}	110	F14			
V_{REFLO}	109	E12	Input	Analog Input	**V_{REFLO}** — Analog Reference Voltage Low. This should normally be connected to a low-noise V_{SS}.

start-up. The crystal and associated components should be mounted as near as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

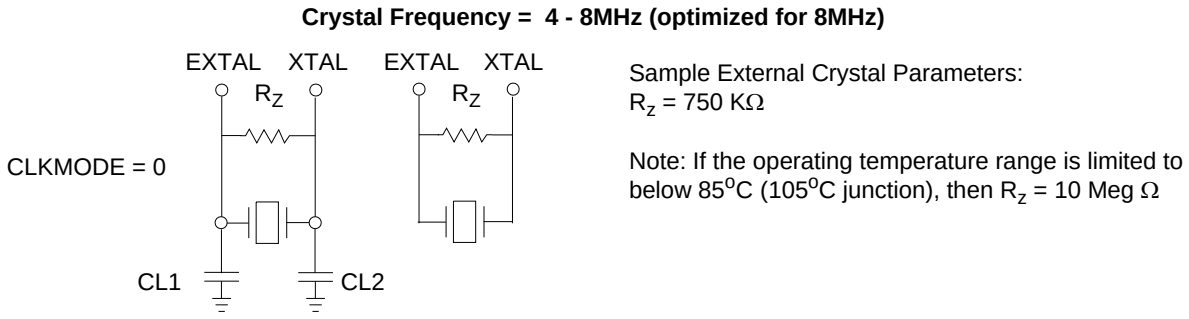

Figure 3-2 Connecting to a Crystal Oscillator

Note: The OCCS_COHL bit must be set to 1 when a crystal oscillator is used. The reset condition on the OCCS_COHL bit is 0. Please see the COHL bit in the Oscillator Control (OSCTL) register, discussed in the **56F8300 Peripheral User Manual**.

3.2.2 Ceramic Resonator (Default)

It is also possible to drive the internal oscillator with a ceramic resonator, assuming the overall system design can tolerate the reduced signal integrity. A typical ceramic resonator circuit is shown in **Figure 3-3**. Refer to the supplier's recommendations when selecting a ceramic resonator and associated components. The resonator and components should be mounted as near as possible to the EXTAL and XTAL pins.

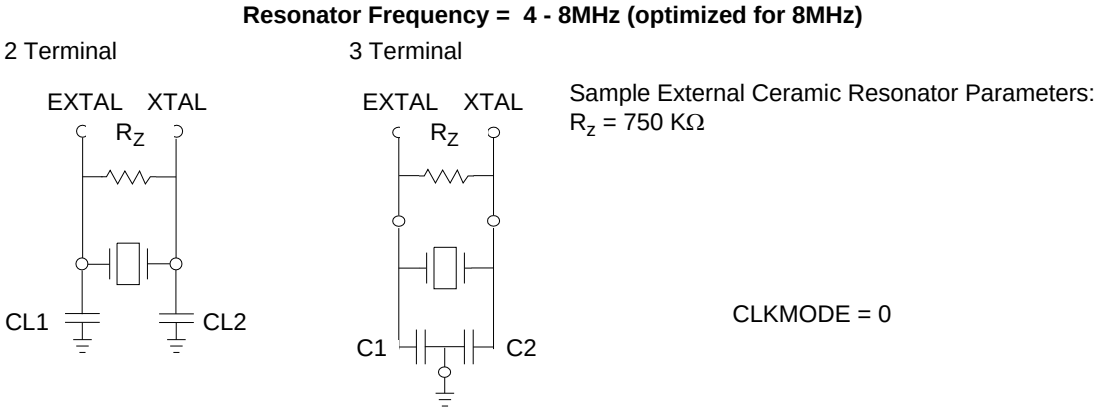

Figure 3-3 Connecting a Ceramic Resonator

Note: The OCCS_COHL bit must be set to 0 when a ceramic resonator is used. The reset condition on the OCCS_COHL bit is 0. Please see the COHL bit in the Oscillator Control (OSCTL) register, discussed in the **56F8300 Peripheral User Manual**.

3.2.3 External Clock Source

The recommended method of connecting an external clock is given in **Figure 3-4**. The external clock source is connected to XTAL and the EXTAL pin is grounded. When using an external clock source, set

The location of the vector table is determined by the Vector Base Address (VBA) register. Please see **Part 5.6.11** for the reset value of the VBA.

In some configurations, the reset address and COP reset address will correspond to vector 0 and 1 of the interrupt vector table. In these instances, the first two locations in the vector table must contain branch or JMP instructions. All other entries must contain JSR instructions.

Note: *PWMA, FlexCAN, Quadrature Decoder 1, and Quad Timers B and D are NOT available on the 56F8167 device.*

Table 4-5 Interrupt Vector Table Contents[1]

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
				Reserved for Reset Overlay[2]
				Reserved for COP Reset Overlay[2]
core	2	3	P:$04	Illegal Instruction
core	3	3	P:$06	SW Interrupt 3
core	4	3	P:$08	HW Stack Overflow
core	5	3	P:$0A	Misaligned Long Word Access
core	6	1-3	P:$0C	OnCE Step Counter
core	7	1-3	P:$0E	OnCE Breakpoint Unit 0
				Reserved
core	9	1-3	P:$12	OnCE Trace Buffer
core	10	1-3	P:$14	OnCE Transmit Register Empty
core	11	1-3	P:$16	OnCE Receive Register Full
				Reserved
core	14	2	P:$1C	SW Interrupt 2
core	15	1	P:$1E	SW Interrupt 1
core	16	0	P:$20	SW Interrupt 0
core	17	0-2	P:$22	IRQA
core	18	0-2	P:$24	IRQB
				Reserved
LVI	20	0-2	P:$28	Low-Voltage Detector (power sense)
PLL	21	0-2	P:$2A	PLL
FM	22	0-2	P:$2C	FM Access Error Interrupt
FM	23	0-2	P:$2E	FM Command Complete
FM	24	0-2	P:$30	FM Command, data and address Buffers Empty
				Reserved

4.4 Data Map

Note: *Data Flash is NOT available on the 56F8167 device.*

Table 4-6 Data Memory Map[1]

Begin/End Address	EX = 0[2]	EX = 1
X:$FF FFFF X:$FF FF00	EOnCE 256 locations allocated	EOnCE 256 locations allocated
X:$FF FEFF X:$01 0000	External Memory	External Memory
X:$00 FFFF X:$00 F000	On-Chip Peripherals 4096 locations allocated	On-Chip Peripherals 4096 locations allocated
X:$00 EFFF X:$00 8000	External Memory	External Memory
X:$00 7FFF X:$00 4000	*On-Chip Data Flash* *32KB*	
X:$00 3FFF X:$00 0000	On-Chip Data RAM 32KB[3]	

1. All addresses are 16-bit Word addresses, not byte addresses.
2. In the Operating Mode Register (OMR).
3. The Data RAM is organized as an 8K x 32-bit memory to allow single-cycle, long-word operations.

4.5 Flash Memory Map

Figure 4-1 illustrates the Flash Memory (FM) map on the system bus.

The Flash Memory is divided into three functional blocks. The Program and boot memories reside on the Program Memory buses. They are controlled by one set of banked registers. Data Memory Flash resides on the Data Memory buses and is controlled separately by its own set of banked registers.

The top nine words of the Program Memory Flash are treated as special memory locations. The content of these words is used to control the operation of the Flash Controller. Because these words are part of the Flash Memory content, their state is maintained during power down and reset. During chip initialization, the content of these memory locations is loaded into Flash Memory control registers, detailed in the Flash Memory chapter of the **56F8300 Peripheral User Manual**. These configuration parameters are located between $03_FFF7 and $03_FFFF.

Table 4-32 GPIOD Registers Address Map (GPIOD_BASE = $00 F320)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOD_PUR	$0	Pull-up Enable Register	0 x 1FFF
GPIOD_DR	$1	Data Register	0 x 0000
GPIOD_DDR	$2	Data Direction Register	0 x 0000
GPIOD_PER	$3	Peripheral Enable Register	0 x 1FC0
GPIOD_IAR	$4	Interrupt Assert Register	0 x 0000
GPIOD_IENR	$5	Interrupt Enable Register	0 x 0000
GPIOD_IPOLR	$6	Interrupt Polarity Register	0 x 0000
GPIOD_IPR	$7	Interrupt Pending Register	0 x 0000
GPIOD_IESR	$8	Interrupt Edge-Sensitive Register	0 x 0000
GPIOD_PPMODE	$9	Push-Pull Mode Register	
GPIOD_RAWDATA	$A	Raw Data Input Register	—

Table 4-33 GPIOE Registers Address Map (GPIOE_BASE = $00 F330)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOE_PUR	$0	Pull-up Enable Register	0 x 3FFF
GPIOE_DR	$1	Data Register	0 x 0000
GPIOE_DDR	$2	Data Direction Register	0 x 0000
GPIOE_PER	$3	Peripheral Enable Register	0 x 3FFF
GPIOE_IAR	$4	Interrupt Assert Register	0 x 0000
GPIOE_IENR	$5	Interrupt Enable Register	0 x 0000
GPIOE_IPOLR	$6	Interrupt Polarity Register	0 x 0000
GPIOE_IPR	$7	Interrupt Pending Register	0 x 0000
GPIOE_IESR	$8	Interrupt Edge-Sensitive Register	0 x 0000
GPIOE_PPMODE	$9	Push-Pull Mode Register	0 x 3FFF
GPIOE_RAWDATA	$A	Raw Data Input Register	—

5.6.3.5 Low Voltage Detector Interrupt Priority Level (LVI IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.6 Reserved—Bits 5–4

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.3.7 External IRQ B Interrupt Priority Level (IRQB IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.8 External IRQ A Interrupt Priority Level (IRQA IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4 Interrupt Priority Register 3 (IPR3)

Base + $3	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	GPIOD IPL		GPIOE IPL		GPIOFIPL		FCMSGBUF IPL		FCWKUP IPL		FCERR IPL		FCBOFF IPL		0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-6 Interrupt Priority Register 3 (IPR3)

5.6.4.1 GPIOD Interrupt Priority Level (GPIOD IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.1 Timer C, Channel 0 Interrupt Priority Level (TMRC0 IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.2 Timer D, Channel 3 Interrupt Priority Level (TMRD3 IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.3 Timer D, Channel 2 Interrupt Priority Level (TMRD2 IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.4 Timer D, Channel 1 Interrupt Priority Level (TMRD1 IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.5 Timer D, Channel 0 Interrupt Priority Level (TMRD0 IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.6 Reserved—Bits 5–4

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.7.7 Quadrature Decoder 0, INDEX Pulse Interrupt Priority Level (DEC0_XIRQ IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.8 Quadrature Decoder 0, HOME Signal Transition or Watchdog Timer Interrupt Priority Level (DEC0_HIRQ IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8 Interrupt Priority Register 7 (IPR7)

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	TMRA0 IPL		TMRB3 IPL		TMRB2 IPL		TMRB1 IPL		TMRB0 IPL		TMRC3 IPL		TMRC2 IPL		TMRC1 IPL	
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-10 Interrupt Priority Register (IPR7)

5.6.8.1 Timer A, Channel 0 Interrupt Priority Level (TMRA0 IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.21 IRQ Pending 3 Register (IRQP3)

Base + $14	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [64:49]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-23 IRQ Pending 3 Register (IRQP3)

5.6.21.1 IRQ Pending (PENDING)—Bits 64–49

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.22 IRQ Pending 4 Register (IRQP4)

Base + $15	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [80:65]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-24 IRQ Pending 4 Register (IRQP4)

5.6.22.1 IRQ Pending (PENDING)—Bits 80–65

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.23 IRQ Pending 5 Register (IRQP5)

Base + $16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	1	1	1	1	1	1	1	1	1	1	1	PENDING[85:81]				
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-25 IRQ Pending Register 5 (IRQP5)

5.6.23.1 Reserved—Bits 96–86

This bit field is reserved or not implemented. The bits are read as 1 and cannot be modified by writing.

6.5.6.3 CAN—Bit 13

This bit controls the pull-up resistors on the CAN_RX pin.

6.5.6.4 EMI_MODE—Bit 12

This bit controls the pull-up resistors on the EMI_MODE pin.

6.5.6.5 $\overline{\text{RESET}}$—Bit 11

This bit controls the pull-up resistors on the $\overline{\text{RESET}}$ pin.

6.5.6.6 IRQ—Bit 10

This bit controls the pull-up resistors on the $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ pins.

6.5.6.7 XBOOT—Bit 9

This bit controls the pull-up resistors on the EXTBOOT pin.

Note: In this package, this input pin is double-bonded with the adjacent V_{SS} pin and this bit should be changed to a 1 in order to reduce power consumption.

6.5.6.8 PWMB—Bit 8

This bit controls the pull-up resistors on the FAULTB0, FAULTB1, FAULTB2, and FAULTB3 pins.

6.5.6.9 PWMA0—Bit 7

This bit controls the pull-up resistors on the FAULTA0, FAULTA1, and FAULTA2 pins.

6.5.6.10 Reserved—Bit 6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.11 CTRL—Bit 5

This bit controls the pull-up resistors on the $\overline{\text{WR}}$ and $\overline{\text{RD}}$ pins.

6.5.6.12 Reserved—Bit 4

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.13 JTAG—Bit 3

This bit controls the pull-up resistors on the $\overline{\text{TRST}}$, TMS and TDI pins.

6.5.6.14 Reserved—Bit 2–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.7 CLKO Select Register (SIM_CLKOSR)

The CLKO select register can be used to multiplex out any one of the clocks generated inside the clock generation and SIM modules. The default value is SYS_CLK. All other clocks primarily muxed out are for test purposes only, and are subject to significant phase shift at high frequencies.

10.10 Serial Peripheral Interface (SPI) Timing

Table 10-18 SPI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 50 50	 — —	 ns ns	10-11, 10-12, 10-13, 10-14
Enable lead time Master Slave	t_{ELD}	 — 25	 — —	 ns ns	10-14
Enable lag time Master Slave	t_{ELG}	 — 100	 — —	 ns ns	10-14
Clock (SCK) high time Master Slave	t_{CH}	 17.6 25	 — —	 ns ns	10-11, 10-12, 10-13, 10-14
Clock (SCK) low time Master Slave	t_{CL}	 24.1 25	 — —	 ns ns	10-14
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	10-11, 10-12, 10-13, 10-14
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	10-11, 10-12, 10-13, 10-14
Access time (time to data active from high-impedance state) Slave	t_A	4.8	15	ns	10-14
Disable time (hold time to high-impedance state) Slave	t_D	3.7	15.2	ns	10-14
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	10-11, 10-12, 10-13, 10-14
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	10-11, 10-12, 10-13
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	10-11, 10-12, 10-13, 10-14
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	10-11, 10-12, 10-13, 10-14

1. Parameters listed are guaranteed by design.

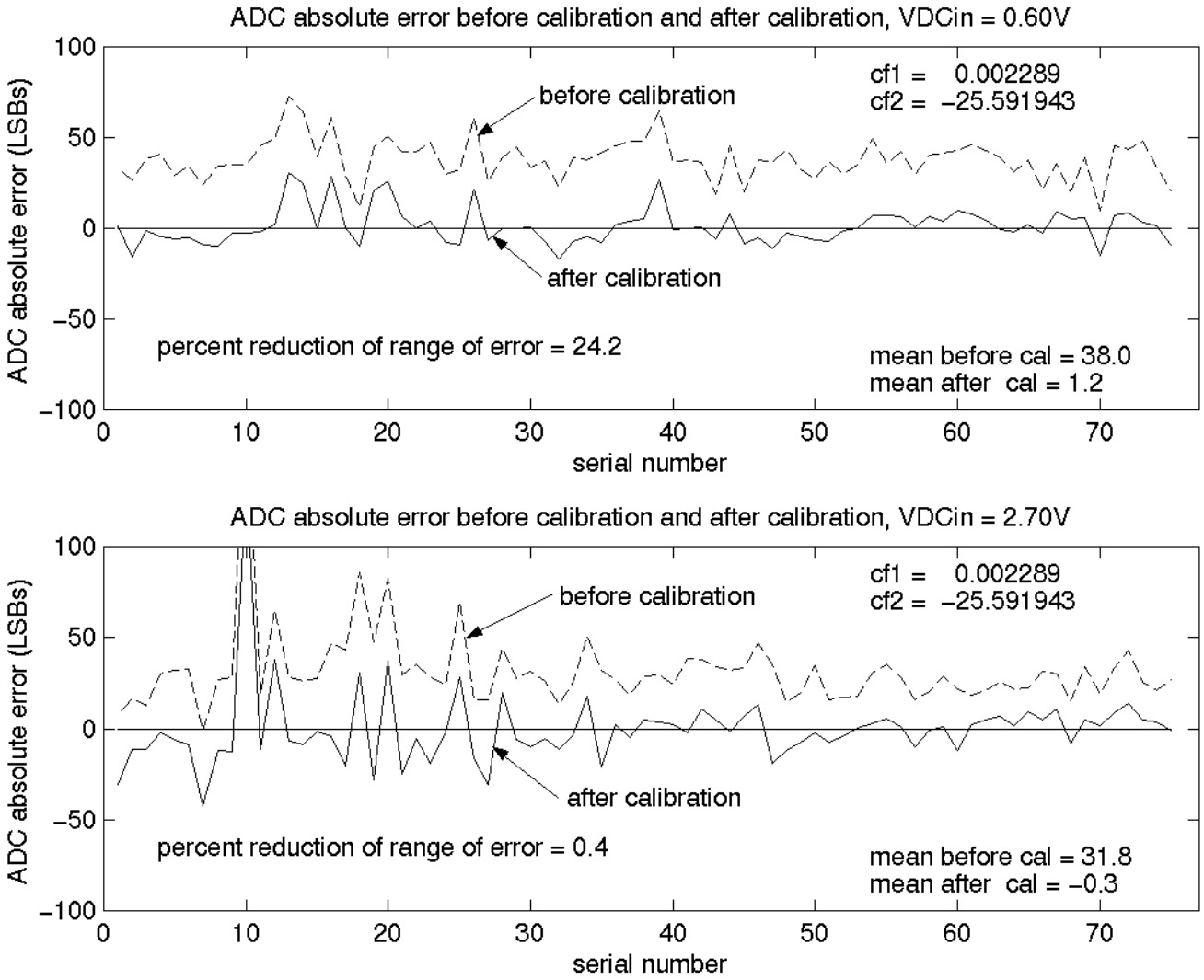

Figure 10-23 ADC Absolute Error Over Processing and Temperature Extremes Before and After Calibration for VDC_{in} = 0.60V and 2.70V

Note: The absolute error data shown in the graphs above reflects the effects of both gain error and offset error. The data was taken on 25 parts: three each from four processing corner lots as well as five from one nominally processed lot, each at three temperatures: -40°C, 27°C, and 150°C (giving the 75 data points shown above), for two input DC voltages: 0.60V and 2.70V. The data indicates that for the given population of parts, calibration significantly reduced (by as much as 24%) the collective variation (spread) of the absolute error of the population. It also significantly reduced (by as much as 38%) the mean (average) of the absolute error and thereby brought it significantly closer to the ideal value of zero. Although not guaranteed, it is believed that calibration will produce results similar to those shown above for any population of parts including those which represent processing and temperature extremes.

- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA} and V_{SSA} pins
- Designs that utilize the $\overline{\text{TRST}}$ pin for JTAG port or EOnCE module functionality (such as development or debugging systems) should allow a means to assert $\overline{\text{TRST}}$ whenever $\overline{\text{RESET}}$ is asserted, as well as a means to assert $\overline{\text{TRST}}$ independently of $\overline{\text{RESET}}$. Designs that do not require debugging functionality, such as consumer products, should tie these pins together.
- Because the Flash memory is programmed through the JTAG/EOnCE port, the designer should provide an interface to this port to allow in-circuit Flash programming

12.3 Power Distribution and I/O Ring Implementation

Figure 12-1 illustrates the general power control incorporated in the 56F8367/56F8167. This chip contains two internal power regulators. One of them is powered from the $V_{DDA\_OSC\_PLL}$ pin and cannot be turned off. This regulator controls power to the internal clock generation circuitry. The other regulator is powered from the V_{DD_IO} pins and provides power to all of the internal digital logic of the core, all peripherals and the internal memories. This regulator can be turned off, if an external V_{DD_CORE} voltage is externally applied to the V_{CAP} pins.

In summary, the entire chip can be supplied from a single 3.3 volt supply if the large core regulator is enabled. If the regulator is not enabled, a dual supply 3.3V/2.5V configuration can also be used.

Notes:

- Flash, RAM and internal logic are powered from the core regulator output
- $V_{PP}1$ and $V_{PP}2$ are not connected in the customer system
- All circuitry, analog *and* digital, shares a common V_{SS} bus

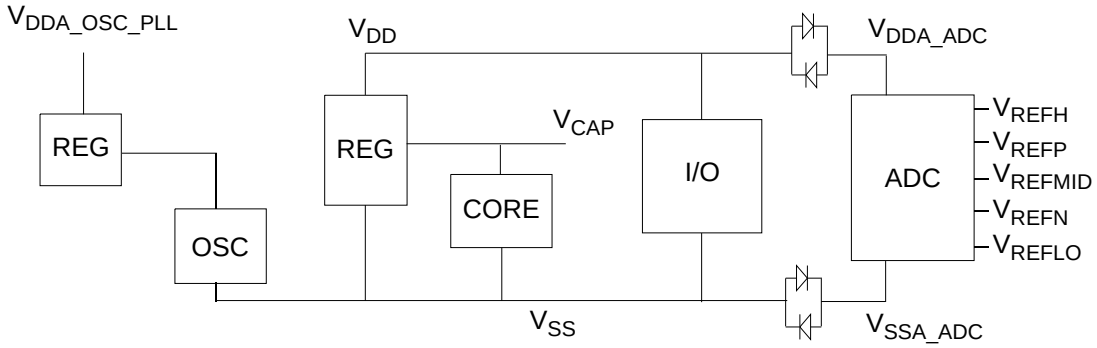

Figure 12-1 Power Management