NXP USA Inc. - MC56F8367VVFE Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	76
Program Memory Size	512KB (256K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	18K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BGA
Supplier Device Package	160-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8367vvfe

Part 1 Overview

1.1 56F8367/56F8167 Features

1.1.1 Core

- Efficient 16-bit 56800E family controller engine with dual Harvard architecture
- Up to 60 Million Instructions Per Second (MIPS) at 60MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- Arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/EOnCE debug programming interface

1.1.2 Differences Between Devices

Table 1-1 outlines the key differences between the 56F8367 and 56F8167 devices.

Table 1-1 Device Differences

Feature	56F8367	56F8167
Guaranteed Speed	60MHz/60 MIPS	40MHZ/40MIPS
Program RAM	4KB	Not Available
Data Flash	32KB	Not Available
PWM	2 x 6	1 x 6
CAN	2	Not Available
Quad Timer	4	2
Quadrature Decoder	2 x 4	1 x 4
Temperature Sensor	1	Not Available
Dedicated GPIO	—	7

1.1.3 Memory

Note: *Features in italics are NOT available in the 56F8167 device.*

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security protection feature
- On-chip memory, including a low-cost, high-volume Flash solution
  - — 512KB of Program Flash
  - — *4KB of Program RAM*
  - — *32KB of Data Flash*
  - — 32KB of Data RAM
  - — 32KB of Boot Flash
- Off-chip memory expansion capabilities provide a simple method for interfacing additional external memory and/or peripheral devices
  - — Access up to 4MB of external program memory or 32MB of external data memory
  - — Chip select logic for glueless interface to ROM and SRAM
- EEPROM emulation capability

1.1.4 Peripheral Circuits

Note: *Features in italics are NOT available in the 56F8167 device.*

- Pulse Width Modulator:
  - — In the 56F8367, two Pulse Width Modulator modules, each with six PWM outputs, three Current Sense inputs, and three Fault inputs; fault-tolerant design with dead time insertion; supports both center-aligned and edge-aligned modes
  - — In the 56F8167, one Pulse Width Modulator module, with six PWM outputs, three Current Sense inputs, and three Fault inputs; fault-tolerant design with dead time insertion; supports both center-aligned and edge-aligned modes
- Four 12-bit, Analog-to-Digital Converters (ADCs), which support four simultaneous conversions with quad, 4-pin multiplexed inputs; ADC and PWM modules can be synchronized through Timer C, channels 2 and 3
- Quadrature Decoder:
  - — In the 56F8367, two four-input Quadrature Decoders or two additional Quad Timers
  - — In the 56F8167, one four-input Quadrature Decoder, which works in conjunction with Quad Timer A
- *Temperature Sensor can be connected, on the board, to any of the ADC inputs to monitor the on-chip temperature*
- Quad Timer:
  - — In the 56F8367, four dedicated general-purpose Quad Timers totaling six dedicated pins: Timer C with two pins and Timer D with four pins
  - — In the 56F8167, two general-purpose Quad Timers; Timer A works in conjunction with Quadrature Decoder 0 or GPIO and Timer C works in conjunction with GPIO
- *Up to two FlexCAN (CAN Version 2.0 B-compliant) modules with 2-pin port for transmit and receive*

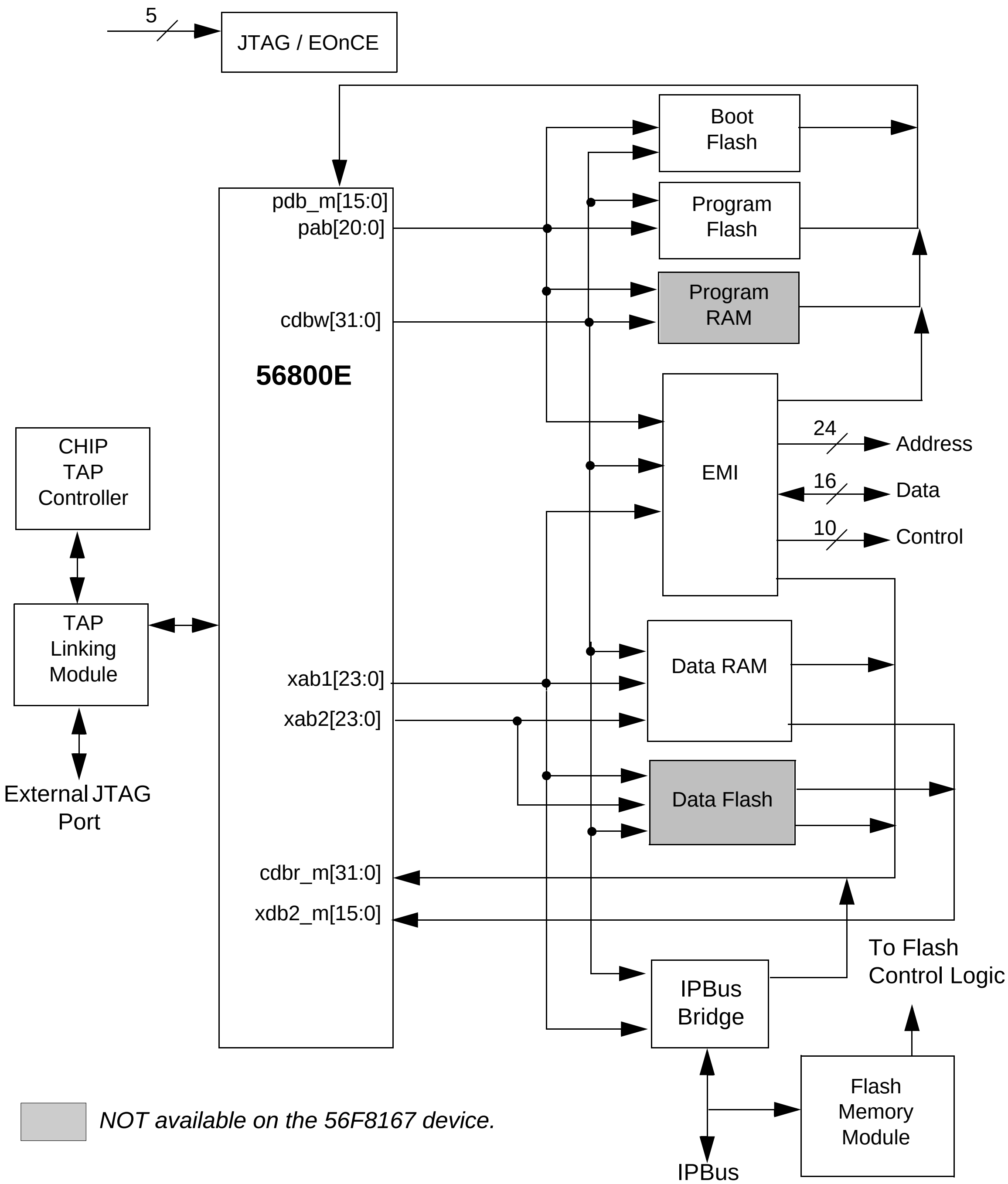


Figure 1-1 System Bus Interfaces

Note: Flash memories are encapsulated within the Flash Memory (FM) Module. Flash control is accomplished by the I/O to the FM over the peripheral bus, while reads and writes are completed between the core and the Flash memories.

Note: The primary data RAM port is 32 bits wide. Other data ports are 16 bits.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the 56F8367 and 56F8167 are organized into functional groups, as detailed in **Table 2-1** and as illustrated in **Figure 2-1**. In **Table 2-2**, each table row describes the signal or signals present on a pin.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins in Package	
	56F8367	56F8167
Power (V_{DD} or V_{DDA})	9	9
Power Option Control	1	1
Ground (V_{SS} or V_{SSA})	7	7
Supply Capacitors[1] & V_{PP}	6	6
PLL and Clock	4	4
Address Bus	24	24
Data Bus	16	16
Bus Control	10	10
Interrupt and Program Control	6	6
Pulse Width Modulator (PWM) Ports	26	13
Serial Peripheral Interface (SPI) Port 0	4	4
Serial Peripheral Interface (SPI) Port 1	—	4
Quadrature Decoder Port 0[2]	4	4
Quadrature Decoder Port 1[3]	4	—
Serial Communications Interface (SCI) Ports[2]	4	4
CAN Ports	2	—
Analog to Digital Converter (ADC) Ports	21	21
Timer Module Ports	6	2
JTAG/Enhanced On-Chip Emulation (EOnCE)	5	5
Temperature Sense	1	—
Dedicated GPIO	—	7

1. If the on-chip regulator is disabled, the V_{CAP} pins serve as 2.5V V_{DD_CORE} power inputs
2. Alternately, can function as Quad Timer pins
3. Pins in this section can function as Quad Timer, SPI #1, or GPIO

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
V_{SS}	27	J4	Supply		V_{SS} — These pins provide ground for chip logic and I/O drivers.
V_{SS}	41	K11			
V_{SS}	74	G11			
V_{SS}	80	E7			
V_{SS}	125	J11			
V_{SS}	160	E6			
V_{SSA_ADC}	115	D12	Supply		**ADC Analog Ground** — This pin supplies an analog ground to the ADC modules.
OCR_DIS	91	K14	Input	Input	**On-Chip Regulator Disable** — Tie this pin to V_{SS} to enable the on-chip regulator Tie this pin to V_{DD} to disable the on-chip regulator **This pin is intended to be a static DC signal from power-up to shut down. Do not try to toggle this pin for power savings during operation.**
V_{CAP}**1***	62	K8	Supply	Supply	V_{CAP}**1 - 4** — When OCR_DIS is tied to V_{SS} (regulator enabled), connect each pin to a 2.2μF or greater bypass capacitor in order to bypass the core logic voltage regulator, required for proper chip operation. When OCR_DIS is tied to V_{DD} (regulator disabled), these pins become V_{DD_CORE} and should be connected to a regulated 2.5V power supply. **Note: This bypass is required even if the chip is powered with an external supply.**
V_{CAP}**2***	144	E8			
V_{CAP}**3***	95	H11			
V_{CAP}**4***	15	G4			
* When the on-chip regulator is disabled, these four pins become 2.5V V_{DD_CORE}.					
V_{PP}**1**	141	A7	Input	Input	V_{PP}**1 - 2** — These pins should be left unconnected as an open circuit for normal functionality.
V_{PP}**2**	2	C2			
CLKMODE	99	H12	Input	Input	**Clock Input Mode Selection** — This input determines the function of the XTAL and EXTAL pins. 1 = External clock input on XTAL is used to directly drive the input clock of the chip. The EXTAL pin should be grounded. 0 = A crystal or ceramic resonator should be connected between XTAL and EXTAL.
EXTAL	94	J12	Input	Input	**External Crystal Oscillator Input** — This input can be connected to an 8MHz external crystal. Tie this pin low if XTAL is driven by an external clock source.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
A6 **(GPIOE2)**	17	G1	Output Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**Address Bus** — A6 - A7 specify two of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A6 - A7 and EMI control signals are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. **Port E GPIO** — These two GPIO pins can be individually programmed as input or output pins. After reset, the default state is Address Bus. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOE_PUR register. Example: GPIOE2, clear bit 2 in the GPIOE_PUR register.
A7 **(GPIOE3)**	18	G3			
A8 **(GPIOA0)**	19	G2	Output Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**Address Bus**— A8 - A15 specify eight of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A8 - A15 and EMI control signals are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. **Port A GPIO** — These eight GPIO pins can be individually programmed as input or output pins. After reset, the default state is Address Bus. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOA_PUR register. Example: GPIOA0, clear bit 0 in the GPIOA_PUR register.
A9 **(GPIOA1)**	20	H1			
A10 **(GPIOA2)**	21	H2			
A11 **(GPIOA3)**	22	H4			
A12 **(GPIOA4)**	23	H3			
A13 **(GPIOA5)**	24	J1			
A14 **(GPIOA6)**	25	J2			
A15 **(GPIOA7)**	26	J3			

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
ISB0 **(GPIOD10)**	61	N8	Schmitt Input Schmitt Input/ Output	Input, pull-up enabled	**ISB0 - 2** — These three input current status pins are used for top/bottom pulse width correction in complementary channel operation for PWMB. **Port D GPIO** — These GPIO pins can be individually programmed as input or output pins. At reset, these pins default to ISB functionality. To deactivate the internal pull-up resistor, clear the appropriate bit of the GPIOD_PUR register. For details, see **Part 6.5.8**.
ISB1 (GPIOD11)	63	L8			
ISB2 (GPIOD12)	64	P8			
FAULTB0	67	N9	Schmitt Input	Input, pull-up enabled	**FAULTB0 - 3** — These four fault input pins are used for disabling selected PWMB outputs in cases where fault conditions originate off-chip. To deactivate the internal pull-up resistor, set the PWMB bit in the SIM_PUDR register. For details, see **Part 6.5.8**.
FAULTB1	68	L9			
FAULTB2	69	L10			
FAULTB3	72	P11			
ANA0	100	G13	Input	Analog Input	**ANA0 - 3** — Analog inputs to ADC A, channel 0
ANA1	101	H13			
ANA2	102	G12			
ANA3	103	F13			
ANA4	104	F12	Input	Analog Input	**ANA4 - 7** — Analog inputs to ADC A, channel 1
ANA5	105	H14			
ANA6	106	G14			
ANA7	107	E13			
V_{REFH}	113	D14	Input	Analog Input	V_{REFH} — Analog Reference Voltage High. V_{REFH} must be less than or equal to V_{DDA_ADC}.
V_{REFP}	112	D13	Input/ Output	Analog Input/ Output	V_{REFP}, V_{REFMID} & V_{REFN} — Internal pins for voltage reference which are brought off-chip so they can be bypassed. Connect to a 0.1μF low ESR capacitor.
V_{REFMID}	111	E14			
V_{REFN}	110	F14			
V_{REFLO}	109	E12	Input	Analog Input	V_{REFLO} — Analog Reference Voltage Low. This should normally be connected to a low-noise V_{SS}.

Table 2-2 Signal and Package Information for the 160-Pin LQFP and MBGA (Continued)

Signal Name	Pin No.	*Ball No.*	Type	State During Reset	Signal Description
TD0 **(GPIOE10)**	129	B10	Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**TD0 - 3**— Timer D, Channels 0, 1, 2 and 3 **Port E GPIO** — These GPIO pins can be individually programmed as input or output pins. At reset, these pins default to Timer functionality. To deactivate the internal pull-up resistor, clear the appropriate bit of the GPIOE_PUR register. See **Part 6.5.6** for details.
TD1 **(GPIOE11)**	130	A10			
TD2 **(GPIOE12)**	131	D10			
TD3 **(GPIOE13)**	132	E10			
IRQA	65	K9	Schmitt Input	Input, pull-up enabled	**External Interrupt Request A and B** — The IRQA and IRQB inputs are asynchronous external interrupt requests during Stop and Wait mode operation. During other operating modes, they are synchronized external interrupt requests, which indicate an external device is requesting service. They can be programmed to be level-sensitive or negative-edge triggered. To deactivate the internal pull-up resistor, set the IRQ bit in the SIM_PUDR register. See **Part 6.5.6** for details.
IRQB	66	P9			
RESET	98	J14	Schmitt Input	Input, pull-up enabled	**Reset** — This input is a direct hardware reset on the processor. When RESET is asserted low, the device is initialized and placed in the reset state. A Schmitt trigger input is used for noise immunity. When the RESET pin is deasserted, the initial chip operating mode is latched from the EXTBOOT pin. The internal reset signal will be deasserted synchronous with the internal clocks after a fixed number of internal clocks. To ensure complete hardware reset, RESET and TRST should be asserted together. The only exception occurs in a debugging environment when a hardware device reset is required and the JTAG/EOnCE module must not be reset. In this case, assert RESET but do not assert TRST. **Note:** The internal Power-On Reset will assert on initial power-up. To deactivate the internal pull-up resistor, set the RESET bit in the SIM_PUDR register. See **Part 6.5.6** for details.
RSTO	97	J13	Output	Output	**Reset Output** — This output reflects the internal reset state of the chip.

Table 4-4 Program Memory Map at Reset

Begin/End Address	Mode 0 (MA = 0)	Mode 1[1] (MA = 1)	
	Internal Boot	External Boot	
	Internal Boot 16-Bit External Address Bus	EMI_MODE = 0[2,3] 16-Bit External Address Bus	EMI_MODE = 1[4] 20-Bit External Address Bus
P:$1F FFFF P:$10 0000	External Program Memory[5]	External Program Memory[5]	External Program Memory[6]
P:$0F FFFF P:$05 0000			External Program Memory COP Reset Address = 04 0002[7] Boot Location = 04 0000[7]
P:$04 FFFF P:$04 F800	*On-Chip Program RAM* 4KB		
P:$04 F7FF P:$04 4000	Reserved 92KB		
P:$04 3FFF P:$04 0000	Boot Flash 32KB COP Reset Address = 04 0002 Boot Location = 04 0000	Boot Flash 32KB (Not Used for Boot in this Mode)	
P:$03 FFFF P:$02 0000	Internal Program Flash[8] 256KB	Internal Program Flash 256KB	
P:$01 FFFF P:$01 0000	Internal Program Flash[8] 256KB	Internal Program Flash 128KB	
P:$00 FFFF P:$00 0000		External Program Memory COP Reset Address = 00 0002 Boot Location = 00 0000	

1. If Flash Security Mode is enabled, EXTBOOT Mode 1 cannot be used. See **Security Features,** Part 7.
2. This mode provides maximum compatibility with 56F80x parts while operating externally.
3. "EMI_MODE = 0" when EMI_MODE pin is tied to ground at boot up.
4. "EMI_MODE = 1" when EMI_MODE pin is tied to V_{DD} at boot up.
5. Not accessible in reset configuration, since the address is above P:$00 FFFF. The higher bit address/GPIO (and/or chip selects) pins must be reconfigured before this external memory is accessible.
6. Not accessible in reset configuration, since the address is above P:$0F FFFF. The higher bit address/GPIO (and/or chip selects) pins must be reconfigured before this external memory is accessible.
7. Booting from this external address allows prototyping of the internal Boot Flash.
8. Two independent program flash blocks allow one to be programmed/erased while executing from another. Each block must have its own mass erase.

4.3 Interrupt Vector Table

Table 4-5 provides the reset and interrupt priority structure, including on-chip peripherals. The table is organized with higher-priority vectors at the top and lower-priority interrupts lower in the table. The priority of an interrupt can be assigned to different levels, as indicated, allowing some control over interrupt priorities. All level 3 interrupts will be serviced before level 2, and so on. For a selected priority level, the lowest vector number has the highest priority.

Part 5 Interrupt Controller (ITCN)

5.1 Introduction

The Interrupt Controller (ITCN) module is used to arbitrate between various interrupt requests (IRQs), to signal to the 56800E core when an interrupt of sufficient priority exists, and what address to jump in order to service this interrupt.

5.2 Features

The ITCN module design includes these distinctive features:

- Programmable priority levels for each IRQ
- Two programmable Fast Interrupts
- Notification to SIM module to restart clocks out of Wait and Stop modes
- Drives initial address on the address bus after reset

For further information, see **Table 4-5**, Interrupt Vector Table Contents.

5.3 Functional Description

The Interrupt Controller is a slave on the IPBus. It contains registers allowing each of the 86 interrupt sources to be set to one of four priority levels, excluding certain interrupts of fixed priority. Next, all of the interrupt requests of a given level are priority encoded to determine the lowest numerical value of the active interrupt requests for that level. Within a given priority level, 0 is the highest priority, while number 85 is the lowest.

5.3.1 Normal Interrupt Handling

Once the ITCN has determined that an interrupt is to be serviced and which interrupt has the highest priority, an interrupt vector address is generated. Normal interrupt handling concatenates the VBA and the vector number to determine the vector address. In this way, an offset is generated into the vector table for each interrupt.

5.3.2 Interrupt Nesting

Interrupt exceptions may be nested to allow an IRQ of higher priority than the current exception to be serviced. The following tables define the nesting requirements for each priority level.

Table 5-1 Interrupt Mask Bit Definition

SR[9][1]	SR[8][1]	Permitted Exceptions	Masked Exceptions
0	0	Priorities 0, 1, 2, 3	None
0	1	Priorities 1, 2, 3	Priority 0
1	0	Priorities 2, 3	Priorities 0, 1
1	1	Priority 3	Priorities 0, 1, 2

1. Core status register bits indicating current interrupt mask within the core.

Add. Offset	Register Name		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	IPR0	R	0	0	BKPT_U0 IPL		STPCNT IPL		0	0	0	0	0	0	0	0	0	0
		W																
$1	IPR1	R	0	0	0	0	0	0	0	0	0	0	RX_REG IPL		TX_REG IPL		TRBUF IPL	
		W																
$2	IPR2	R	FMCBE IPL		FMCC IPL		FMERR IPL		LOCK IPL		LVI IPL		0	0	IRQB IPL		IRQA IPL	
		W																
$3	IPR3	R	GPIOD IPL		GPIOE IPL		GPIOF IPL		FCMSGBUF IPL		FCWKUP IPL		FCERR IPL		FCBOFF IPL		0	0
		W																
$4	IPR4	R	SPI0_RCV IPL		SPI1_XMIT IPL		SPI1_RCV IPL		0	0	0	0	GPIOA IPL		GPIOB IPL		GPIOC IPL	
		W																
$5	IPR5	R	DEC1_XIRQ IPL		DEC1_HIRQ IPL		SCI1_RCV IPL		SCI1_RERR IPL		0	0	SCI1_TIDL IPL		SCI1_XMIT IPL		SPI0_XMIT IPL	
		W																
$6	IPR6	R	TMRC0 IPL		TMRD3 IPL		TMRD2 IPL		TMRD1 IPL		TMRD0 IPL		0	0	DEC0_XIRQ IPL		DEC0_HIRQ IPL	
		W																
$7	IPR7	R	TMRA0 IPL		TMRB3 IPL		TMRB2 IPL		TMRB1 IPL		TMRB0 IPL		TMRC3 IPL		TMRC2 IPL		TMRC1 IPL	
		W																
$8	IPR8	R	SCI0_RCV IPL		SCI0_RERR IPL		0	0	SCI0_TIDL IPL		SCI0_XMIT IPL		TMRA3 IPL		TMRA2 IPL		TMRA1 IPL	
		W																
$9	IPR9	R	PWMA F IPL		PWMB F IPL		PWMA_RL IPL		PWMB_RL IPL		ADCA_ZC IPL		ABCB_ZC IPL		ADCA_CC IPL		ADCB_CC IPL	
		W																
$A	VBA	R	0	0	0	VECTOR BASE ADDRESS												
		W																
$B	VBA0	R	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0						
		W																
$C	FIVAL0	R	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
		W																
$D	FIVAH0	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
		W																
$E	FIM1	R	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1						
		W																
$F	FIVAL1	R	FAST INTERRUPT 1 VECTOR ADDRESS LOW															
		W																
$10	FIVAH1	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1 VECTOR ADDRESS HIGH				
		W																
$11	IRQP0	R	PENDING [16:2]															1
		W																
$12	IRQP1	R	PENDING [32:17]															
		W																
$13	IRQP2	R	PENDING [48:33]															
		W																
$14	IRQP3	R	PENDING [64:49]															
		W																
$15	IRQP4	R	PENDING [80:65]															
		W																
$16	IRQP5	R	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	PENDING [81]
		W																
	Reserved																	
$1D	ICTL	R	INT	IPIC		VAB							INT_DIS	1	IRQB STATE	IRQA STATE	$\overline{IRQB}$ EDG	$\overline{IRQA}$ EDG
		W																
	Reserved																	
$1F	IPR10	R	0	0	0	0	0	0	0	0	FLEXCAN2 MSGBUG IPL		FLEXCAN2 WKUP IPL		FLEXCAN2 ERR IPL		FLEXCAN2 BOFF IPL	
		W																

= Reserved

Figure 5-2 ITCN Register Map Summary

5.6.4.7 FlexCAN Bus Off Interrupt Priority Level (FCBOFF IPL)— Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.8 Reserved—Bits 1–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.5 Interrupt Priority Register 4 (IPR4)

Base + $4	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	SPI0_RCV IPL		SPI1_XMIT IPL		SPI1_RCV IPL		0	0	0	0	GPIOA IPL		GPIOB IPL		GPIOC IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-7 Interrupt Priority Register 4 (IPR4)

5.6.5.1 SPI0 Receiver Full Interrupt Priority Level (SPI0_RCV IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.2 SPI1 Transmit Empty Interrupt Priority Level (SPI1_XMIT IPL)— Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.8 ADC B Conversion Complete Interrupt Priority Level (ADCB_CC IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.11 Vector Base Address Register (VBA)

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	VECTOR BASE ADDRESS												
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-13 Vector Base Address Register (VBA)

5.6.11.1 Reserved—Bits 15–13

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.11.2 Interrupt Vector Base Address (VECTOR BASE ADDRESS)—Bits 12–0

The contents of this register determine the location of the Vector Address Table. The value in this register is used as the upper 13 bits of the interrupt Vector Address Bus (VAB[20:0]). The lower eight bits are determined based upon the highest-priority interrupt. They are then appended onto VBA before presenting the full VAB to the 56800E core; see **Part 5.3.1** for details.

5.6.12 Fast Interrupt 0 Match Register (FIM0)

Base + $B	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0						
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-14 Fast Interrupt 0 Match Register (FIM0)

5.6.12.1 Reserved—Bits 15–7

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.12.2 Fast Interrupt 0 Vector Number (FAST INTERRUPT 0)—Bits 6–0

This value determines which IRQ will be a Fast Interrupt 0. Fast interrupts vector directly to a service routine based on values in the Fast Interrupt Vector Address registers without having to go to a jump table first; see **Part 5.3.3**. IRQs used as fast interrupts *must* be set to priority level 2. Unexpected results will occur if a fast interrupt vector is set to any other priority. Fast interrupts automatically become the highest-priority level 2 interrupt, regardless of their location in the interrupt table, prior to being declared as fast interrupt. Fast interrupt 0 has priority over Fast Interrupt 1. To determine the vector number of each IRQ, refer to **Table 4-5**.

5.6.13 Fast Interrupt 0 Vector Address Low Register (FIVAL0)

Base + $C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-15 Fast Interrupt 0 Vector Address Low Register (FIVAL0)

5.6.13.1 Fast Interrupt 0 Vector Address Low (FIVAL0)—Bits 15–0

The lower 16 bits of the vector address are used for Fast Interrupt 0. This register is combined with FIVAH0 to form the 21-bit vector address for Fast Interrupt 0 defined in the FIM0 register.

5.6.14 Fast Interrupt 0 Vector Address High Register (FIVAH0)

Base + $D	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-16 Fast Interrupt 0 Vector Address High Register (FIVAH0)

5.6.14.1 Reserved—Bits 15–5

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.14.2 Fast Interrupt 0 Vector Address High (FIVAH0)—Bits 4–0

The upper five bits of the vector address are used for Fast Interrupt 0. This register is combined with FIVAL0 to form the 21-bit vector address for Fast Interrupt 0 defined in the FIM0 register.

5.6.15 Fast Interrupt 1 Match Register (FIM1)

Base + $E	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1						
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-17 Fast Interrupt 1 Match Register (FIM1)

5.6.15.1 Reserved—Bits 15–7

This bit field is reserved or not implemented. It is read as 0, but cannot be modified by writing.

Add. Offset	Register Name		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	SIM_ CONTROL	R	0	0	0	0	0	0	0	0	0	EMI_ MODE	ONCE EBL	SW RST	STOP_ DISABLE		WAIT_ DISABLE	
		W																
$1	SIM_ RSTSTS	R	0	0	0	0	0	0	0	0	0	0	SWR	COPR	EXTR	POR	0	0
		W																
$2	SIM_SCR0	R	FIELD															
		W																
$3	SIM_SCR1	R	FIELD															
		W																
$4	SIM_SCR2	R	FIELD															
		W																
$5	SIM_SCR3	R	FIELD															
		W																
$6	SIM_MSH_ ID	R	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	0
		W																
$7	SIM_LSH_ID	R	1	1	0	1	0	0	0	0	0	0	0	1	1	1	0	1
		W																
$8	SIM_PUDR	R	0	PWMA 1	CAN	EMI_ MODE	$\overline{\text{RESET}}$	IRQ	XBOOT	PWMB	PWMA 0	0	CTRL	0	JTAG	0	0	0
		W																
	Reserved																	
$A	SIM_ CLKOSR	R	0	0	0	0	0	0	$\overline{\text{A23}}$	$\overline{\text{A22}}$	$\overline{\text{A21}}$	$\overline{\text{A20}}$	CLKDIS	CLKOSEL				
		W																
$B	SIM_GPS	R	0	0	0	0	0	0	0	0	0	0	D1	D0	C3	C2	C1	C0
		W																
$C	SIM_PCE	R	EMI	ADCB	ADCA	CAN	DEC1	DEC0	TMRD	TMRC	TMRB	TMRA	SCI1	SCI0	SPI1	SPI0	PWM B	PWM A
		W																
$D	SIM_ISALH	R	1	1	1	1	1	1	1	1	1	1	1	1	1	1	ISAL[23:22]	
		W																
$E	SIM_ISALL	R	ISAL[21:6]															
		W																
$F	SIM_PCE2	R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CAN2
		W																

= Reserved

Figure 6-2 SIM Register Map Summary

6.5.1 SIM Control Register (SIM_CONTROL)

Base + $0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	EMI_ MODE	ONCE EBL	SW RST	STOP_ DISABLE		WAIT_ DISABLE	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-3 SIM Control Register (SIM_CONTROL)

6.5.1.1 Reserved—Bits 15–7

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.2.1 Reserved—Bits 15–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.2.2 Software Reset (SWR)—Bit 5

When 1, this bit indicates that the previous reset occurred as a result of a software reset (write to SW RST bit in the SIM_CONTROL register). This bit will be cleared by any hardware reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit will clear it.

6.5.2.3 COP Reset (COPR)—Bit 4

When 1, the COPR bit indicates the Computer Operating Properly (COP) timer-generated reset has occurred. This bit will be cleared by a Power-On Reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit will clear it.

6.5.2.4 External Reset (EXTR)—Bit 3

If 1, the EXTR bit indicates an external system reset has occurred. This bit will be cleared by a Power-On Reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit position will clear it. Basically, when the EXTR bit is 1, the previous system reset was caused by the external RESET pin being asserted low.

6.5.2.5 Power-On Reset (POR)—Bit 2

When 1, the POR bit indicates a Power-On Reset occurred some time in the past. This bit can only be cleared by software or by another type of reset. Writing a 0 to this bit will set the bit while writing a 1 to the bit position will clear the bit. In summary, if the bit is 1, the previous system reset was due to a Power-On Reset.

6.5.2.6 Reserved—Bits 1–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.3 SIM Software Control Registers (SIM_SCR0, SIM_SCR1, SIM_SCR2, and SIM_SCR3)

Only SIM_SCR0 is shown below. SIM_SCR1, SIM_SCR2, and SIM_SCR3 are identical in functionality.

Base + $2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FIELD															
Write																
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-5 SIM Software Control Register 0 (SIM_SCR0)

6.5.3.1 Software Control Data 1 (FIELD)—Bits 15–0

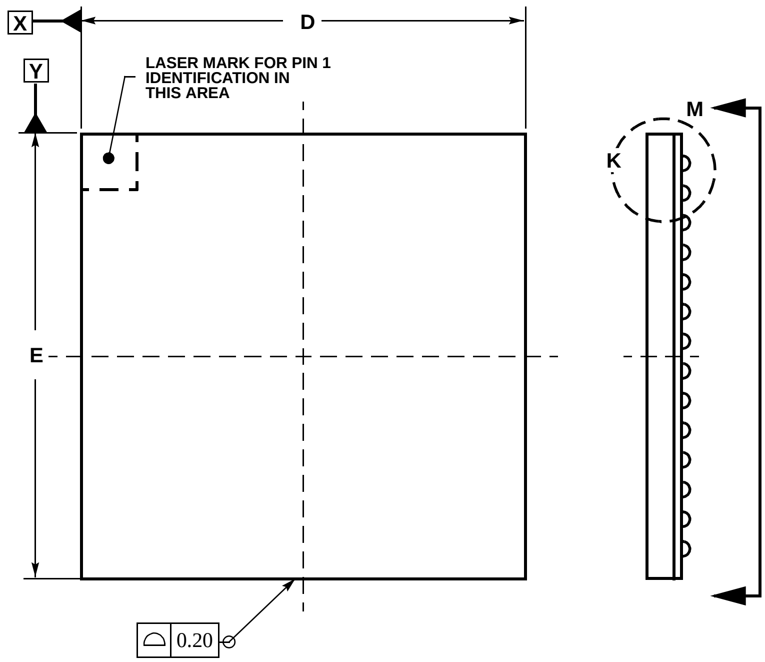
This register is reset only by the Power-On Reset (POR). It has no part-specific functionality and is intended for use by a software developer to contain data that will be unaffected by the other reset sources (RESET pin, software reset, and COP reset).

Table 8-3 GPIO External Signals Map (Continued)
Pins in italics are NOT available in the 56F8167 device

GPIO Port	GPIO Bit	Reset Function	Functional Signal	Package Pin
GPIOB	0	GPIO[1]	A16	33
	1	GPIO[1]	A17	34
	2	GPIO[1]	A18	35
	3	GPIO[1]	A19	36
	4	GPIO	A20 / Prescaler_clock	37
	5	GPIO	A21 / SYS_CLK	46
	6	GPIO	A22 / SYS_CLK2	47
	7	GPIO	A23 / Oscillator_Clock	48
[1]This is a function of the EMI_MODE, EXTBOOT, and Flash security settings at reset.				
GPIOC	0	Peripheral	*PhaseA1 / TB0* / SCLK1[1]	6
	1	Peripheral	*PhaseB1 / TB1* / MOSI1[1]	7
	2	Peripheral	*Index1 / TB2* / MISO1[1]	8
	3	Peripheral	*Home1 / TB3* / $\overline{\text{SSI1}}$[1]	9
	4	Peripheral	PHASEA0 / TA0	155
	5	Peripheral	PHASEB0 / TA1	156
	6	Peripheral	Index0 / TA2	157
	7	Peripheral	Home0 / TA3	158
	8	Peripheral	*ISA0*	126
	9	Peripheral	*ISA1*	127
	10	Peripheral	*ISA2*	128

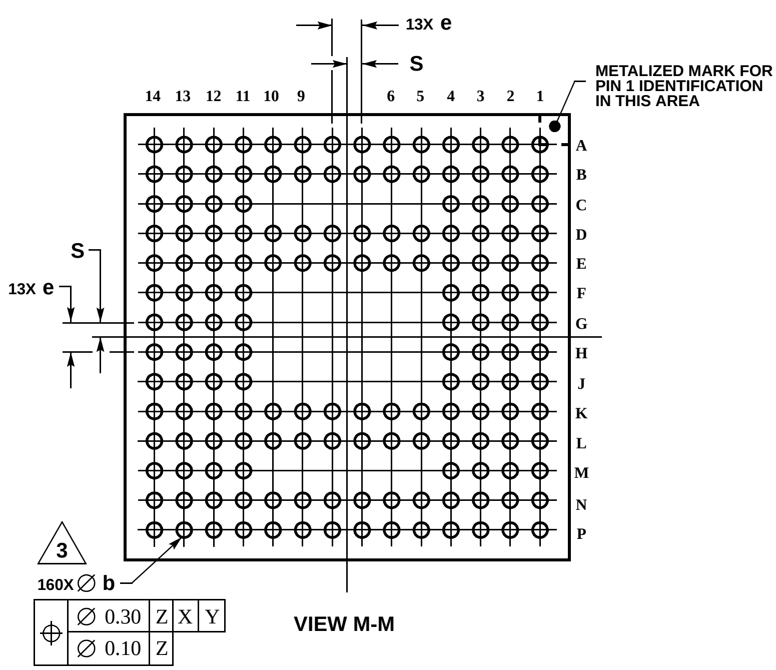
Table 8-3 GPIO External Signals Map (Continued)
Pins in italics are NOT available in the 56F8167 device

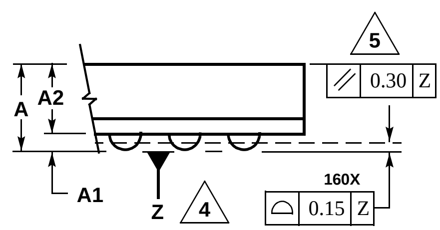
GPIO Port	GPIO Bit	Reset Function	Functional Signal	Package Pin
GPIOD	0	GPIO	$\overline{CS2}$ / *CAN2_TX*	55
	1	GPIO	$\overline{CS3}$ / *CAN2_RX*	56
	2	GPIO	$\overline{CS4}$	57
	3	GPIO	$\overline{CS5}$	58
	4	GPIO	$\overline{CS6}$	59
	5	GPIO	$\overline{CS7}$	60
	6	Peripheral	TXD1	49
	7	Peripheral	RXD1	50
	8	Peripheral	$\overline{PS}$ / $\overline{CS0}$	53
	9	Peripheral	$\overline{DS}$ / $\overline{CS1}$	54
	10	Peripheral	ISB0	61
	11	Peripheral	ISB1	63
	12	Peripheral	ISB2	64
GPIOE	0	Peripheral	TXD0	4
	1	Peripheral	RXD0	5
	2	Peripheral	A6	17
	3	Peripheral	A7	18
	4	Peripheral	SCLK0	146
	5	Peripheral	MOSI0	148
	6	Peripheral	MISO0	147
	7	Peripheral	$\overline{SS0}$	145
	8	Peripheral	TC0	133
	9	Peripheral	TC1	135
	10	Peripheral	*TD0*	129
	11	Peripheral	*TD1*	130
	12	Peripheral	*TD2*	131
	13	Peripheral	*TD3*	132



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	1.32	1.75
A1	0.27	0.47
A2	1.18 REF	
b	0.35	0.65
D	15.00 BSC	
E	15.00 BSC	
e	1.00 BSC	
S	0.50 BSC	





DETAIL K
ROTATED 90° CLOCKWISE

CASE 1268-01
ISSUE O

Figure 11-3 160 MAPBGA Mechanical Information

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