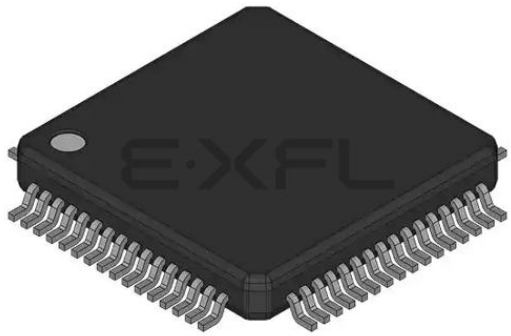

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	I²C, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	32
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at91sam7s128c-au

- **Fully Static Operation: Up to 55 MHz at 1.65V and 85° C Worst Case Conditions**
- **Available in 64-lead LQFP Green or 64-pad QFN Green Package (SAM7S512/256/128/64/321/161) and 48-lead LQFP Green or 48-pad QFN Green Package (SAM7S32/16)**

1. Description

Atmel's SAM7S is a series of low pincount Flash microcontrollers based on the 32-bit ARM RISC processor. It features a high-speed Flash and an SRAM, a large set of peripherals, including a USB 2.0 device (except for the SAM7S32 and SAM7S16), and a complete set of system functions minimizing the number of external components. The device is an ideal migration path for 8-bit microcontroller users looking for additional performance and extended memory.

The embedded Flash memory can be programmed in-system via the JTAG-ICE interface or via a parallel interface on a production programmer prior to mounting. Built-in lock bits and a security bit protect the firmware from accidental overwrite and preserves its confidentiality.

The SAM7S Series system controller includes a reset controller capable of managing the power-on sequence of the microcontroller and the complete system. Correct device operation can be monitored by a built-in brownout detector and a watchdog running off an integrated RC oscillator.

The SAM7S Series are general-purpose microcontrollers. Their integrated USB Device port makes them ideal devices for peripheral applications requiring connectivity to a PC or cellular phone. Their aggressive price point and high level of integration pushes their scope of use far into the cost-sensitive, high-volume consumer market.

1.1 Configuration Summary of the SAM7S512, SAM7S256, SAM7S128, SAM7S64, SAM7S321, SAM7S32, SAM7S161 and SAM7S16

The SAM7S512, SAM7S256, SAM7S128, SAM7S64, SAM7S321, SAM7S32, SAM7S161 and SAM7S16 differ in memory size, peripheral set and package. Table 1-1 summarizes the configuration of the six devices.

Except for the SAM7S32/16, all other SAM7S devices are package and pinout compatible.

Table 1-1. Configuration Summary

SAM7S512	512 Kbytes	Master	dual plane	64 Kbytes	1	2(1) (2)	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S256	256 Kbytes	Master	single plane	64 Kbytes	1	2(1) (2)	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S128	128 Kbytes	Master	single plane	32 Kbytes	1	2(1) (2)	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S64	64 Kbytes	Master	single plane	16 Kbytes	1	2(2)	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S321	32 Kbytes	Master	single plane	8 Kbytes	1	2(2)	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S32	32 Kbytes	Master	single plane	8 Kbytes	not present	1	1	9	3(3)	Yes	21	LQFP/ QFN 48
SAM7S161	16 Kbytes	Master/ Slave	single plane	4 Kbytes	1	2(2)	2	11	3	No	32	LQFP
SAM7S16	16 Kbytes	Master/ Slave	single plane	4 Kbytes	not present	1	1	9	3(3)	No	21	LQFP/ QFN 48

Notes: 1. Fractional Baud Rate.
2. Full modem line support on USART1.
3. Only two TC channels are accessible through the PIO.

2. Block Diagram

Figure 2-1. SAM7S512/256/128/64/321/161 Block Diagram

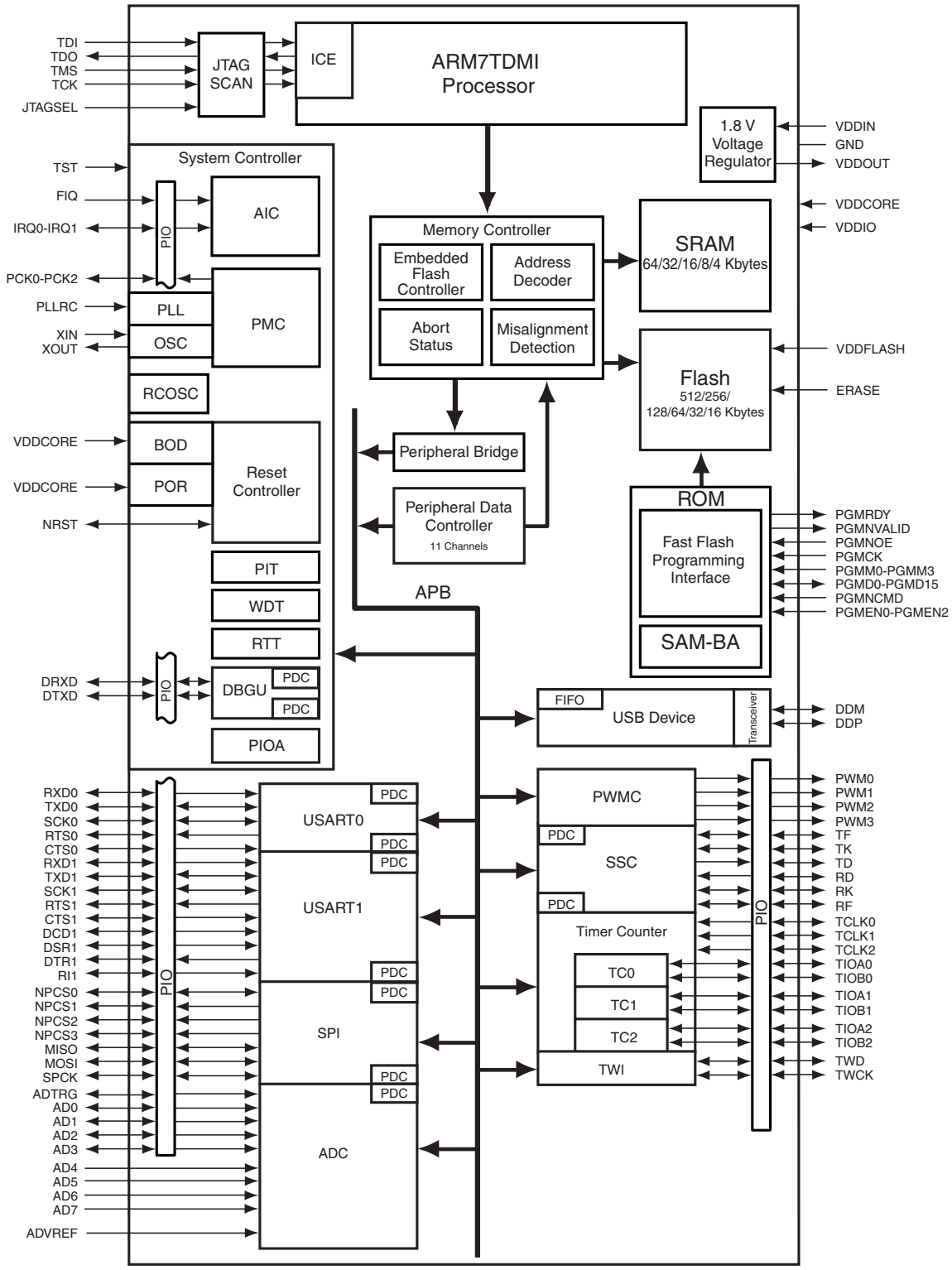


Table 3-1. Signal Description List (Continued)

DDM	USB Device Port Data -	Analog		not present on SAM7S32/16
DDP	USB Device Port Data +	Analog		not present on SAM7S32/16
SCK0 - SCK1	Serial Clock	I/O		SCK1 not present on SAM7S32/16
TXD0 - TXD1	Transmit Data	I/O		TXD1 not present on SAM7S32/16
RXD0 - RXD1	Receive Data	Input		RXD1 not present on SAM7S32/16
RTS0 - RTS1	Request To Send	Output		RTS1 not present on SAM7S32/16
CTS0 - CTS1	Clear To Send	Input		CTS1 not present on SAM7S32/16
DCD1	Data Carrier Detect	Input		not present on SAM7S32/16
DTR1	Data Terminal Ready	Output		not present on SAM7S32/16
DSR1	Data Set Ready	Input		not present on SAM7S32/16
RI1	Ring Indicator	Input		not present on SAM7S32/16
TD	Transmit Data	Output		
RD	Receive Data	Input		
TK	Transmit Clock	I/O		
RK	Receive Clock	I/O		
TF	Transmit Frame Sync	I/O		
RF	Receive Frame Sync	I/O		
TCLK0 - TCLK2	External Clock Inputs	Input		TCLK1 and TCLK2 not present on SAM7S32/16
TIOA0 - TIOA2	I/O Line A	I/O		TIOA2 not present on SAM7S32/16
TIOB0 - TIOB2	I/O Line B	I/O		TIOB2 not present on SAM7S32/16
PWM0 - PWM3	PWM Channels	Output		
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
SPCK	SPI Serial Clock	I/O		
NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
NPCS1-NPCS3	SPI Peripheral Chip Select 1 to 3	Output	Low	

4. Package and Pinout

The SAM7S512/256/128/64/321 are available in a 64-lead LQFP or 64-pad QFN package.

The SAM7S161 is available in a 64-Lead LQFP package.

The SAM7S32/16 are available in a 48-lead LQFP or 48-pad QFN package.

4.1 64-lead LQFP and 64-pad QFN Package Outlines

Figure 4-1 and Figure 4-2 show the orientation of the 64-lead LQFP and the 64-pad QFN package. A detailed mechanical description is given in the section Mechanical Characteristics of the full datasheet.

Figure 4-1. 64-lead LQFP Package (Top View)

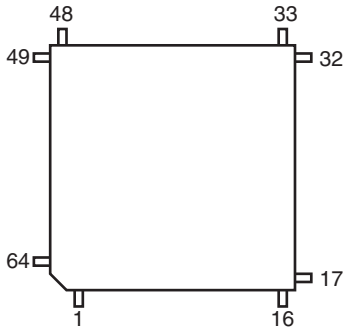
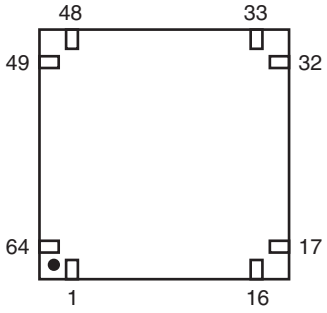


Figure 4-2. 64-pad QFN Package (Top View)



4.2 64-lead LQFP and 64-pad QFN Pinout

Table 4-1. SAM7S512/256/128/64/321/161 Pinout[1]

1	ADVREF	17	GND	33	TDI	49	TDO
2	GND	18	VDDIO	34	PA6/PGMNOE	50	JTAGSEL
3	AD4	19	PA16/PGMD4	35	PA5/PGMRDY	51	TMS
4	AD5	20	PA15/PGMD3	36	PA4/PGMNCMD	52	PA31
5	AD6	21	PA14/PGMD2	37	PA27/PGMD15	53	TCK
6	AD7	22	PA13/PGMD1	38	PA28	54	VDDCORE
7	VDDIN	23	PA24/PGMD12	39	NRST	55	ERASE
8	VDDOUT	24	VDDCORE	40	TST	56	DDM
9	PA17/PGMD5/AD0	25	PA25/PGMD13	41	PA29	57	DDP
10	PA18/PGMD6/AD1	26	PA26/PGMD14	42	PA30	58	VDDIO
11	PA21/PGMD9	27	PA12/PGMD0	43	PA3	59	VDDFLASH
12	VDDCORE	28	PA11/PGMM3	44	PA2/PGMEN2	60	GND
13	PA19/PGMD7/AD2	29	PA10/PGMM2	45	VDDIO	61	XOUT
14	PA22/PGMD10	30	PA9/PGMM1	46	GND	62	XIN/PGMCK
15	PA23/PGMD11	31	PA8/PGMM0	47	PA1/PGMEN1	63	PLLRC
16	PA20/PGMD8/AD3	32	PA7/PGMNVALID	48	PA0/PGMEN0	64	VDDPLL

Note: 1. The bottom pad of the QFN package must be connected to ground.

4.3 48-lead LQFP and 48-pad QFN Package Outlines

Figure 4-3 and Figure 4-4 show the orientation of the 48-lead LQFP and the 48-pad QFN package. A detailed mechanical description is given in the section Mechanical Characteristics of the full datasheet.

Figure 4-3. 48-lead LQFP Package (Top View)

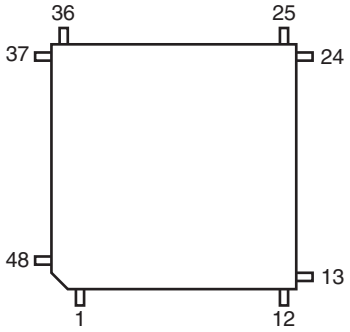
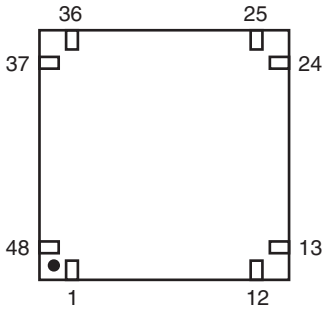


Figure 4-4. 48-pad QFN Package (Top View)



4.4 48-lead LQFP and 48-pad QFN Pinout

Table 4-2. SAM7S32/16 Pinout[1]

1	ADVREF	13	VDDIO	25	TDI	37	TDO
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	AD4	15	PA15/PGMD3	27	PA5/PGMRDY	39	TMS
4	AD5	16	PA14/PGMD2	28	PA4/PGMNCMD	40	TCK
5	AD6	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	AD7	18	VDDCORE	30	TST	42	ERASE
7	VDDIN	19	PA12/PGMD0	31	PA3	43	VDDFLASH
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	GND
9	PA17/PGMD5/AD0	21	PA10/PGMM2	33	VDDIO	45	XOUT
10	PA18/PGMD6/AD1	22	PA9/PGMM1	34	GND	46	XIN/PGMCK
11	PA19/PGMD7/AD2	23	PA8/PGMM0	35	PA1/PGMEN1	47	PLLRC
12	PA20/AD3	24	PA7/PGMNVALID	36	PA0/PGMEN0	48	VDDPLL

Note: 1. The bottom pad of the QFN package must be connected to ground.

Figure 5-1. 3.3V System Single Power Supply Schematic

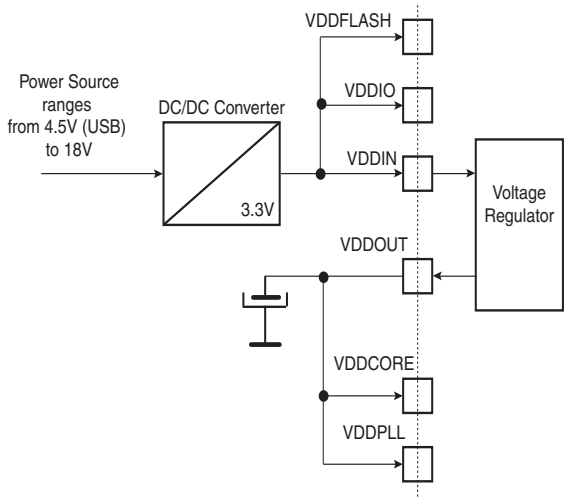
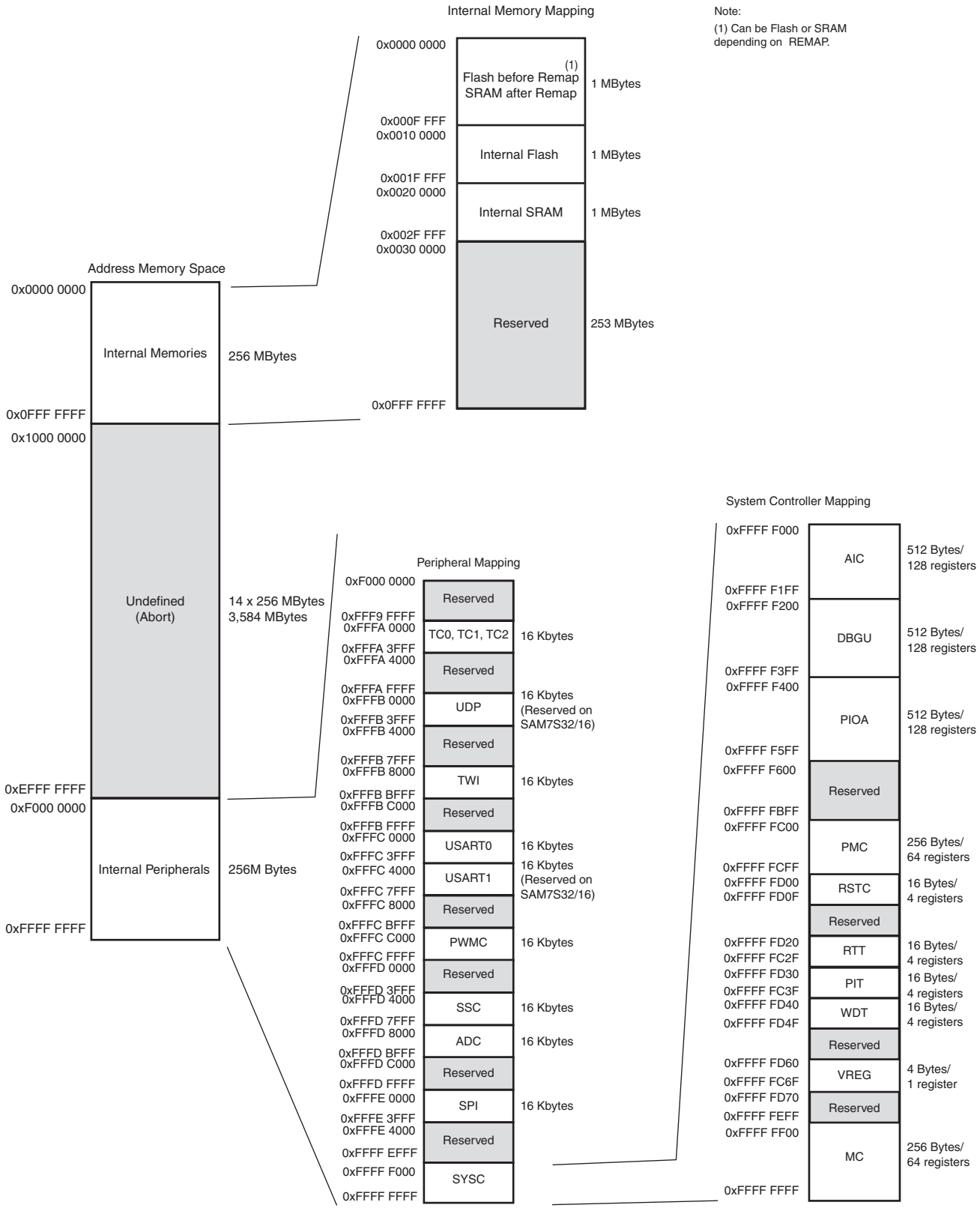


Figure 8-1. SAM SAM7S512/256/128/64/321/32/161/16 Memory Mapping



The 8 NVM bits are software programmable through the EFC User Interface. The command “Set Lock Bit” enables the protection. The command “Clear Lock Bit” unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.6 SAM7S161/16

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S161/16 contains 8 lock regions and each lock region contains 32 pages of 64 bytes. Each lock region has a size of 2 Kbytes.

If a locked-region’s erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 8 NVM bits are software programmable through the EFC User Interface. The command “Set Lock Bit” enables the protection. The command “Clear Lock Bit” unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

Table 8-1 summarizes the configuration of the eight devices.

Table 8-1. Flash Configuration Summary

SAM7S512	32	64	256 bytes
SAM7S256	16	64	256 bytes
SAM7S128	8	64	256 bytes
SAM7S64	16	32	128 bytes
SAM7S321/32	8	32	128 bytes
SAM7S161/16	8	32	64 bytes

8.8.4 Security Bit Feature

The SAM7S Series features a security bit, based on a specific NVM Bit. When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the Command “Set Security Bit” of the EFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full flash erase is performed. When the security bit is deactivated, all accesses to the flash are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 50 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

8.8.5 Non-volatile Brownout Detector Control

Two general purpose NVM (GPNVM) bits are used for controlling the brownout detector (BOD), so that even after a power loss, the brownout detector operations remain in their state.

These two GPNVM bits can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EFC User Interface.

- GPNVM Bit 0 is used as a brownout detector enable bit. Setting the GPNVM Bit 0 enables the BOD, clearing it disables the BOD. Asserting ERASE clears the GPNVM Bit 0 and thus disables the brownout detector by default.
- The GPNVM Bit 1 is used as a brownout reset enable signal for the reset controller. Setting the GPNVM Bit 1 enables the brownout reset when a brownout is detected, Clearing the GPNVM Bit 1 disables the brownout reset. Asserting ERASE disables the brownout reset by default.

9.9 PIO Controller

- One PIO Controller, controlling 32 I/O lines (21 for SAM7S32/16)
- Fully programmable through set/clear registers
- Multiplexing of two peripheral functions per I/O line
- For each I/O line (whether assigned to a peripheral or used as general-purpose I/O)
  - Input change interrupt
  - Half a clock period glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull-up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

9.10 Voltage Regulator Controller

The aim of this controller is to select the Power Mode of the Voltage Regulator between Normal Mode (bit 0 is cleared) or Standby Mode (bit 0 is set).

Table 10-2. Peripheral Identifiers (SAM7S32/16)

0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC[1]	System	
2	PIOA	Parallel I/O Controller A	
3	Reserved		
4	ADC[1]	Analog-to Digital Converter	
5	SPI	Serial Peripheral Interface	
6	US	USART	
7	Reserved		
8	SSC	Synchronous Serial Controller	
9	TWI	Two-wire Interface	
10	PWMC	PWM Controller	
11	Reserved		
12	TC0	Timer/Counter 0	
13	TC1	Timer/Counter 1	
14	TC2	Timer/Counter 2	
15 - 29	Reserved		
30	AIC	Advanced Interrupt Controller	IRQ0
31	Reserved		

10.3 Peripheral Multiplexing on PIO Lines

The SAM7S Series features one PIO controller, PIOA, that multiplexes the I/O lines of the peripheral set.

PIO Controller A controls 32 lines (21 lines for SAM7S32/16). Each line can be assigned to one of two peripheral functions, A or B. Some of them can also be multiplexed with the analog inputs of the ADC Controller.

Table 10-3, “Multiplexing on PIO Controller A (SAM7S512/256/128/64/321/161),” on page 35 and Table 10-4, “Multiplexing on PIO Controller A (SAM7S32/16),” on page 36 define how the I/O lines of the peripherals A, B or the analog inputs are multiplexed on the PIO Controller A. The two columns “Function” and “Comments” have been inserted for the user’s own comments; they may be used to track how pins are defined in an application.

Note that some peripheral functions that are output only may be duplicated in the table.

All pins reset in their Parallel I/O lines function are configured as input with the programmable pull-up enabled, so that the device is maintained in a static state as soon as a reset is detected.

10.4 PIO Controller A Multiplexing

Table 10-3. Multiplexing on PIO Controller A (SAM7S512/256/128/64/321/161)

PA0	PWM0	TIOA0	High-Drive		
PA1	PWM1	TIOB0	High-Drive		
PA2	PWM2	SCK0	High-Drive		
PA3	TWD	NPCS3	High-Drive		
PA4	TWCK	TCLK0			
PA5	RXD0	NPCS3			
PA6	TXD0	PCK0			
PA7	RTS0	PWM3			
PA8	CTS0	ADTRG			
PA9	DRXD	NPCS1			
PA10	DTXD	NPCS2			
PA11	NPCS0	PWM0			
PA12	MISO	PWM1			
PA13	MOSI	PWM2			
PA14	SPCK	PWM3			
PA15	TF	TIOA1			
PA16	TK	TIOB1			
PA17	TD	PCK1	AD0		
PA18	RD	PCK2	AD1		
PA19	RK	FIQ	AD2		
PA20	RF	IRQ0	AD3		
PA21	RXD1	PCK1			
PA22	TXD1	NPCS3			
PA23	SCK1	PWM0			
PA24	RTS1	PWM1			
PA25	CTS1	PWM2			
PA26	DCD1	TIOA2			
PA27	DTR1	TIOB2			
PA28	DSR1	TCLK1			
PA29	RI1	TCLK2			
PA30	IRQ1	NPCS2			
PA31	NPCS1	PCK2			

Table 10-4. Multiplexing on PIO Controller A (SAM7S32/16)

PA0	PWM0	TIOA0	High-Drive		
PA1	PWM1	TIOB0	High-Drive		
PA2	PWM2	SCK0	High-Drive		
PA3	TWD	NPCS3	High-Drive		
PA4	TWCK	TCLK0			
PA5	RXD0	NPCS3			
PA6	TXD0	PCK0			
PA7	RTS0	PWM3			
PA8	CTS0	ADTRG			
PA9	DRXD	NPCS1			
PA10	DTXD	NPCS2			
PA11	NPCS0	PWM0			
PA12	MISO	PWM1			
PA13	MOSI	PWM2			
PA14	SPCK	PWM3			
PA15	TF	TIOA1			
PA16	TK	TIOB1			
PA17	TD	PCK1	AD0		
PA18	RD	PCK2	AD1		
PA19	RK	FIQ	AD2		
PA20	RF	IRQ0	AD3		

10.8 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.9 Timer Counter

- Three 16-bit Timer Counter Channels
  - Two output compare or one input capture per channel (except for SAM7S32/16 which have only two channels connected to the PIO)
- Wide range of functions including:
  - Frequency measurement
  - Event counting
  - Interval measurement
  - Pulse generation
  - Delay timing
  - Pulse Width Modulation
  - Up/down capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs (The SAM7S32/16 have one)
  - Five internal clock inputs, as defined in Table 10-5

Table 10-5. Timer Counter Clocks Assignment

TIMER_CLOCK1	MCK/2
TIMER_CLOCK2	MCK/8
TIMER_CLOCK3	MCK/32
TIMER_CLOCK4	MCK/128
TIMER_CLOCK5	MCK/1024

  - Two multi-purpose input/output signals
  - Two global registers that act on all three TC channels

10.10 PWM Controller

- Four channels, one 16-bit counter per channel
- Common clock generator, providing thirteen different clocks
  - One Modulo n counter providing eleven clocks
  - Two independent linear dividers working on modulo n counter outputs
- Independent channel programming
  - Independent enable/disable commands
  - Independent clock selection
  - Independent period and duty cycle, with double buffering
  - Programmable selection of the output waveform polarity

11. Package Drawings

The SAM7S series devices are available in LQFP and QFN package types.

11.1 LQFP Packages

Figure 11-1. 48-and 64-lead LQFP Package Drawing

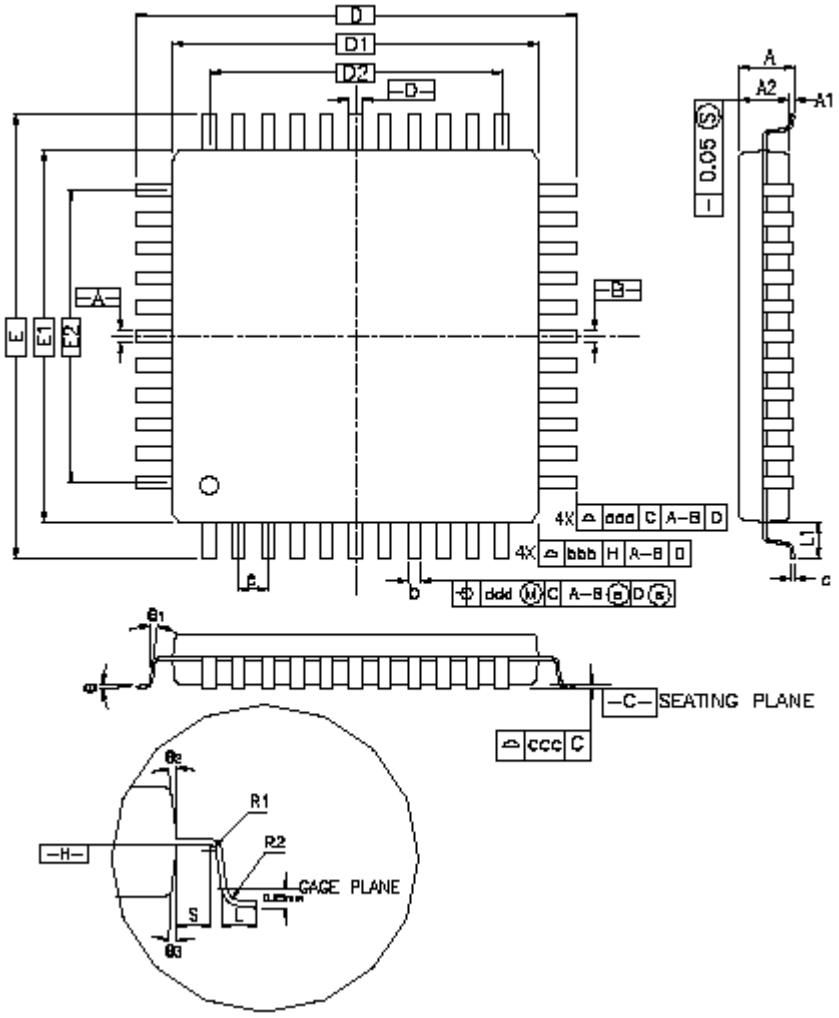


Table 11-1. 48-lead LQFP Package Dimensions (in mm)

Symbol						
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
R2	0.08	–	0.20	0.003	–	0.008
R1	0.08	–	–	0.003	–	–
q	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	–	–	0°	–	–
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	5.50			0.217		
E2	5.50			0.217		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

12. SAM7S Ordering Information

Table 12-1. SAM7S Series Ordering Information

MLR A Ordering Code	MLR B Ordering Code	MLR C Ordering Code	MLR D Ordering Code	Package	Package Type	Temperature Operating Range
AT91SAM7S16-AU AT91SAM7S16-MU	–	–	–	LQFP 48 QFN 48	Green	Industrial (-40· C to 85· C)
AT91SAM7S161-AU	–	–	–	LQFP 64	Green	Industrial (-40· C to 85· C)
AT91SAM7S32-AU-001 AT91SAM7S32-MU	AT91SAM7S32B-AU AT91SAM7S32B-MU			LQFP 48 QFN 48	Green	Industrial (-40· C to 85· C)
AT91SAM7S321-AU AT91SAM7S321-MU	–	–	–	LQFP 64 QFN 64	Green	Industrial (-40· C to 85· C)
–	AT91SAM7S64B-AU AT91SAM7S64B-MU	AT91SAM7S64C-AU AT91SAM7S64C-MU	–	LQFP 64 QFN 64	Green	Industrial (-40· C to 85· C)
–	AT91SAM7S128-AU-001 AT91SAM7S128-MU	AT91SAM7S128C-AU AT91SAM7S128C-MU	AT91SAM7S128D-AU AT91SAM7S128D-MU	LQFP 64 QFN 64	Green	Industrial (-40· C to 85· C)
–	AT91SAM7S256-AU-001 AT91SAM7S256-MU	AT91SAM7S256C-AU AT91SAM7S256C-MU	AT91SAM7S256D-AU AT91SAM7S256D-MU	LQFP 64 QFN 64	Green	Industrial (-40· C to 85· C)
AT91SAM7S512-AU AT91SAM7S512-MU	AT91SAM7S512B-AU AT91SAM7S512B-MU	–	–	LQFP 64 QFN 64	Green	Industrial (-40· C to 85· C)

Revision History

6175AS	First issue - Unqualified on Intranet Corresponds to 6175A full datasheet approval loop. Qualified on Intranet.	
6175BS	Section 8. “Memories” on page 18 updated: 2 ms => 3 ms, 10 ms => 15 ms, 4 ms => 6 ms	CSR05-529
6175CS	Section 12. ”SAM7S Ordering Information” AT91SAM7S321 changed in Table 12-1 on page 47	#2342
6175DS	“Features” , Table 1-1, “Configuration Summary,” on page 3, Section 4. ”Package and Pinout” Section 12. ”SAM7S Ordering Information” QFN package information added	#2444
6175ES	Section 10.11 on page 39 USB Device port, Ping-pong Mode includes Isochronous endpoints. “Features” on page 1, and global: AT91SAM7S512 added to series. Reference to Manchester Encoder removed from USART. Section 8. ”Memories” Reformatted Memories, Consolidated Memory Mapping in Figure 8-1 on page 20 Section 10. ”Peripherals” Reordered sub sections. Section 11. ”Package Drawings” QFN, LQFP package drawings added. “ice_nreset” signals changed to” power_on_reset” in System Controller block diagrams, Figure 9-1 on page 26 and Figure 9-2 on page 27. Section 4. ”Package and Pinout” LQFP and QFN Package Outlines replace Mechanical Overview. Section 10.1 ”User Interface”, User peripherals are mapped between 0xF000 0000 and 0xFFFF EFFF. SYSIRQ changed to SYSC in “Peripheral Identifiers” Table 10-1 and Table 10-2	specs #2748 #2832 (DBGU IP) rfo review
6175FS	AT91SAM7S161 and AT91SAM7S16 added to product family **Features:** Timer Counter, on page 2 product specific information rewritten, Table 1-1, “Configuration Summary,” on page 3, footnote explains TC on AT91SAM7S32/16 has only two channels accessible via PIO, and in Section 10.9 ”Timer Counter”, precisions added to “compare and capture” output/input. Section 10.6 ”Two-wire Interface”, updated reference to I^2C compatibility, internal address registers, slave addressing, Modes for AT91SAM7S161/16 “One Two-wire Interface (TWI)” on page 2, updated in Features Section 10.12 ”Analog-to-digital Converter”, updated Successive Approximation Register ADC and the INL, DNL ± values of LSB. Section 8.8.3 ”Lock Regions”, locked-region’s erase or program command updated Section 9.5 ”Debug Unit”, Chip ID updated. Section 6. ”I/O Lines Considerations”, JTAG Port Pin, Test Pin, Erase Pin, updated.	BDs 4208 rfo review 4325 5063

6175GS	“Features” ,“Debug Unit (DBGU)” updated with “Mode for General Purpose 2-wire UART Serial Communication” Section 7.4 ”Peripheral DMA Controller”, added list of PDC priorities. Section 9. ”System Controller”, Figure 9-1 and Figure 9-2 RTT is reset by “power_on_reset”. Section 9.1.1 ”Brownout Detector and Power-on Reset”, fourth paragraph reduced. Section 9.5 ”Debug Unit”, the list; Section I ”Chip ID Registers”, chip IDs updated, added SAM7S32 Rev B and SAM7S64 Rev B to the list. Section 12. ”SAM7S Ordering Information”, Updated product ordering information by MRL A and MRL B versions.	5846 5913 5224 5685 rfo
6175HS	Section 6.2 ”Test Pin”, added to SAM-BA Boot recovery procedure, a power cycle of the board is mandatory. Section 8.10 ”SAM-BA Boot Assistant”, added to SAM-BA Boot recovery procedure, a power cycle of the board is mandatory.	6068
6175IS	Section 9.5 ”Debug Unit”, Chip ID Registers list updated. MRL C column added to Table 12-1, “SAM7S Series Ordering Information”.	7185
6175JS	Product Series Naming Convention Except for part ordering and library references, AT91 prefix dropped from most nomenclature. AT91SAM7S becomes SAM7S. Debug Unit: “Chip ID Registers” on page 31, Chip ID is 0x270B0A4F for AT91SAM7S512 Rev B	rfo 7945
6175KS	Section 9.5 ”Debug Unit”, Chip ID Registers list updated. Added Chip ID for SAM7S128 Rev D and SAM7S256 Rev D Table 12-1, “SAM7S Series Ordering Information”.Added SAM7S128 Rev D and SAM7S256 Rev D	8380/8467