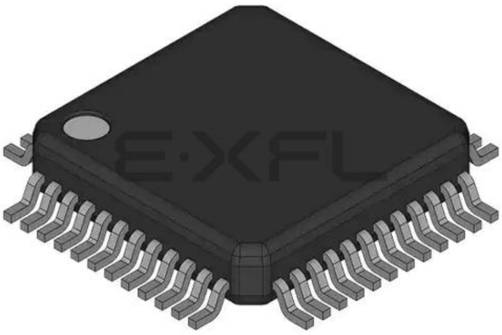

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	I²C, SPI, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at91sam7s16-au

- **Fully Static Operation: Up to 55 MHz at 1.65V and 85· C Worst Case Conditions**
- **Available in 64-lead LQFP Green or 64-pad QFN Green Package (SAM7S512/256/128/64/321/161) and 48-lead LQFP Green or 48-pad QFN Green Package (SAM7S32/16)**

1. Description

Atmel's SAM7S is a series of low pincount Flash microcontrollers based on the 32-bit ARM RISC processor. It features a high-speed Flash and an SRAM, a large set of peripherals, including a USB 2.0 device (except for the SAM7S32 and SAM7S16), and a complete set of system functions minimizing the number of external components. The device is an ideal migration path for 8-bit microcontroller users looking for additional performance and extended memory.

The embedded Flash memory can be programmed in-system via the JTAG-ICE interface or via a parallel interface on a production programmer prior to mounting. Built-in lock bits and a security bit protect the firmware from accidental overwrite and preserves its confidentiality.

The SAM7S Series system controller includes a reset controller capable of managing the power-on sequence of the microcontroller and the complete system. Correct device operation can be monitored by a built-in brownout detector and a watchdog running off an integrated RC oscillator.

The SAM7S Series are general-purpose microcontrollers. Their integrated USB Device port makes them ideal devices for peripheral applications requiring connectivity to a PC or cellular phone. Their aggressive price point and high level of integration pushes their scope of use far into the cost-sensitive, high-volume consumer market.

1.1 Configuration Summary of the SAM7S512, SAM7S256, SAM7S128, SAM7S64, SAM7S321, SAM7S32, SAM7S161 and SAM7S16

The SAM7S512, SAM7S256, SAM7S128, SAM7S64, SAM7S321, SAM7S32, SAM7S161 and SAM7S16 differ in memory size, peripheral set and package. Table 1-1 summarizes the configuration of the six devices.

Except for the SAM7S32/16, all other SAM7S devices are package and pinout compatible.

Table 1-1. Configuration Summary

SAM7S512	512 Kbytes	Master	dual plane	64 Kbytes	1	2(1) (2)	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S256	256 Kbytes	Master	single plane	64 Kbytes	1	2(1) (2)	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S128	128 Kbytes	Master	single plane	32 Kbytes	1	2(1) (2)	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S64	64 Kbytes	Master	single plane	16 Kbytes	1	2(2)	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S321	32 Kbytes	Master	single plane	8 Kbytes	1	2(2)	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S32	32 Kbytes	Master	single plane	8 Kbytes	not present	1	1	9	3(3)	Yes	21	LQFP/ QFN 48
SAM7S161	16 Kbytes	Master/ Slave	single plane	4 Kbytes	1	2(2)	2	11	3	No	32	LQFP
SAM7S16	16 Kbytes	Master/ Slave	single plane	4 Kbytes	not present	1	1	9	3(3)	No	21	LQFP/ QFN 48

Notes: 1. Fractional Baud Rate.

2. Full modem line support on USART1.

3. Only two TC channels are accessible through the PIO.

3. Signal Description

Table 3-1. Signal Description List

VDDIN	Voltage and ADC Regulator Power Supply Input	Power		3.0 to 3.6V
VDDOUT	Voltage Regulator Output	Power		1.85V nominal
VDDFLASH	Flash Power Supply	Power		3.0V to 3.6V
VDDIO	I/O Lines Power Supply	Power		3.0V to 3.6V or 1.65V to 1.95V
VDDCORE	Core Power Supply	Power		1.65V to 1.95V
VDDPLL	PLL	Power		1.65V to 1.95V
GND	Ground	Ground		
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
PLLRC	PLL Filter	Input		
PCK0 - PCK2	Programmable Clock Output	Output		
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor
JTAGSEL	JTAG Selection	Input		Pull-down resistor(1)
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	Pull-down resistor(1)
NRST	Microcontroller Reset	I/O	Low	Open-drain with pull-Up resistor
TST	Test Mode Select	Input	High	Pull-down resistor(1)
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
IRQ0 - IRQ1	External Interrupt Inputs	Input		IRQ1 not present on SAM7S32/16
FIQ	Fast Interrupt Input	Input		
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset PA0 - PA20 only on SAM7S32/16

Table 3-1. Signal Description List (Continued)

TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		
AD0-AD3	Analog Inputs	Analog		Digital pulled-up inputs at reset
AD4-AD7	Analog Inputs	Analog		Analog Inputs
ADTRG	ADC Trigger	Input		
ADVREF	ADC Reference	Analog		
PGMEN0-PGMEN2	Programming Enabling	Input		
PGMM0-PGMM3	Programming Mode	Input		
PGMD0-PGMD15	Programming Data	I/O		PGMD0-PGMD7 only on SAM7S32/16
PGMRDY	Programming Ready	Output	High	
PGMNVALID	Data Direction	Output	Low	
PGMNOE	Programming Read	Input	Low	
PGMCK	Programming Clock	Input		
PGMNCMD	Programming Command	Input	Low	

Note: 1. Refer to Section 6. "I/O Lines Considerations" on page 14.

5. Power Considerations

5.1 Power Supplies

The SAM7S Series has six types of power supply pins and integrates a voltage regulator, allowing the device to be supplied with only one voltage. The six power supply pin types are:

- VDDIN pin. It powers the voltage regulator and the ADC; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDOUT pin. It is the output of the 1.8V voltage regulator.
- VDDIO pin. It powers the I/O lines and the USB transceivers; dual voltage range is supported. Ranges from 3.0V to 3.6V, 3.3V nominal or from 1.65V to 1.95V, 1.8V nominal. Note that supplying less than 3.0V to VDDIO prevents any use of the USB transceivers.
- VDDFLASH pin. It powers a part of the Flash and is required for the Flash to operate correctly; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDCORE pins. They power the logic of the device; voltage ranges from 1.65V to 1.95V, 1.8V typical. It can be connected to the VDDOUT pin with decoupling capacitor. VDDCORE is required for the device, including its embedded Flash, to operate correctly.

During startup, core supply voltage (VDDCORE) slope must be superior or equal to 6V/ms.

- VDDPLL pin. It powers the oscillator and the PLL. It can be connected directly to the VDDOUT pin.

No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

In order to decrease current consumption, if the voltage regulator and the ADC are not used, VDDIN, ADVREF, AD4, AD5, AD6 and AD7 should be connected to GND. In this case VDDOUT should be left unconnected.

5.2 Power Consumption

The SAM7S Series has a static current of less than 60 µA on VDDCORE at 25°C, including the RC oscillator, the voltage regulator and the power-on reset. When the brown-out detector is activated, 20 µA static current is added.

The dynamic power consumption on VDDCORE is less than 50 mA at full speed when running out of the Flash. Under the same conditions, the power consumption on VDDFLASH does not exceed 10 mA.

5.3 Voltage Regulator

The SAM7S Series embeds a voltage regulator that is managed by the System Controller.

In Normal Mode, the voltage regulator consumes less than 100 µA static current and draws 100 mA of output current.

The voltage regulator also has a Low-power Mode. In this mode, it consumes less than 25 µA static current and draws 1 mA of output current.

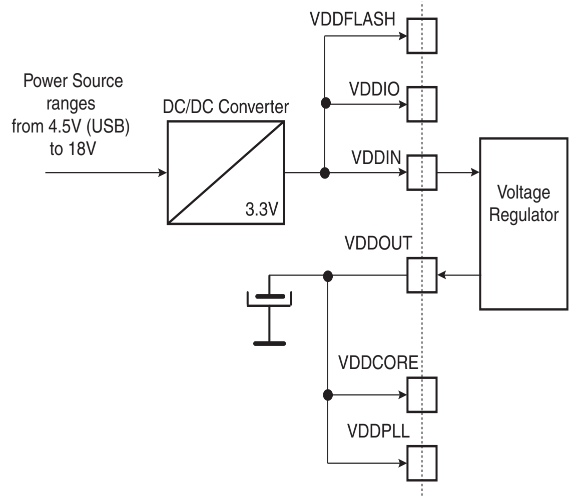
Adequate output supply decoupling is mandatory for VDDOUT to reduce ripple and avoid oscillations. The best way to achieve this is to use two capacitors in parallel: one external 470 pF (or 1 nF) NPO capacitor must be connected between VDDOUT and GND as close to the chip as possible. One external 2.2 µF (or 3.3 µF) X7R capacitor must be connected between VDDOUT and GND.

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop. The input decoupling capacitor should be placed close to the chip. For example, two capacitors can be used in parallel: 100 nF NPO and 4.7 µF X7R.

5.4 Typical Powering Schematics

The SAM7S Series supports a 3.3V single supply mode. The internal regulator is connected to the 3.3V source and its output feeds VDDCORE and the VDDPLL. Figure 5-1 shows the power schematics to be used for USB bus-powered systems.

Figure 5-1. 3.3V System Single Power Supply Schematic



7. Processor and Architecture

7.1 ARM7TDMI Processor

- RISC processor based on ARMv4T Von Neumann architecture
  - Runs at up to 55 MHz, providing 0.9 MIPS/MHz
- Two instruction sets
  - ARM® high-performance 32-bit instruction set
  - Thumb® high code density 16-bit instruction set
- Three-stage pipeline architecture
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)

7.2 Debug and Test Features

- Integrated EmbeddedICE™ (embedded in-circuit emulator)
  - Two watchpoint units
  - Test access port accessible through a JTAG protocol
  - Debug communication channel
- Debug Unit
  - Two-pin UART
  - Debug communication channel interrupt handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on all digital pins

7.3 Memory Controller

- Bus Arbiter
  - Handles requests from the ARM7TDMI and the Peripheral DMA Controller
- Address decoder provides selection signals for
  - Three internal 1 Mbyte memory areas
  - One 256 Mbyte embedded peripheral area
- Abort Status Registers
  - Source, Type and all parameters of the access leading to an abort are saved
  - Facilitates debug by detection of bad pointers
- Misalignment Detector
  - Alignment checking of all data accesses
  - Abort generation in case of misalignment
- Remap Command
  - Remaps the SRAM in place of the embedded non-volatile memory
  - Allows handling of dynamic exception vectors
- Embedded Flash Controller
  - Embedded Flash interface, up to three programmable wait states
  - Prefetch buffer, buffering and anticipating the 16-bit requests, reducing the required wait states
  - Key-protected program, erase and lock/unlock sequencer
  - Single command for erasing, programming and locking operations
  - Interrupt generation in case of forbidden operation

- Fast access time, 30 MHz single-cycle access in Worst Case conditions
- Page programming time: 6 ms, including page auto-erase
- Page programming without auto-erase: 3 ms
- Full chip erase time: 15 ms
- 10,000 write cycles, 10-year data retention capability
- 16 lock bits, protecting 16 sectors of 32 pages
- Protection Mode to secure contents of the Flash

- 16 Kbytes of Fast SRAM
  - Single-cycle access at full speed

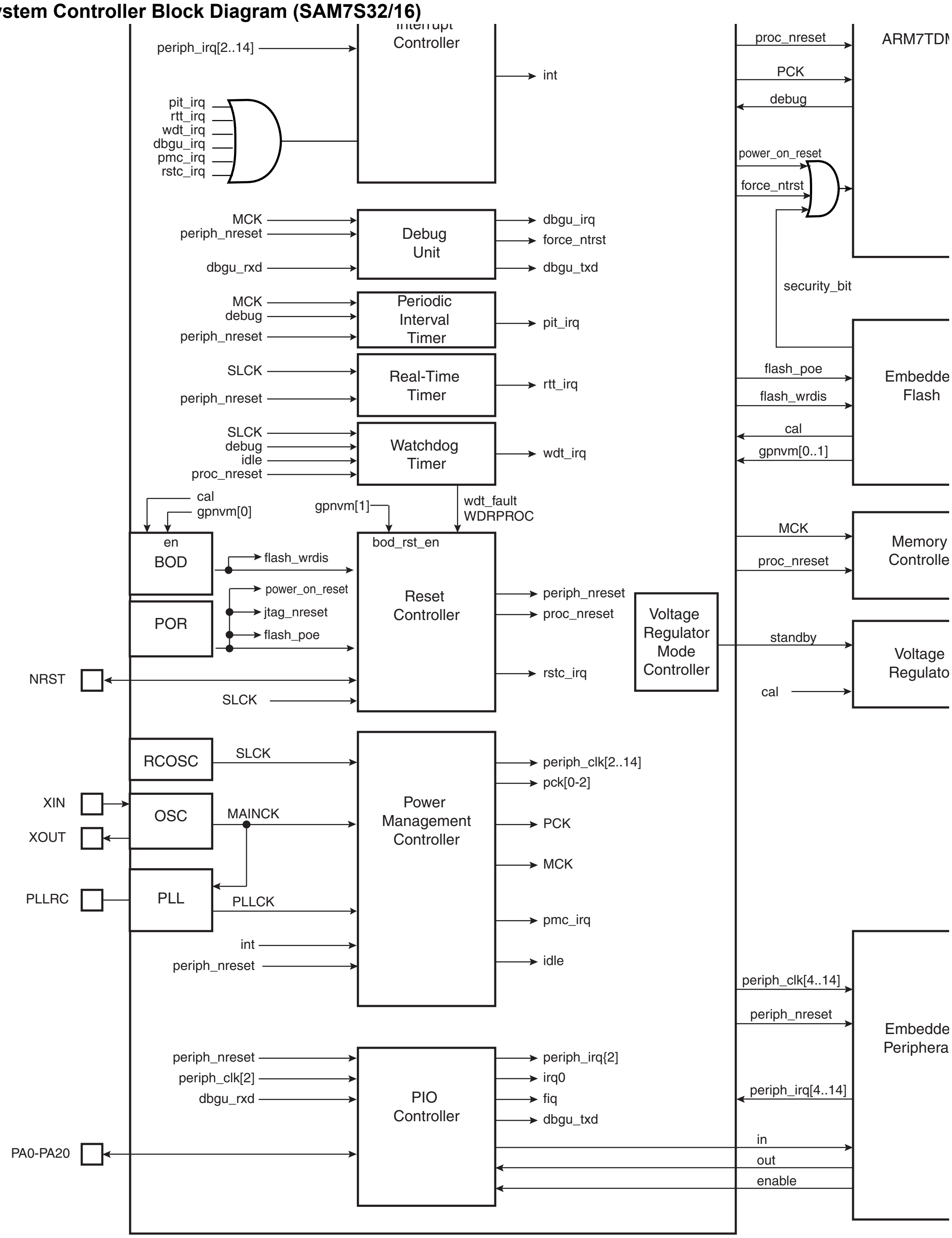
8.5 SAM7S321/32

- 32 Kbytes of Flash Memory, single plane
  - 256 pages of 128 bytes
  - Fast access time, 30 MHz single-cycle access in Worst Case conditions
  - Page programming time: 6 ms, including page auto-erase
  - Page programming without auto-erase: 3 ms
  - Full chip erase time: 15 ms
  - 10,000 write cycles, 10-year data retention capability
  - 8 lock bits, protecting 8 sectors of 32 pages
  - Protection Mode to secure contents of the Flash
- 8 Kbytes of Fast SRAM
  - Single-cycle access at full speed

8.6 SAM7S161/16

- 16 Kbytes of Flash Memory, single plane
  - 256 pages of 64 bytes
  - Fast access time, 30 MHz single-cycle access in Worst Case conditions
  - Page programming time: 6 ms, including page auto-erase
  - Page programming without auto-erase: 3 ms
  - Full chip erase time: 15 ms
  - 10,000 write cycles, 10-year data retention capability
  - 8 lock bits, protecting 8 sectors of 32 pages
  - Protection Mode to secure contents of the Flash
- 4 Kbytes of Fast SRAM
  - Single-cycle access at full speed

Figure 9-2. System Controller Block Diagram (SAM7S32/16)



9.1 Reset Controller

The Reset Controller is based on a power-on reset cell and one brownout detector. It gives the status of the last reset, indicating whether it is a power-up reset, a software reset, a user reset, a watchdog reset or a brownout reset. In addition, it controls the internal resets and the NRST pin open-drain output. It allows to shape a signal on the NRST line, guaranteeing that the length of the pulse meets any requirement.

Note that if NRST is used as a reset output signal for external devices during power-off, the brownout detector must be activated.

9.1.1 Brownout Detector and Power-on Reset

The SAM7S Series embeds a brownout detection circuit and a power-on reset cell. Both are supplied with and monitor VDDCORE. Both signals are provided to the Flash to prevent any code corruption during power-up or power-down sequences or if brownouts occur on the VDDCORE power supply.

The power-on reset cell has a limited-accuracy threshold at around 1.5V. Its output remains low during power-up until VDDCORE goes over this voltage level. This signal goes to the reset controller and allows a full re-initialization of the device.

The brownout detector monitors the VDDCORE level during operation by comparing it to a fixed trigger level. It secures system operations in the most difficult environments and prevents code corruption in case of brownout on the VDDCORE.

Only VDDCORE is monitored.

When the brownout detector is enabled and VDDCORE decreases to a value below the trigger level (Vbot-, defined as Vbot - hyst/2), the brownout output is immediately activated.

When VDDCORE increases above the trigger level (Vbot+, defined as Vbot + hyst/2), the reset is released. The brownout detector only detects a drop if the voltage on VDDCORE stays below the threshold voltage for longer than about 1µs.

The threshold voltage has a hysteresis of about 50 mV, to ensure spike free brownout detection. The typical value of the brownout detector threshold is 1.68V with an accuracy of ± 2% and is factory calibrated.

The brownout detector is low-power, as it consumes less than 20 µA static current. However, it can be deactivated to save its static current. In this case, it consumes less than 1µA. The deactivation is configured through the GPNVM bit 0 of the Flash.

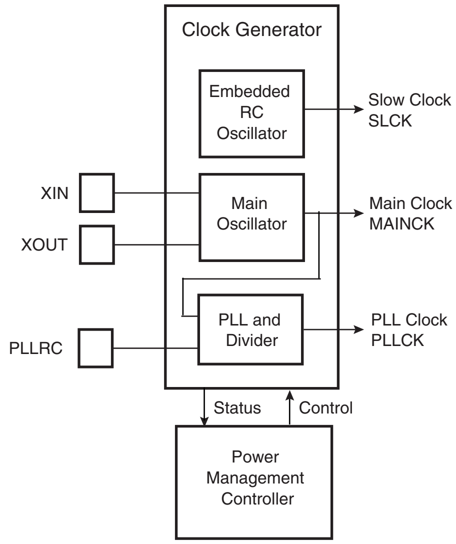
9.2 Clock Generator

The Clock Generator embeds one low-power RC Oscillator, one Main Oscillator and one PLL with the following characteristics:

- RC Oscillator ranges between 22 kHz and 42 kHz
- Main Oscillator frequency ranges between 3 and 20 MHz
- Main Oscillator can be bypassed
- PLL output ranges between 80 and 220 MHz

It provides SLCK, MAINCK and PLLCK.

Figure 9-3. Clock Generator Block Diagram



9.3 Power Management Controller

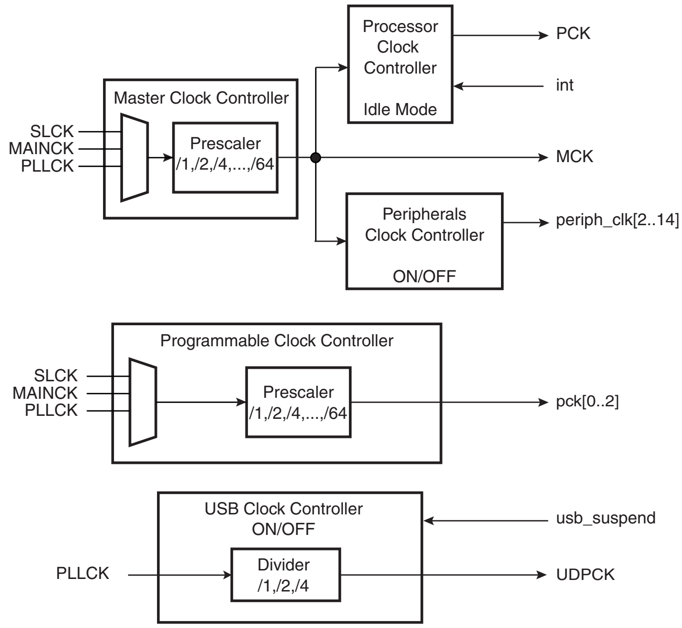
The Power Management Controller uses the Clock Generator outputs to provide:

- the Processor Clock PCK
- the Master Clock MCK
- the USB Clock UDPCK (not present on SAM7S32/16)
- all the peripheral clocks, independently controllable
- three programmable clock outputs

The Master Clock (MCK) is programmable from a few hundred Hz to the maximum operating frequency of the device.

The Processor Clock (PCK) switches off when entering processor idle mode, thus allowing reduced power consumption while waiting for an interrupt.

Figure 9-4. Power Management Controller Block Diagram



9.4 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of an ARM Processor
- Individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals RTT, PIT, EFC, PMC, DBGU, etc.)
  - Other sources control the peripheral interrupts or external interrupts
  - Programmable edge-triggered or level-sensitive internal sources
  - Programmable positive/negative edge-triggered or high/low level-sensitive external sources
- 8-level Priority Controller
  - Drives the normal interrupt of the processor
  - Handles priority of the interrupt sources
  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes interrupt service routine branch and execution
  - One 32-bit vector register per interrupt source
  - Interrupt vector register reads the corresponding current interrupt vector
- Protect Mode
  - Easy debugging by preventing automatic operations
- Fast Forcing
  - Permits redirecting any interrupt source on the fast interrupt
- General Interrupt Mask
  - Provides processor synchronization on events without triggering an interrupt

9.5 Debug Unit

- Comprises:
  - One two-pin UART
  - One Interface for the Debug Communication Channel (DCC) support

9.9 PIO Controller

- One PIO Controller, controlling 32 I/O lines (21 for SAM7S32/16)
- Fully programmable through set/clear registers
- Multiplexing of two peripheral functions per I/O line
- For each I/O line (whether assigned to a peripheral or used as general-purpose I/O)
  - Input change interrupt
  - Half a clock period glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull-up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

9.10 Voltage Regulator Controller

The aim of this controller is to select the Power Mode of the Voltage Regulator between Normal Mode (bit 0 is cleared) or Standby Mode (bit 0 is set).

- Programmable center or left aligned output waveform

10.11 USB Device Port (Does not pertain to SAM7S32/16)

- USB V2.0 full-speed compliant, 12 Mbits per second.
- Embedded USB V2.0 full-speed transceiver
- Embedded 328-byte dual-port RAM for endpoints
- Four endpoints
  - Endpoint 0: 8 bytes
  - Endpoint 1 and 2: 64 bytes ping-pong
  - Endpoint 3: 64 bytes
  - Ping-pong Mode (two memory banks) for isochronous and bulk endpoints
- Suspend/resume logic

10.12 Analog-to-digital Converter

- 8-channel ADC
- 10-bit 384 Ksamples/sec. or 8-bit 583 Ksamples/sec. Successive Approximation Register ADC
- ±2 LSB Integral Non Linearity, ±1 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger source
  - Hardware or software trigger
  - External trigger pin
  - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer
  - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels
- Four of eight analog inputs shared with digital signals

11. Package Drawings

The SAM7S series devices are available in LQFP and QFN package types.

11.1 LQFP Packages

Figure 11-1. 48-and 64-lead LQFP Package Drawing

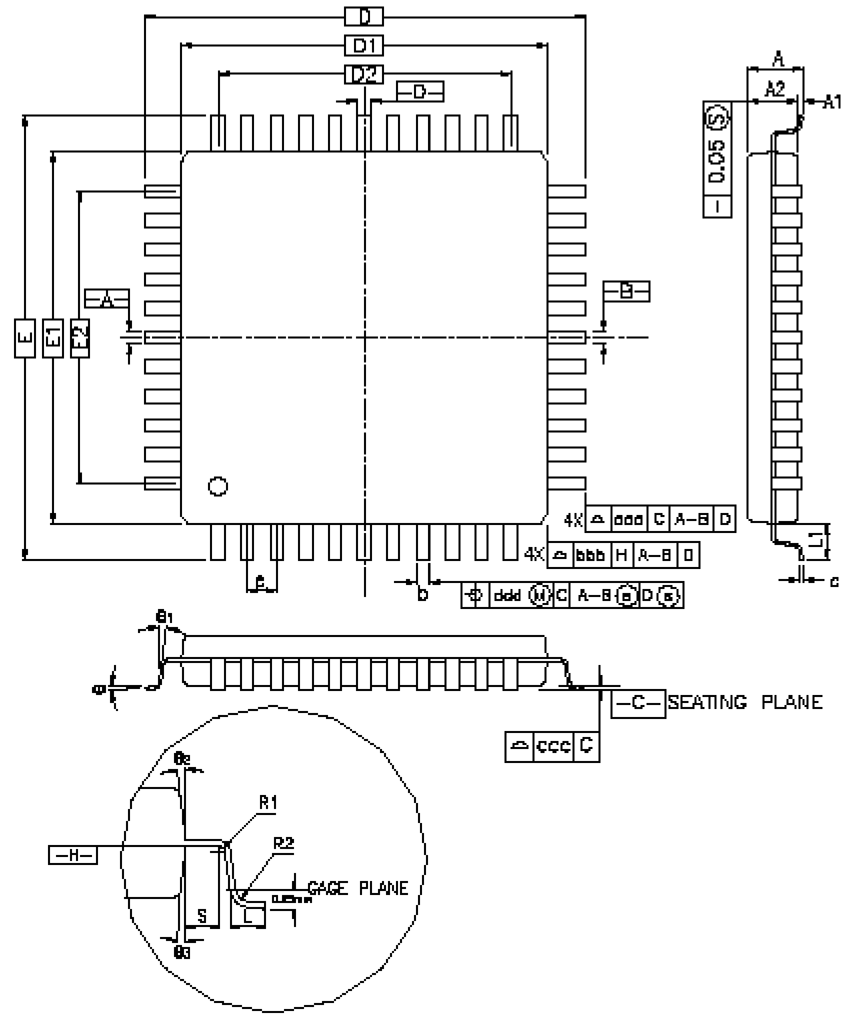


Table 11-3. 48-pad QFN Package Dimensions (in mm)

Symbol						
A	–	–	090	–	–	0.035
A1	–	–	0.050	–	–	0.002
A2	–	0.65	0.70	–	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.18	0.20	0.23	0.007	0.008	0.009
D	7.00 bsc			0.276 bsc		
D2	5.45	5.60	5.75	0.215	0.220	0.226
E	7.00 bsc			0.276 bsc		
E2	5.45	5.60	5.75	0.215	0.220	0.226
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 bsc			0.020 bsc		
R	0.09	–	–	0.004	–	–
Tolerances of Form and Position						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

Table 11-4. 64-pad QFN Package Dimensions (in mm)

Symbol						
A	–	–	090	–	–	0.035
A1	–	–	0.05	–	–	0.001
A2	–	0.65	0.70	–	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.23	0.25	0.28	0.009	0.010	0.011
D	9.00 bsc			0.354 bsc		
D2	6.95	7.10	7.25	0.274	0.280	0.285
E	9.00 bsc			0.354 bsc		
E2	6.95	7.10	7.25	0.274	0.280	0.285
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 bsc			0.020 bsc		
R	0.125	–	–	0.0005	–	–
Tolerances of Form and Position						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

12. SAM7S Ordering Information

Table 12-1. SAM7S Series Ordering Information

MLR A Ordering Code	MLR B Ordering Code	MLR C Ordering Code	MLR D Ordering Code	Package	Package Type	Temperature Operating Range
AT91SAM7S16-AU AT91SAM7S16-MU	–	–	–	LQFP 48 QFN 48	Green	Industrial (-40· C to 85· C)
AT91SAM7S161-AU	–	–	–	LQFP 64	Green	Industrial (-40· C to 85· C)
AT91SAM7S32-AU-001 AT91SAM7S32-MU	AT91SAM7S32B-AU AT91SAM7S32B-MU			LQFP 48 QFN 48	Green	Industrial (-40· C to 85· C)
AT91SAM7S321-AU AT91SAM7S321-MU	–	–	–	LQFP 64 QFN 64	Green	Industrial (-40· C to 85· C)
–	AT91SAM7S64B-AU AT91SAM7S64B-MU	AT91SAM7S64C-AU AT91SAM7S64C-MU	–	LQFP 64 QFN 64	Green	Industrial (-40· C to 85· C)
–	AT91SAM7S128-AU-001 AT91SAM7S128-MU	AT91SAM7S128C-AU AT91SAM7S128C-MU	AT91SAM7S128D-AU AT91SAM7S128D-MU	LQFP 64 QFN 64	Green	Industrial (-40· C to 85· C)
–	AT91SAM7S256-AU-001 AT91SAM7S256-MU	AT91SAM7S256C-AU AT91SAM7S256C-MU	AT91SAM7S256D-AU AT91SAM7S256D-MU	LQFP 64 QFN 64	Green	Industrial (-40· C to 85· C)
AT91SAM7S512-AU AT91SAM7S512-MU	AT91SAM7S512B-AU AT91SAM7S512B-MU	–	–	LQFP 64 QFN 64	Green	Industrial (-40· C to 85· C)

6175GS	“Features” ,“Debug Unit (DBGU)” updated with “Mode for General Purpose 2-wire UART Serial Communication” Section 7.4 ”Peripheral DMA Controller”, added list of PDC priorities. Section 9. ”System Controller”, Figure 9-1 and Figure 9-2 RTT is reset by “power_on_reset”. Section 9.1.1 ”Brownout Detector and Power-on Reset”, fourth paragraph reduced. Section 9.5 ”Debug Unit”, the list; Section I ”Chip ID Registers”, chip IDs updated, added SAM7S32 Rev B and SAM7S64 Rev B to the list. Section 12. ”SAM7S Ordering Information”, Updated product ordering information by MRL A and MRL B versions.	5846 5913 5224 5685 rfo
6175HS	Section 6.2 ”Test Pin”, added to SAM-BA Boot recovery procedure, a power cycle of the board is mandatory. Section 8.10 ”SAM-BA Boot Assistant”, added to SAM-BA Boot recovery procedure, a power cycle of the board is mandatory.	6068
6175IS	Section 9.5 ”Debug Unit”, Chip ID Registers list updated. MRL C column added to Table 12-1, “SAM7S Series Ordering Information”.	7185
6175JS	Product Series Naming Convention Except for part ordering and library references, AT91 prefix dropped from most nomenclature. AT91SAM7S becomes SAM7S. Debug Unit: “Chip ID Registers” on page 31, Chip ID is 0x270B0A4F for AT91SAM7S512 Rev B	rfo 7945
6175KS	Section 9.5 ”Debug Unit”, Chip ID Registers list updated. Added Chip ID for SAM7S128 Rev D and SAM7S256 Rev D Table 12-1, “SAM7S Series Ordering Information”.Added SAM7S128 Rev D and SAM7S256 Rev D	8380/8467

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