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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	I <sup>2</sup> C, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/atmel/at91sam7s161-au">https://www.e-xfl.com/product-detail/atmel/at91sam7s161-au</a>

- **Fully Static Operation: Up to 55 MHz at 1.65V and 85- C Worst Case Conditions**
- **Available in 64-lead LQFP Green or 64-pad QFN Green Package (SAM7S512/256/128/64/321/161) and 48-lead LQFP Green or 48-pad QFN Green Package (SAM7S32/16)**

## 1. Description

Atmel's SAM7S is a series of low pincount Flash microcontrollers based on the 32-bit ARM RISC processor. It features a high-speed Flash and an SRAM, a large set of peripherals, including a USB 2.0 device (except for the SAM7S32 and SAM7S16), and a complete set of system functions minimizing the number of external components. The device is an ideal migration path for 8-bit microcontroller users looking for additional performance and extended memory.

The embedded Flash memory can be programmed in-system via the JTAG-ICE interface or via a parallel interface on a production programmer prior to mounting. Built-in lock bits and a security bit protect the firmware from accidental overwrite and preserves its confidentiality.

The SAM7S Series system controller includes a reset controller capable of managing the power-on sequence of the microcontroller and the complete system. Correct device operation can be monitored by a built-in brownout detector and a watchdog running off an integrated RC oscillator.

The SAM7S Series are general-purpose microcontrollers. Their integrated USB Device port makes them ideal devices for peripheral applications requiring connectivity to a PC or cellular phone. Their aggressive price point and high level of integration pushes their scope of use far into the cost-sensitive, high-volume consumer market.

### 1.1 Configuration Summary of the SAM7S512, SAM7S256, SAM7S128, SAM7S64, SAM7S321, SAM7S32, SAM7S161 and SAM7S16

The SAM7S512, SAM7S256, SAM7S128, SAM7S64, SAM7S321, SAM7S32, SAM7S161 and SAM7S16 differ in memory size, peripheral set and package. [Table 1-1](#) summarizes the configuration of the six devices.

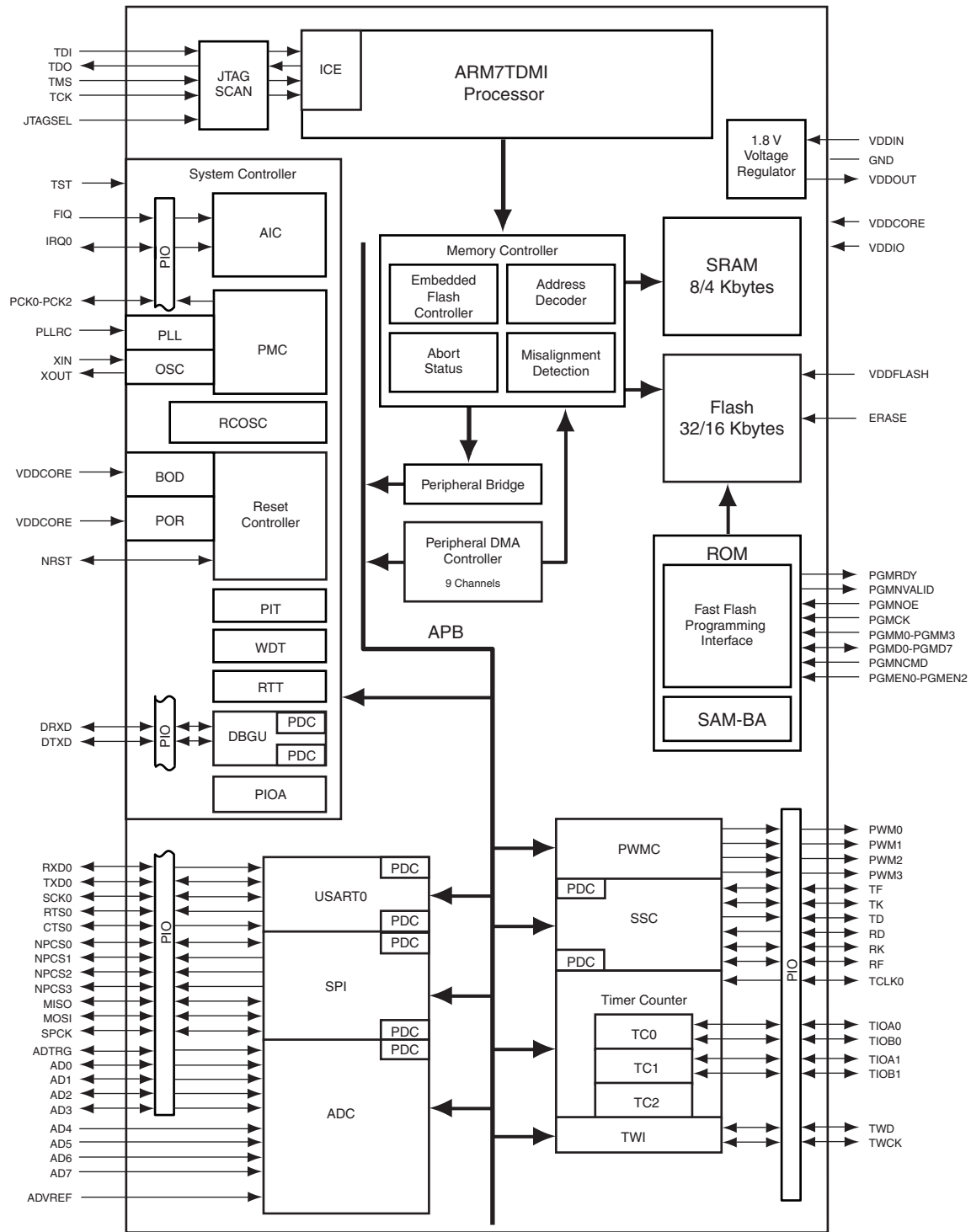
Except for the SAM7S32/16, all other SAM7S devices are package and pinout compatible.

**Table 1-1. Configuration Summary**

Device	Flash	SRAM	Flash Plane	SRAM	TC	UART	USART	IO	IO	IO	IO	IO	IO
SAM7S512	512 Kbytes	Master	dual plane	64 Kbytes	1	2 <sup>(1) (2)</sup>	2	11	3	Yes	32	LQFP/ QFN 64	
SAM7S256	256 Kbytes	Master	single plane	64 Kbytes	1	2 <sup>(1) (2)</sup>	2	11	3	Yes	32	LQFP/ QFN 64	
SAM7S128	128 Kbytes	Master	single plane	32 Kbytes	1	2 <sup>(1) (2)</sup>	2	11	3	Yes	32	LQFP/ QFN 64	
SAM7S64	64 Kbytes	Master	single plane	16 Kbytes	1	2 <sup>(2)</sup>	2	11	3	Yes	32	LQFP/ QFN 64	
SAM7S321	32 Kbytes	Master	single plane	8 Kbytes	1	2 <sup>(2)</sup>	2	11	3	Yes	32	LQFP/ QFN 64	
SAM7S32	32 Kbytes	Master	single plane	8 Kbytes	not present	1	1	9	3 <sup>(3)</sup>	Yes	21	LQFP/ QFN 48	
SAM7S161	16 Kbytes	Master/ Slave	single plane	4 Kbytes	1	2 <sup>(2)</sup>	2	11	3	No	32	LQFP	
SAM7S16	16 Kbytes	Master/ Slave	single plane	4 Kbytes	not present	1	1	9	3 <sup>(3)</sup>	No	21	LQFP/ QFN 48	

- Notes:
1. Fractional Baud Rate.
  2. Full modem line support on USART1.
  3. Only two TC channels are accessible through the PIO.

Figure 2-2. SAM7S32/16 Block Diagram



### 4.3 48-lead LQFP and 48-pad QFN Package Outlines

Figure 4-3 and Figure 4-4 show the orientation of the 48-lead LQFP and the 48-pad QFN package. A detailed mechanical description is given in the section Mechanical Characteristics of the full datasheet.

Figure 4-3. 48-lead LQFP Package (Top View)

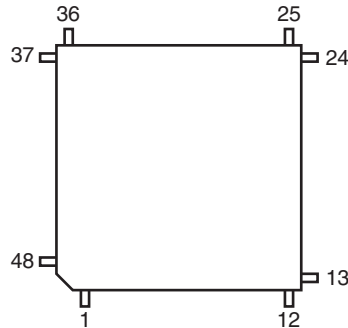
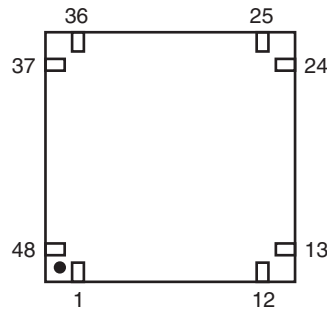


Figure 4-4. 48-pad QFN Package (Top View)



### 4.4 48-lead LQFP and 48-pad QFN Pinout

Table 4-2. SAM7S32/16 Pinout<sup>(1)</sup>

1	ADVREF	13	VDDIO	25	TDI	37	TDO
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	AD4	15	PA15/PGMD3	27	PA5/PGMRDY	39	TMS
4	AD5	16	PA14/PGMD2	28	PA4/PGMNCMD	40	TCK
5	AD6	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	AD7	18	VDDCORE	30	TST	42	ERASE
7	VDDIN	19	PA12/PGMD0	31	PA3	43	VDDFLASH
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	GND
9	PA17/PGMD5/AD0	21	PA10/PGMM2	33	VDDIO	45	XOUT
10	PA18/PGMD6/AD1	22	PA9/PGMM1	34	GND	46	XIN/PGMCK
11	PA19/PGMD7/AD2	23	PA8/PGMM0	35	PA1/PGMEN1	47	PLLRC
12	PA20/AD3	24	PA7/PGMNVALID	36	PA0/PGMEN0	48	VDDPLL

Note: 1. The bottom pad of the QFN package must be connected to ground.

## 5. Power Considerations

### 5.1 Power Supplies

The SAM7S Series has six types of power supply pins and integrates a voltage regulator, allowing the device to be supplied with only one voltage. The six power supply pin types are:

- VDDIN pin. It powers the voltage regulator and the ADC; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDOUT pin. It is the output of the 1.8V voltage regulator.
- VDDIO pin. It powers the I/O lines and the USB transceivers; dual voltage range is supported. Ranges from 3.0V to 3.6V, 3.3V nominal or from 1.65V to 1.95V, 1.8V nominal. Note that supplying less than 3.0V to VDDIO prevents any use of the USB transceivers.
- VDDFLASH pin. It powers a part of the Flash and is required for the Flash to operate correctly; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDCORE pins. They power the logic of the device; voltage ranges from 1.65V to 1.95V, 1.8V typical. It can be connected to the VDDOUT pin with decoupling capacitor. VDDCORE is required for the device, including its embedded Flash, to operate correctly.

During startup, core supply voltage (VDDCORE) slope must be superior or equal to 6V/ms.

- VDDPLL pin. It powers the oscillator and the PLL. It can be connected directly to the VDDOUT pin.

No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

In order to decrease current consumption, if the voltage regulator and the ADC are not used, VDDIN, ADVREF, AD4, AD5, AD6 and AD7 should be connected to GND. In this case VDDOUT should be left unconnected.

### 5.2 Power Consumption

The SAM7S Series has a static current of less than 60  $\mu$ A on VDDCORE at 25°C, including the RC oscillator, the voltage regulator and the power-on reset. When the brown-out detector is activated, 20  $\mu$ A static current is added.

The dynamic power consumption on VDDCORE is less than 50 mA at full speed when running out of the Flash. Under the same conditions, the power consumption on VDDFLASH does not exceed 10 mA.

### 5.3 Voltage Regulator

The SAM7S Series embeds a voltage regulator that is managed by the System Controller.

In Normal Mode, the voltage regulator consumes less than 100  $\mu$ A static current and draws 100 mA of output current.

The voltage regulator also has a Low-power Mode. In this mode, it consumes less than 25  $\mu$ A static current and draws 1 mA of output current.

Adequate output supply decoupling is mandatory for VDDOUT to reduce ripple and avoid oscillations. The best way to achieve this is to use two capacitors in parallel: one external 470 pF (or 1 nF) NPO capacitor must be connected between VDDOUT and GND as close to the chip as possible. One external 2.2  $\mu$ F (or 3.3  $\mu$ F) X7R capacitor must be connected between VDDOUT and GND.

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop. The input decoupling capacitor should be placed close to the chip. For example, two capacitors can be used in parallel: 100 nF NPO and 4.7  $\mu$ F X7R.

### 5.4 Typical Powering Schematics

The SAM7S Series supports a 3.3V single supply mode. The internal regulator is connected to the 3.3V source and its output feeds VDDCORE and the VDDPLL. [Figure 5-1](#) shows the power schematics to be used for USB bus-powered systems.

## 6. I/O Lines Considerations

### 6.1 JTAG Port Pins

TMS, TDI and TCK are schmitt trigger inputs. TMS and TCK are 5-V tolerant, TDI is not. TMS, TDI and TCK do not integrate a pull-up resistor.

TDO is an output, driven at up to VDDIO, and has no pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. The JTAGSEL pin integrates a permanent pull-down resistor of about 15 k $\Omega$  to GND, so that it can be left unconnected for normal operations.

### 6.2 Test Pin

The TST pin is used for manufacturing test, fast programming mode or SAM-BA Boot Recovery of the SAM7S Series when asserted high. The TST pin integrates a permanent pull-down resistor of about 15 k $\Omega$  to GND, so that it can be left unconnected for normal operations.

To enter fast programming mode, the TST pin and the PA0 and PA1 pins should be tied high and PA2 tied to low.

To enter SAM-BA Boot Recovery, the TST pin and the PA0, PA1 and PA2 pins should be tied high for at least 10 seconds. Then a power cycle of the board is mandatory.

Driving the TST pin at a high level while PA0 or PA1 is driven at 0 leads to unpredictable results.

### 6.3 Reset Pin

The NRST pin is bidirectional with an open drain output buffer. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. There is no constraint on the length of the reset pulse, and the reset controller can guarantee a minimum pulse length. This allows connection of a simple push-button on the pin NRST as system user reset, and the use of the signal NRST to reset all the components of the system.

The NRST pin integrates a permanent pull-up resistor to VDDIO.

### 6.4 ERASE Pin

The ERASE pin is used to re-initialize the Flash content and some of its NVM bits. It integrates a permanent pull-down resistor of about 15 k $\Omega$  to GND, so that it can be left unconnected for normal operations.

### 6.5 PIO Controller A Lines

- All the I/O lines PA0 to PA31 on SAM7S512/256/128/64/321 (PA0 to PA20 on SAM7S32) are 5V-tolerant and all integrate a programmable pull-up resistor.
- All the I/O lines PA0 to PA31 on SAM7S161 (PA0 to PA20 on SAM7S16) are **not** 5V-tolerant and all integrate a programmable pull-up resistor.

Programming of this pull-up resistor is performed independently for each I/O line through the PIO controllers.

5V-tolerant means that the I/O lines can drive voltage level according to VDDIO, but can be driven with a voltage of up to 5.5V. However, driving an I/O line with a voltage over VDDIO while the programmable pull-up resistor is enabled will create a current path through the pull-up resistor from the I/O line to VDDIO. Care should be taken, in particular at reset, as all the I/O lines default to input with the pull-up resistor enabled at reset.

### 6.6 I/O Line Drive Levels

The PIO lines PA0 to PA3 are high-drive current capable. Each of these I/O lines can drive up to 16 mA permanently.

The remaining I/O lines can draw only 8 mA.

However, the total current drawn by all the I/O lines cannot exceed 150 mA (100 mA for SAM7S32/16).



## 7.4 Peripheral DMA Controller

- Handles data transfer between peripherals and memories
- Eleven channels: SAM7S512/256/128/64/321/161
- Nine channels: SAM7S32/16
  - Two for each USART
  - Two for the Debug Unit
  - Two for the Serial Synchronous Controller
  - Two for the Serial Peripheral Interface
  - One for the Analog-to-digital Converter
- Low bus arbitration overhead
  - One Master Clock cycle needed for a transfer from memory to peripheral
  - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirements
- Peripheral DMA Controller (PDC) priority is as follows (from the highest priority to the lowest):

Receive	DBGU
Receive	USART0
Receive	USART1
Receive	SSC
Receive	ADC
Receive	SPI
Transmit	DBGU
Transmit	USART0
Transmit	USART1
Transmit	SSC
Transmit	SPI



## 8. Memories

### 8.1 SAM7S512

- 512 Kbytes of Flash Memory, dual plane
  - 2 contiguous banks of 1024 pages of 256 bytes
  - Fast access time, 30 MHz single-cycle access in Worst Case conditions
  - Page programming time: 6 ms, including page auto-erase
  - Page programming without auto-erase: 3 ms
  - Full chip erase time: 15 ms
  - 10,000 write cycles, 10-year data retention capability
  - 32 lock bits, protecting 32 sectors of 64 pages
  - Protection Mode to secure contents of the Flash
- 64 Kbytes of Fast SRAM
  - Single-cycle access at full speed

### 8.2 SAM7S256

- 256 Kbytes of Flash Memory, single plane
  - 1024 pages of 256 bytes
  - Fast access time, 30 MHz single-cycle access in Worst Case conditions
  - Page programming time: 6 ms, including page auto-erase
  - Page programming without auto-erase: 3 ms
  - Full chip erase time: 15 ms
  - 10,000 write cycles, 10-year data retention capability
  - 16 lock bits, protecting 16 sectors of 64 pages
  - Protection Mode to secure contents of the Flash
- 64 Kbytes of Fast SRAM
  - Single-cycle access at full speed

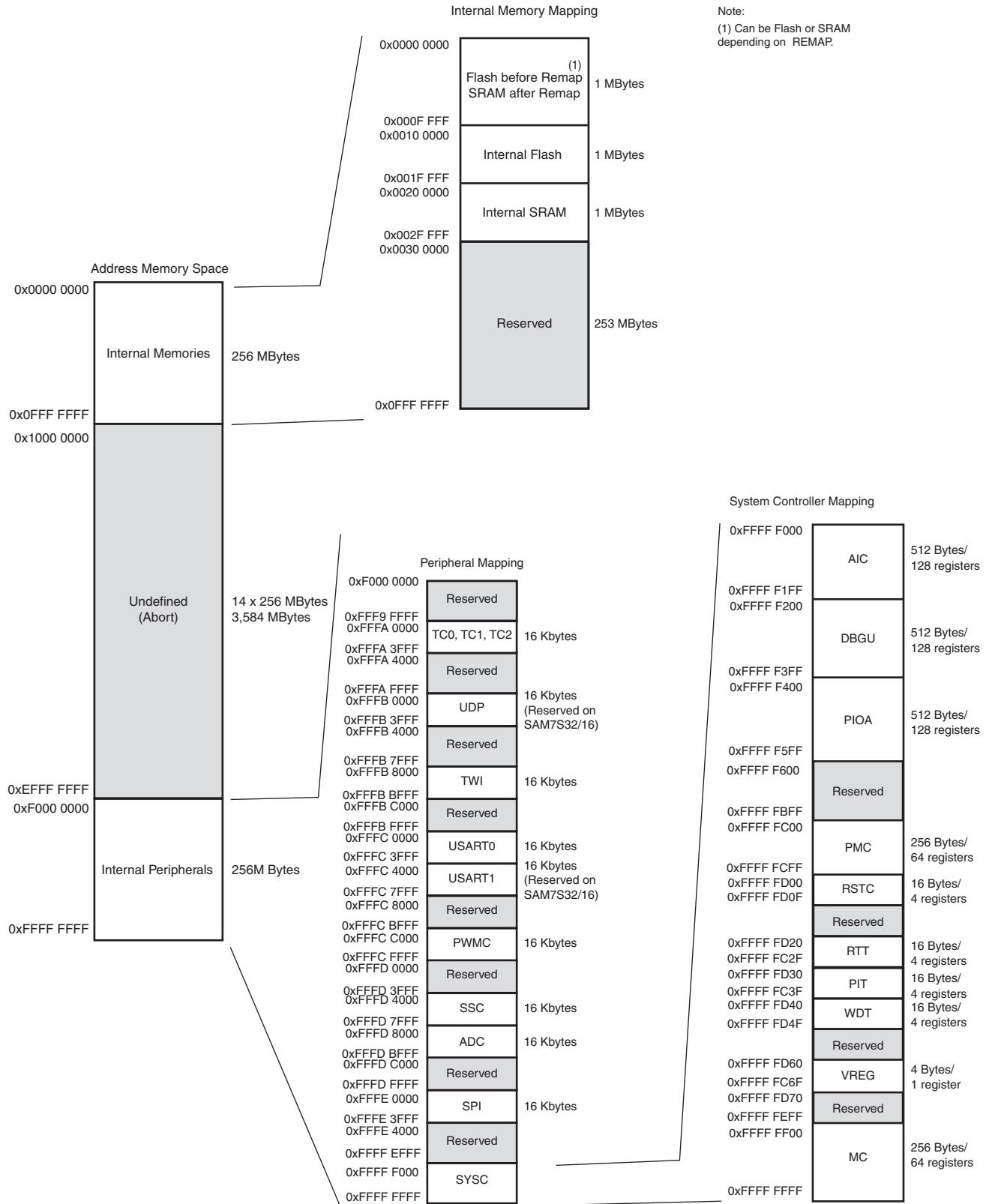
### 8.3 SAM7S128

- 128 Kbytes of Flash Memory, single plane
  - 512 pages of 256 bytes
  - Fast access time, 30 MHz single-cycle access in Worst Case conditions
  - Page programming time: 6 ms, including page auto-erase
  - Page programming without auto-erase: 3 ms
  - Full chip erase time: 15 ms
  - 10,000 write cycles, 10-year data retention capability
  - 8 lock bits, protecting 8 sectors of 64 pages
  - Protection Mode to secure contents of the Flash
- 32 Kbytes of Fast SRAM
  - Single-cycle access at full speed

### 8.4 SAM7S64

- 64 Kbytes of Flash Memory, single plane
  - 512 pages of 128 bytes

**Figure 8-1. SAM SAM7S512/256/128/64/321/32/161/16 Memory Mapping**



Note:  
(1) Can be Flash or SRAM depending on REMAP.

## 8.7 Memory Mapping

### 8.7.1 Internal SRAM

- The SAM7S512 embeds a high-speed 64-Kbyte SRAM bank.
- The SAM7S256 embeds a high-speed 64-Kbyte SRAM bank.
- The SAM7S128 embeds a high-speed 32-Kbyte SRAM bank.
- The SAM7S64 embeds a high-speed 16-Kbyte SRAM bank.
- The SAM7S321 embeds a high-speed 8-Kbyte SRAM bank.
- The SAM7S32 embeds a high-speed 8-Kbyte SRAM bank.
- The SAM7S161 embeds a high-speed 4-Kbyte SRAM bank.
- The SAM7S16 embeds a high-speed 4-Kbyte SRAM bank.

After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x0020 0000. After Remap, the SRAM also becomes available at address 0x0.

### 8.7.2 Internal ROM

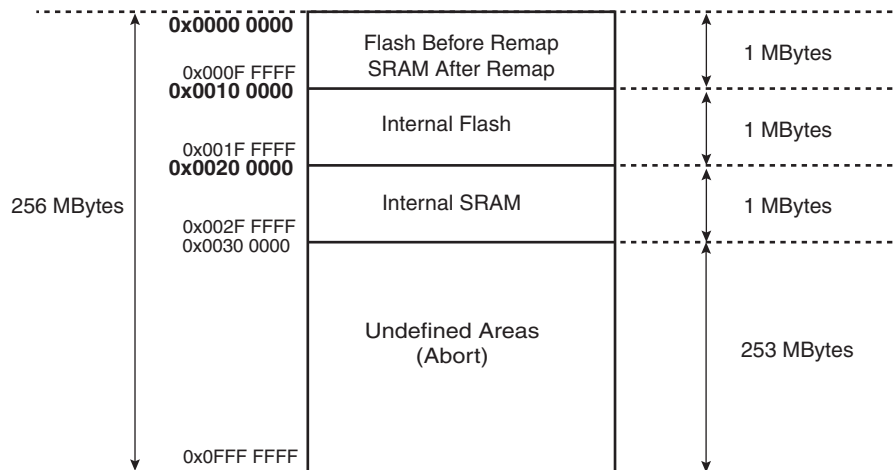
The SAM7S Series embeds an Internal ROM. The ROM contains the FFPI and the SAM-BA program. The internal ROM is not mapped by default.

### 8.7.3 Internal Flash

- The SAM7S512 features two contiguous banks (dual plane) of 256 Kbytes of Flash.
- The SAM7S256 features one bank (single plane) of 256 Kbytes of Flash.
- The SAM7S128 features one bank (single plane) of 128 Kbytes of Flash.
- The SAM7S64 features one bank (single plane) of 64 Kbytes of Flash.
- The SAM7S321/32 features one bank (single plane) of 32 Kbytes of Flash.
- The SAM7S161/16 features one bank (single plane) of 16 Kbytes of Flash.

At any time, the Flash is mapped to address 0x0010 0000. It is also accessible at address 0x0 after the reset and before the Remap Command.

Figure 8-2. Internal Memory Mapping



## 8.8.3 Lock Regions

### 8.8.3.1 SAM7S512

Two Embedded Flash Controllers each manage 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S512 contains 32 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC\_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC\_FMR register.

The 16 NVM bits (or 32 NVM bits) are software programmable through the corresponding EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

### 8.8.3.2 SAM7S256

The Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S256 contains 16 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC\_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC\_FMR register.

The 16 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

### 8.8.3.3 SAM7S128

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S128 contains 8 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC\_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC\_FMR register.

The 8 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

### 8.8.3.4 SAM7S64

The Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S64 contains 16 lock regions and each lock region contains 32 pages of 128 bytes. Each lock region has a size of 4 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC\_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC\_FMR register.

The 16 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

### 8.8.3.5 SAM7S321/32

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S321/32 contains 8 lock regions and each lock region contains 32 pages of 128 bytes. Each lock region has a size of 4 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC\_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC\_FMR register.

The 8 NVM bits are software programmable through the EFC User Interface. The command “Set Lock Bit” enables the protection. The command “Clear Lock Bit” unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

### 8.8.3.6 SAM7S161/16

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S161/16 contains 8 lock regions and each lock region contains 32 pages of 64 bytes. Each lock region has a size of 2 Kbytes.

If a locked-region’s erase or program command occurs, the command is aborted and the LOCKE bit in the MC\_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC\_FMR register.

The 8 NVM bits are software programmable through the EFC User Interface. The command “Set Lock Bit” enables the protection. The command “Clear Lock Bit” unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

Table 8-1 summarizes the configuration of the eight devices.

**Table 8-1. Flash Configuration Summary**

SAM7S512	32	64	256 bytes
SAM7S256	16	64	256 bytes
SAM7S128	8	64	256 bytes
SAM7S64	16	32	128 bytes
SAM7S321/32	8	32	128 bytes
SAM7S161/16	8	32	64 bytes

### 8.8.4 Security Bit Feature

The SAM7S Series features a security bit, based on a specific NVM Bit. When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the Command “Set Security Bit” of the EFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full flash erase is performed. When the security bit is deactivated, all accesses to the flash are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 50 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

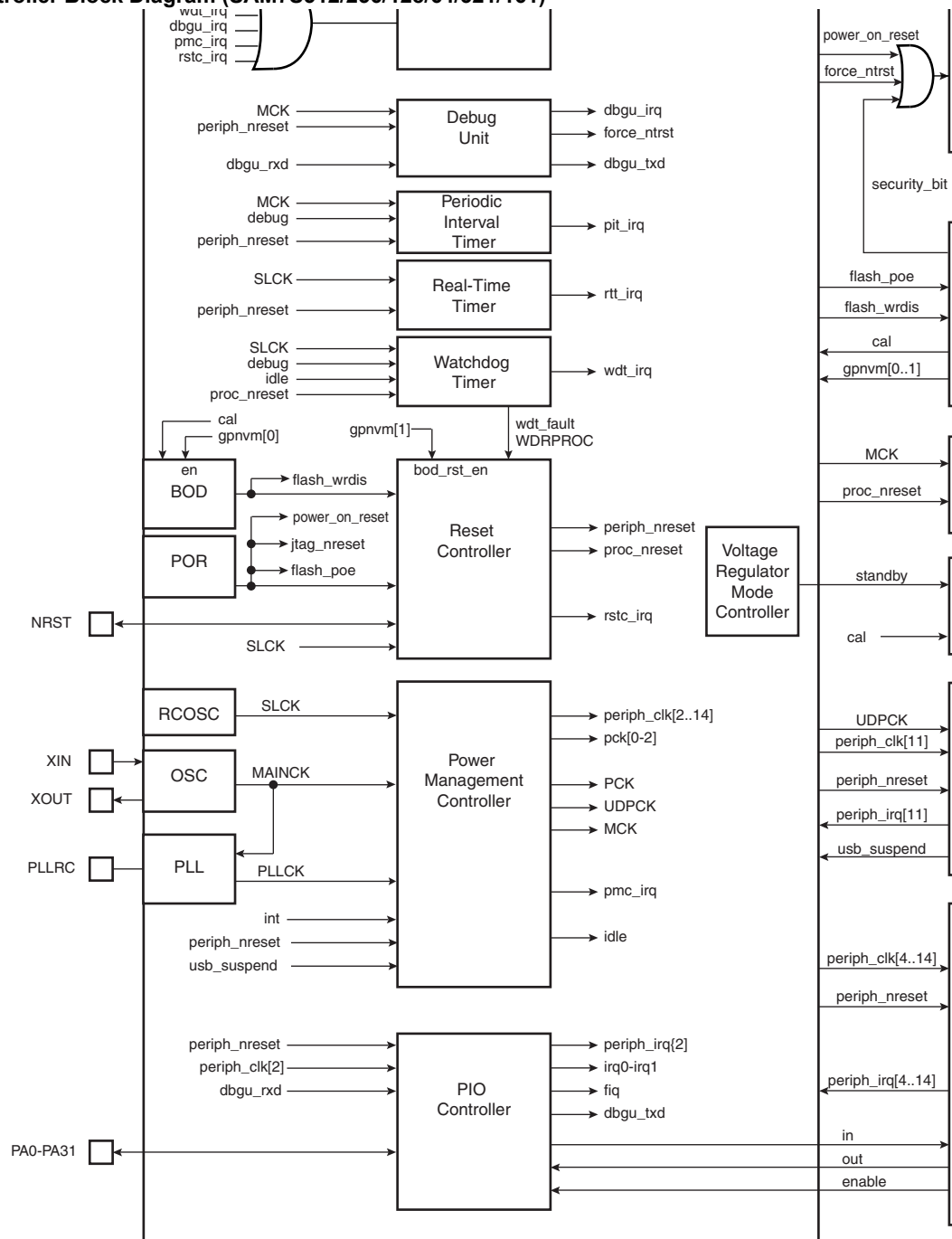
### 8.8.5 Non-volatile Brownout Detector Control

Two general purpose NVM (GPNVM) bits are used for controlling the brownout detector (BOD), so that even after a power loss, the brownout detector operations remain in their state.

These two GPNVM bits can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EFC User Interface.

- GPNVM Bit 0 is used as a brownout detector enable bit. Setting the GPNVM Bit 0 enables the BOD, clearing it disables the BOD. Asserting ERASE clears the GPNVM Bit 0 and thus disables the brownout detector by default.
- The GPNVM Bit 1 is used as a brownout reset enable signal for the reset controller. Setting the GPNVM Bit 1 enables the brownout reset when a brownout is detected, Clearing the GPNVM Bit 1 disables the brownout reset. Asserting ERASE disables the brownout reset by default.

Figure 9-1. System Controller Block Diagram (SAM7S512/256/128/64/321/161)



- One set of Chip ID Registers
- One Interface providing ICE Access Prevention
- Two-pin UART
  - Implemented features are compatible with the USART
  - Programmable Baud Rate Generator
  - Parity, Framing and Overrun Error
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
- Debug Communication Channel Support
  - Offers visibility of COMMRX and COMMTX signals from the ARM Processor
- Chip ID Registers
  - Identification of the device revision, sizes of the embedded memories, set of peripherals
  - Chip ID is 0x270B0A40 for AT91SAM7S512 Rev A
  - Chip ID is 0x270B0A4F for AT91SAM7S512 Rev B
  - Chip ID is 0x270D0940 for AT91SAM7S256 Rev A
  - Chip ID is 0x270B0941 for AT91SAM7S256 Rev B
  - Chip ID is 0x270B0942 for AT91SAM7S256 Rev C
  - Chip ID is TBD for AT91SAM7S256 Rev D
  - Chip ID is 0x270C0740 for AT91SAM7S128 Rev A
  - Chip ID is 0x270A0741 for AT91SAM7S128 Rev B
  - Chip ID is 0x270A0742 for AT91SAM7S128 Rev C
  - Chip ID is TBD for AT91SAM7S128 Rev D
  - Chip ID is 0x27090540 for AT91SAM7S64 Rev A
  - Chip ID is 0x27090543 for AT91SAM7S64 Rev B
  - Chip ID is 0x27090544 for AT91SAM7S64 Rev C
  - Chip ID is 0x27080342 for AT91SAM7S321 Rev A
  - Chip ID is 0x27080340 for AT91SAM7S32 Rev A
  - Chip ID is 0x27080341 for AT91SAM7S32 Rev B
  - Chip ID is 0x27050241 for AT91SAM7S161 Rev A
  - Chip ID is 0x27050240 for AT91SAM7S16 Rev A

Note: Refer to the errata section of the datasheet for updates on chip ID.

## 9.6 Periodic Interval Timer

- 20-bit programmable counter plus 12-bit interval counter

## 9.7 Watchdog Timer

- 12-bit key-protected Programmable Counter running on prescaled SCLK
- Provides reset or interrupt signals to the system
- Counter may be stopped while the processor is in debug state or in idle mode

## 9.8 Real-time Timer

- 32-bit free-running counter with alarm running on prescaled SCLK
- Programmable 16-bit prescaler for SCLK accuracy compensation

## 10.5 Serial Peripheral Interface

- Supports communication with external serial devices
  - Four chip selects with external decoder allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash<sup>®</sup> and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
  - Maximum frequency at up to Master Clock

## 10.6 Two-wire Interface

- Master Mode only (SAM7S512/256/128/64/321/32)
- Master, Multi-Master and Slave Mode support (SAM7S161/16)
- General Call supported in Slave Mode (SAM7S161/16)
- Compatibility with I<sup>2</sup>C compatible devices (refer to the TWI sections of the datasheet)
- One, two or three bytes internal address registers for easy Serial Memory access
- 7-bit or 10-bit slave addressing
- Sequential read/write operations

## 10.7 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode
  - 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB or LSB first
  - Optional break generation and detection
  - By 8 or by 16 over-sampling receiver frequency
  - Hardware handshaking RTS - CTS
  - Modem Signals Management DTR-DSR-DCD-RI on USART1 (not present on SAM7S32/16)
  - Receiver time-out and transmitter timeguard
  - Multi-drop Mode with address generation and detection
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

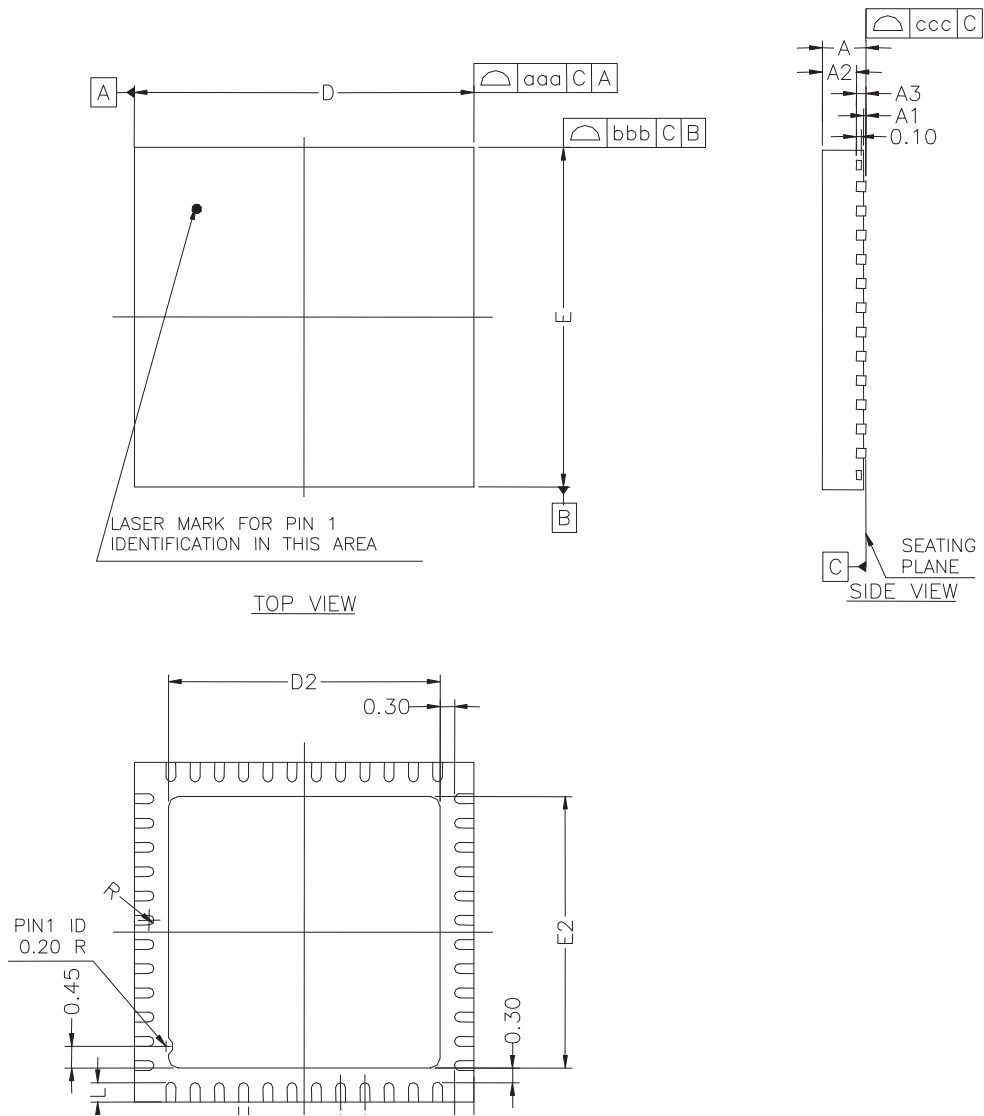


**Table 11-2. 64-lead LQFP Package Dimensions (in mm)**

Symbol						
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.383 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.383 BSC		
R2	0.08	–	0.20	0.003	–	0.008
R1	0.08	–	–	0.003	–	–
q	0°	3.5°	7°	0°	3.5°	7°
θ <sub>1</sub>	0°	–	–	0°	–	–
θ <sub>2</sub>	11°	12°	13°	11°	12°	13°
θ <sub>3</sub>	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	7.50			0.285		
E2	7.50			0.285		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

## 11.2 QFN Packages

Figure 11-2. 48-pad QFN Package



**Table 11-4. 64-pad QFN Package Dimensions (in mm)**

Symbol						
A	–	–	090	–	–	0.035
A1	–	–	0.05	–	–	0.001
A2	–	0.65	0.70	–	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.23	0.25	0.28	0.009	0.010	0.011
D	9.00 bsc			0.354 bsc		
D2	6.95	7.10	7.25	0.274	0.280	0.285
E	9.00 bsc			0.354 bsc		
E2	6.95	7.10	7.25	0.274	0.280	0.285
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 bsc			0.020 bsc		
R	0.125	–	–	0.0005	–	–
Tolerances of Form and Position						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

## 12. SAM7S Ordering Information

Table 12-1. SAM7S Series Ordering Information

MLR A Ordering Code	MLR B Ordering Code	MLR C Ordering Code	MLR D Ordering Code	Package	Package Type	Temperature Operating Range
AT91SAM7S16-AU AT91SAM7S16-MU	–	–	–	LQFP 48 QFN 48	Green	Industrial (-40 C to 85 C)
AT91SAM7S161-AU	–	–	–	LQFP 64	Green	Industrial (-40 C to 85 C)
AT91SAM7S32-AU-001 AT91SAM7S32-MU	AT91SAM7S32B-AU AT91SAM7S32B-MU			LQFP 48 QFN 48	Green	Industrial (-40 C to 85 C)
AT91SAM7S321-AU AT91SAM7S321-MU	–	–	–	LQFP 64 QFN 64	Green	Industrial (-40 C to 85 C)
–	AT91SAM7S64B-AU AT91SAM7S64B-MU	AT91SAM7S64C-AU AT91SAM7S64C-MU	–	LQFP 64 QFN 64	Green	Industrial (-40 C to 85 C)
–	AT91SAM7S128-AU-001 AT91SAM7S128-MU	AT91SAM7S128C-AU AT91SAM7S128C-MU	AT91SAM7S128D-AU AT91SAM7S128D-MU	LQFP 64 QFN 64	Green	Industrial (-40 C to 85 C)
–	AT91SAM7S256-AU-001 AT91SAM7S256-MU	AT91SAM7S256C-AU AT91SAM7S256C-MU	AT91SAM7S256D-AU AT91SAM7S256D-MU	LQFP 64 QFN 64	Green	Industrial (-40 C to 85 C)
AT91SAM7S512-AU AT91SAM7S512-MU	AT91SAM7S512B-AU AT91SAM7S512B-MU	–	–	LQFP 64 QFN 64	Green	Industrial (-40 C to 85 C)

## Revision History

6175AS	First issue - Unqualified on Intranet Corresponds to 6175A full datasheet approval loop. Qualified on Intranet.	
6175BS	<a href="#">Section 8. "Memories" on page 18</a> updated: 2 ms => 3 ms, 10 ms => 15 ms, 4 ms => 6 ms	CSR05-529
6175CS	<a href="#">Section 12. "SAM7S Ordering Information" AT91SAM7S321</a> changed in <a href="#">Table 12-1 on page 47</a>	#2342
6175DS	"Features", <a href="#">Table 1-1, "Configuration Summary," on page 3</a> , <a href="#">Section 4. "Package and Pinout"</a> <a href="#">Section 12. "SAM7S Ordering Information"</a> QFN package information added	#2444
6175ES	<a href="#">Section 10.11 on page 39</a> USB Device port, Ping-pong Mode includes Isochronous endpoints. "Features" <a href="#">on page 1</a> , and global: AT91SAM7S512 added to series. Reference to Manchester Encoder removed from USART. <a href="#">Section 8. "Memories"</a> Reformatted Memories, Consolidated Memory Mapping in <a href="#">Figure 8-1 on page 20</a> <a href="#">Section 10. "Peripherals"</a> Reordered sub sections. <a href="#">Section 11. "Package Drawings"</a> QFN, LQFP package drawings added. "ice_nreset" signals changed to "power_on_reset" in System Controller block diagrams, <a href="#">Figure 9-1 on page 26</a> and <a href="#">Figure 9-2 on page 27</a> . <a href="#">Section 4. "Package and Pinout"</a> LQFP and QFN Package Outlines replace Mechanical Overview. <a href="#">Section 10.1 "User Interface"</a> , User peripherals are mapped between 0xF000 0000 and 0xFFFF EFFF. SYSIRQ changed to SYSC in "Peripheral Identifiers" <a href="#">Table 10-1</a> and <a href="#">Table 10-2</a>	specs  #2748  #2832 (DBGU IP)  rfo review
6175FS	AT91SAM7S161 and AT91SAM7S16 added to product family <b>Features:</b> Timer Counter, <a href="#">on page 2</a> product specific information rewritten, <a href="#">Table 1-1, "Configuration Summary," on page 3</a> , footnote explains TC on AT91SAM7S32/16 has only two channels accessible via PIO, and in <a href="#">Section 10.9 "Timer Counter"</a> , precisions added to "compare and capture" output/input. <a href="#">Section 10.6 "Two-wire Interface"</a> , updated reference to I <sup>2</sup> C compatibility, internal address registers, slave addressing, Modes for AT91SAM7S161/16 "One Two-wire Interface (TWI)" <a href="#">on page 2</a> , updated in Features <a href="#">Section 10.12 "Analog-to-digital Converter"</a> , updated Successive Approximation Register ADC and the INL, DNL ± values of LSB. <a href="#">Section 8.8.3 "Lock Regions"</a> , locked-region's erase or program command updated <a href="#">Section 9.5 "Debug Unit"</a> , Chip ID updated. <a href="#">Section 6. "I/O Lines Considerations"</a> , JTAG Port Pin, Test Pin, Erase Pin, updated.	BDs  4208  rfo review  4325  5063