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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	I²C, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	32
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at91sam7s256c-mu

- **Debug Unit (DBGU)**
 - 2-wire UART and Support for Debug Communication Channel interrupt, Programmable ICE Access Prevention
 - Mode for General Purpose 2-wire UART Serial Communication
- **Periodic Interval Timer (PIT)**
 - 20-bit Programmable Counter plus 12-bit Interval Counter
- **Windowed Watchdog (WDT)**
 - 12-bit key-protected Programmable Counter
 - Provides Reset or Interrupt Signals to the System
 - Counter May Be Stopped While the Processor is in Debug State or in Idle Mode
- **Real-time Timer (RTT)**
 - 32-bit Free-running Counter with Alarm
 - Runs Off the Internal RC Oscillator
- **One Parallel Input/Output Controller (PIOA)**
 - Thirty-two (SAM7S512/256/128/64/321/161) or twenty-one (SAM7S32/16) Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
 - Input Change Interrupt Capability on Each I/O Line
 - Individually Programmable Open-drain, Pull-up resistor and Synchronous Output
- **Eleven (SAM7S512/256/128/64/321/161) or Nine (SAM7S32/16) Peripheral DMA Controller (PDC) Channels**
- **One USB 2.0 Full Speed (12 Mbits per Second) Device Port (Except for the SAM7S32/16).**
 - On-chip Transceiver, 328-byte Configurable Integrated FIFOs
- **One Synchronous Serial Controller (SSC)**
 - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
 - I²S Analog Interface Support, Time Division Multiplex Support
 - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- **Two (SAM7S512/256/128/64/321/161) or One (SAM7S32/16) Universal Synchronous/Asynchronous Receiver Transmitters (USART)**
 - Individual Baud Rate Generator, IrDA[®] Infrared Modulation/Demodulation
 - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
 - Full Modem Line Support on USART1 (SAM7S512/256/128/64/321/161)
- **One Master/Slave Serial Peripheral Interface (SPI)**
 - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- **One Three-channel 16-bit Timer/Counter (TC)**
 - Three External Clock Input and Two Multi-purpose I/O Pins per Channel (SAM7S512/256/128/64/321/161)
 - One External Clock Input and Two Multi-purpose I/O Pins for the first Two Channels Only (SAM7S32/16)
 - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- **One Four-channel 16-bit PWM Controller (PWMC)**
- **One Two-wire Interface (TWI)**
 - Master Mode Support Only, All Two-wire Atmel EEPROMs and I²C Compatible Devices Supported (SAM7S512/256/128/64/321/32)
 - Master, Multi-Master and Slave Mode Support, All Two-wire Atmel EEPROMs and I²C Compatible Devices Supported (SAM7S161/16)
- **One 8-channel 10-bit Analog-to-Digital Converter, Four Channels Multiplexed with Digital I/Os**
- **SAM-BA[™] Boot Assistant**
 - Default Boot program
 - Interface with SAM-BA Graphic User Interface
- **IEEE[®] 1149.1 JTAG Boundary Scan on All Digital Pins**
- **5V-tolerant I/Os, including Four High-current Drive I/O lines, Up to 16 mA Each (SAM7S161/16 I/Os Not 5V-tolerant)**
- **Power Supplies**
 - Embedded 1.8V Regulator, Drawing up to 100 mA for the Core and External Components
 - 3.3V or 1.8V VDDIO I/O Lines Power Supply, Independent 3.3V VDDFLASH Flash Power Supply
 - 1.8V VDDCORE Core Power Supply with Brown-out Detector

- **Fully Static Operation: Up to 55 MHz at 1.65V and 85° C Worst Case Conditions**
- **Available in 64-lead LQFP Green or 64-pad QFN Green Package (SAM7S512/256/128/64/321/161) and 48-lead LQFP Green or 48-pad QFN Green Package (SAM7S32/16)**

1. Description

Atmel's SAM7S is a series of low pincount Flash microcontrollers based on the 32-bit ARM RISC processor. It features a high-speed Flash and an SRAM, a large set of peripherals, including a USB 2.0 device (except for the SAM7S32 and SAM7S16), and a complete set of system functions minimizing the number of external components. The device is an ideal migration path for 8-bit microcontroller users looking for additional performance and extended memory.

The embedded Flash memory can be programmed in-system via the JTAG-ICE interface or via a parallel interface on a production programmer prior to mounting. Built-in lock bits and a security bit protect the firmware from accidental overwrite and preserves its confidentiality.

The SAM7S Series system controller includes a reset controller capable of managing the power-on sequence of the microcontroller and the complete system. Correct device operation can be monitored by a built-in brownout detector and a watchdog running off an integrated RC oscillator.

The SAM7S Series are general-purpose microcontrollers. Their integrated USB Device port makes them ideal devices for peripheral applications requiring connectivity to a PC or cellular phone. Their aggressive price point and high level of integration pushes their scope of use far into the cost-sensitive, high-volume consumer market.

1.1 Configuration Summary of the SAM7S512, SAM7S256, SAM7S128, SAM7S64, SAM7S321, SAM7S32, SAM7S161 and SAM7S16

The SAM7S512, SAM7S256, SAM7S128, SAM7S64, SAM7S321, SAM7S32, SAM7S161 and SAM7S16 differ in memory size, peripheral set and package. [Table 1-1](#) summarizes the configuration of the six devices.

Except for the SAM7S32/16, all other SAM7S devices are package and pinout compatible.

Table 1-1. Configuration Summary

SAM7S512	512 Kbytes	Master	dual plane	64 Kbytes	1	2 ^{(1) (2)}	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S256	256 Kbytes	Master	single plane	64 Kbytes	1	2 ^{(1) (2)}	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S128	128 Kbytes	Master	single plane	32 Kbytes	1	2 ^{(1) (2)}	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S64	64 Kbytes	Master	single plane	16 Kbytes	1	2 ⁽²⁾	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S321	32 Kbytes	Master	single plane	8 Kbytes	1	2 ⁽²⁾	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S32	32 Kbytes	Master	single plane	8 Kbytes	not present	1	1	9	3 ⁽³⁾	Yes	21	LQFP/ QFN 48
SAM7S161	16 Kbytes	Master/ Slave	single plane	4 Kbytes	1	2 ⁽²⁾	2	11	3	No	32	LQFP
SAM7S16	16 Kbytes	Master/ Slave	single plane	4 Kbytes	not present	1	1	9	3 ⁽³⁾	No	21	LQFP/ QFN 48

- Notes:
1. Fractional Baud Rate.
 2. Full modem line support on USART1.
 3. Only two TC channels are accessible through the PIO.

2. Block Diagram

Figure 2-1. SAM7S512/256/128/64/321/161 Block Diagram

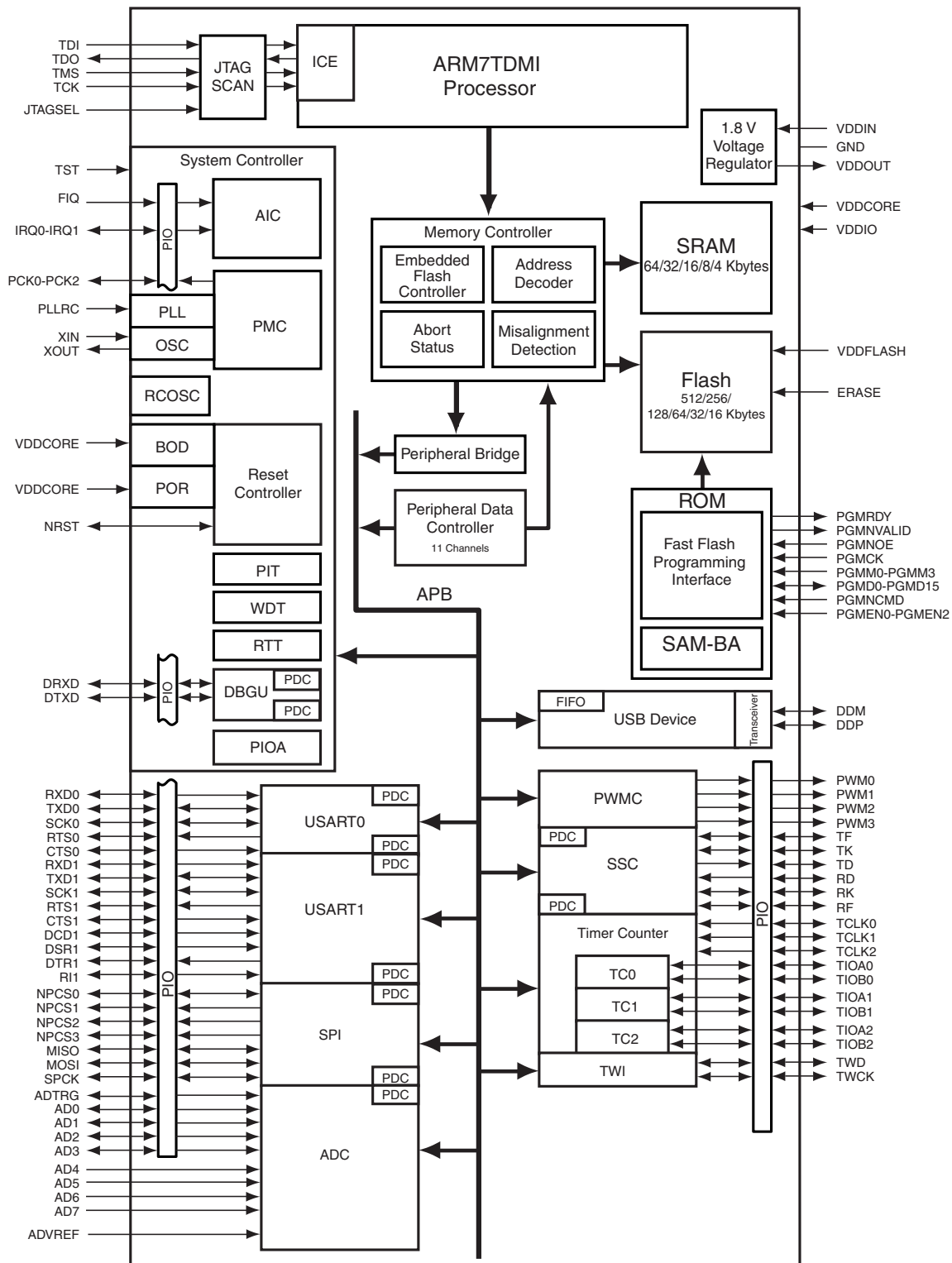


Table 3-1. Signal Description List (Continued)

DDM	USB Device Port Data -	Analog		not present on SAM7S32/16
DDP	USB Device Port Data +	Analog		not present on SAM7S32/16
SCK0 - SCK1	Serial Clock	I/O		SCK1 not present on SAM7S32/16
TXD0 - TXD1	Transmit Data	I/O		TXD1 not present on SAM7S32/16
RXD0 - RXD1	Receive Data	Input		RXD1 not present on SAM7S32/16
RTS0 - RTS1	Request To Send	Output		RTS1 not present on SAM7S32/16
CTS0 - CTS1	Clear To Send	Input		CTS1 not present on SAM7S32/16
DCD1	Data Carrier Detect	Input		not present on SAM7S32/16
DTR1	Data Terminal Ready	Output		not present on SAM7S32/16
DSR1	Data Set Ready	Input		not present on SAM7S32/16
RI1	Ring Indicator	Input		not present on SAM7S32/16
TD	Transmit Data	Output		
RD	Receive Data	Input		
TK	Transmit Clock	I/O		
RK	Receive Clock	I/O		
TF	Transmit Frame Sync	I/O		
RF	Receive Frame Sync	I/O		
TCLK0 - TCLK2	External Clock Inputs	Input		TCLK1 and TCLK2 not present on SAM7S32/16
TIOA0 - TIOA2	I/O Line A	I/O		TIOA2 not present on SAM7S32/16
TIOB0 - TIOB2	I/O Line B	I/O		TIOB2 not present on SAM7S32/16
PWM0 - PWM3	PWM Channels	Output		
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
SPCK	SPI Serial Clock	I/O		
NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
NPCS1-NPCS3	SPI Peripheral Chip Select 1 to 3	Output	Low	

Table 3-1. Signal Description List (Continued)

TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		
AD0-AD3	Analog Inputs	Analog		Digital pulled-up inputs at reset
AD4-AD7	Analog Inputs	Analog		Analog Inputs
ADTRG	ADC Trigger	Input		
ADVREF	ADC Reference	Analog		
PGMEN0-PGMEN2	Programming Enabling	Input		
PGMM0-PGMM3	Programming Mode	Input		
PGMD0-PGMD15	Programming Data	I/O		PGMD0-PGMD7 only on SAM7S32/16
PGMRDY	Programming Ready	Output	High	
PGMNVALID	Data Direction	Output	Low	
PGMNOE	Programming Read	Input	Low	
PGMCK	Programming Clock	Input		
PGMNCMD	Programming Command	Input	Low	

Note: 1. Refer to [Section 6. "I/O Lines Considerations"](#) on page 14.

4. Package and Pinout

The SAM7S512/256/128/64/321 are available in a 64-lead LQFP or 64-pad QFN package.

The SAM7S161 is available in a 64-Lead LQFP package.

The SAM7S32/16 are available in a 48-lead LQFP or 48-pad QFN package.

4.1 64-lead LQFP and 64-pad QFN Package Outlines

Figure 4-1 and Figure 4-2 show the orientation of the 64-lead LQFP and the 64-pad QFN package. A detailed mechanical description is given in the section Mechanical Characteristics of the full datasheet.

Figure 4-1. 64-lead LQFP Package (Top View)

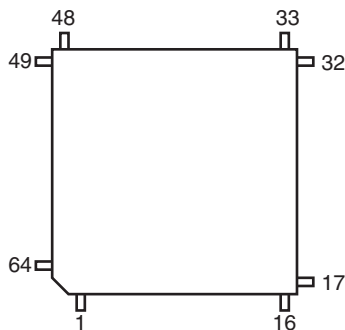
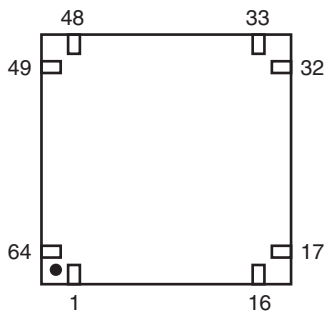


Figure 4-2. 64-pad QFN Package (Top View)



7. Processor and Architecture

7.1 ARM7TDMI Processor

- RISC processor based on ARMv4T Von Neumann architecture
 - Runs at up to 55 MHz, providing 0.9 MIPS/MHz
- Two instruction sets
 - ARM® high-performance 32-bit instruction set
 - Thumb® high code density 16-bit instruction set
- Three-stage pipeline architecture
 - Instruction Fetch (F)
 - Instruction Decode (D)
 - Execute (E)

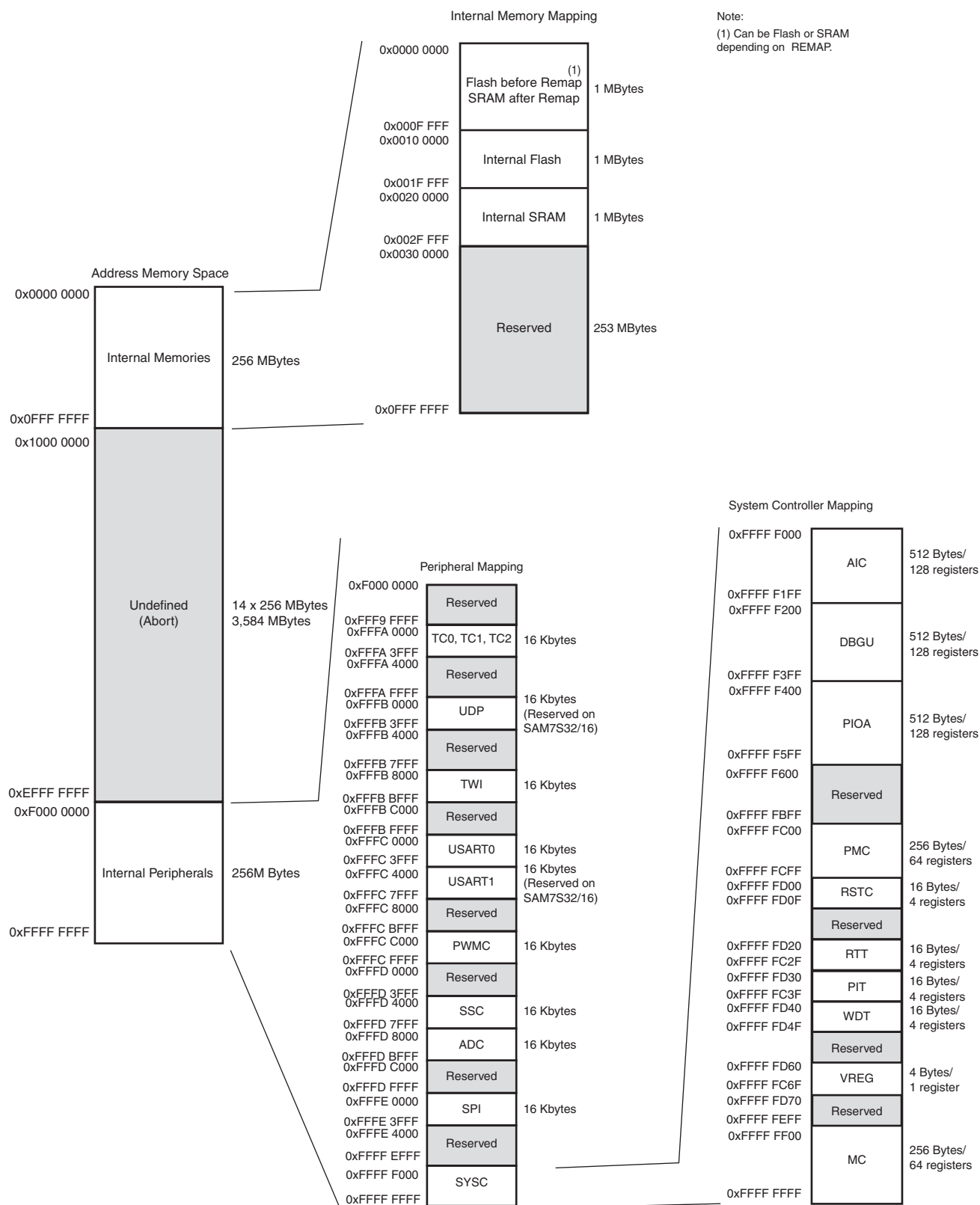
7.2 Debug and Test Features

- Integrated EmbeddedICE™ (embedded in-circuit emulator)
 - Two watchpoint units
 - Test access port accessible through a JTAG protocol
 - Debug communication channel
- Debug Unit
 - Two-pin UART
 - Debug communication channel interrupt handling
 - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on all digital pins

7.3 Memory Controller

- Bus Arbiter
 - Handles requests from the ARM7TDMI and the Peripheral DMA Controller
- Address decoder provides selection signals for
 - Three internal 1 Mbyte memory areas
 - One 256 Mbyte embedded peripheral area
- Abort Status Registers
 - Source, Type and all parameters of the access leading to an abort are saved
 - Facilitates debug by detection of bad pointers
- Misalignment Detector
 - Alignment checking of all data accesses
 - Abort generation in case of misalignment
- Remap Command
 - Remaps the SRAM in place of the embedded non-volatile memory
 - Allows handling of dynamic exception vectors
- Embedded Flash Controller
 - Embedded Flash interface, up to three programmable wait states
 - Prefetch buffer, buffering and anticipating the 16-bit requests, reducing the required wait states
 - Key-protected program, erase and lock/unlock sequencer
 - Single command for erasing, programming and locking operations
 - Interrupt generation in case of forbidden operation

Figure 8-1. SAM SAM7S512/256/128/64/321/32/161/16 Memory Mapping



8.7 Memory Mapping

8.7.1 Internal SRAM

- The SAM7S512 embeds a high-speed 64-Kbyte SRAM bank.
- The SAM7S256 embeds a high-speed 64-Kbyte SRAM bank.
- The SAM7S128 embeds a high-speed 32-Kbyte SRAM bank.
- The SAM7S64 embeds a high-speed 16-Kbyte SRAM bank.
- The SAM7S321 embeds a high-speed 8-Kbyte SRAM bank.
- The SAM7S32 embeds a high-speed 8-Kbyte SRAM bank.
- The SAM7S161 embeds a high-speed 4-Kbyte SRAM bank.
- The SAM7S16 embeds a high-speed 4-Kbyte SRAM bank.

After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x0020 0000. After Remap, the SRAM also becomes available at address 0x0.

8.7.2 Internal ROM

The SAM7S Series embeds an Internal ROM. The ROM contains the FFPI and the SAM-BA program.

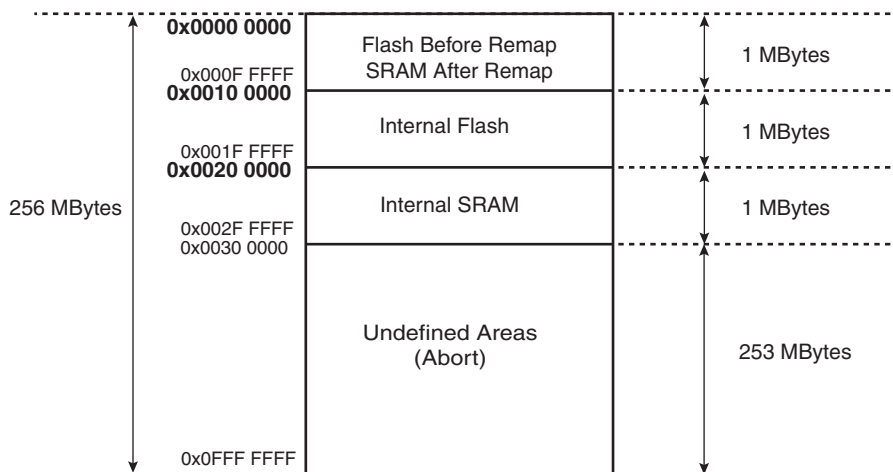
The internal ROM is not mapped by default.

8.7.3 Internal Flash

- The SAM7S512 features two contiguous banks (dual plane) of 256 Kbytes of Flash.
- The SAM7S256 features one bank (single plane) of 256 Kbytes of Flash.
- The SAM7S128 features one bank (single plane) of 128 Kbytes of Flash.
- The SAM7S64 features one bank (single plane) of 64 Kbytes of Flash.
- The SAM7S321/32 features one bank (single plane) of 32 Kbytes of Flash.
- The SAM7S161/16 features one bank (single plane) of 16 Kbytes of Flash.

At any time, the Flash is mapped to address 0x0010 0000. It is also accessible at address 0x0 after the reset and before the Remap Command.

Figure 8-2. Internal Memory Mapping



The 8 NVM bits are software programmable through the EFC User Interface. The command “Set Lock Bit” enables the protection. The command “Clear Lock Bit” unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.6 SAM7S161/16

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S161/16 contains 8 lock regions and each lock region contains 32 pages of 64 bytes. Each lock region has a size of 2 Kbytes.

If a locked-region’s erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 8 NVM bits are software programmable through the EFC User Interface. The command “Set Lock Bit” enables the protection. The command “Clear Lock Bit” unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

Table 8-1 summarizes the configuration of the eight devices.

Table 8-1. Flash Configuration Summary

SAM7S512	32	64	256 bytes
SAM7S256	16	64	256 bytes
SAM7S128	8	64	256 bytes
SAM7S64	16	32	128 bytes
SAM7S321/32	8	32	128 bytes
SAM7S161/16	8	32	64 bytes

8.8.4 Security Bit Feature

The SAM7S Series features a security bit, based on a specific NVM Bit. When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the Command “Set Security Bit” of the EFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full flash erase is performed. When the security bit is deactivated, all accesses to the flash are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 50 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

8.8.5 Non-volatile Brownout Detector Control

Two general purpose NVM (GPNVM) bits are used for controlling the brownout detector (BOD), so that even after a power loss, the brownout detector operations remain in their state.

These two GPNVM bits can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EFC User Interface.

- GPNVM Bit 0 is used as a brownout detector enable bit. Setting the GPNVM Bit 0 enables the BOD, clearing it disables the BOD. Asserting ERASE clears the GPNVM Bit 0 and thus disables the brownout detector by default.
- The GPNVM Bit 1 is used as a brownout reset enable signal for the reset controller. Setting the GPNVM Bit 1 enables the brownout reset when a brownout is detected, Clearing the GPNVM Bit 1 disables the brownout reset. Asserting ERASE disables the brownout reset by default.

Figure 9-1. System Controller Block Diagram (SAM7S512/256/128/64/321/161)

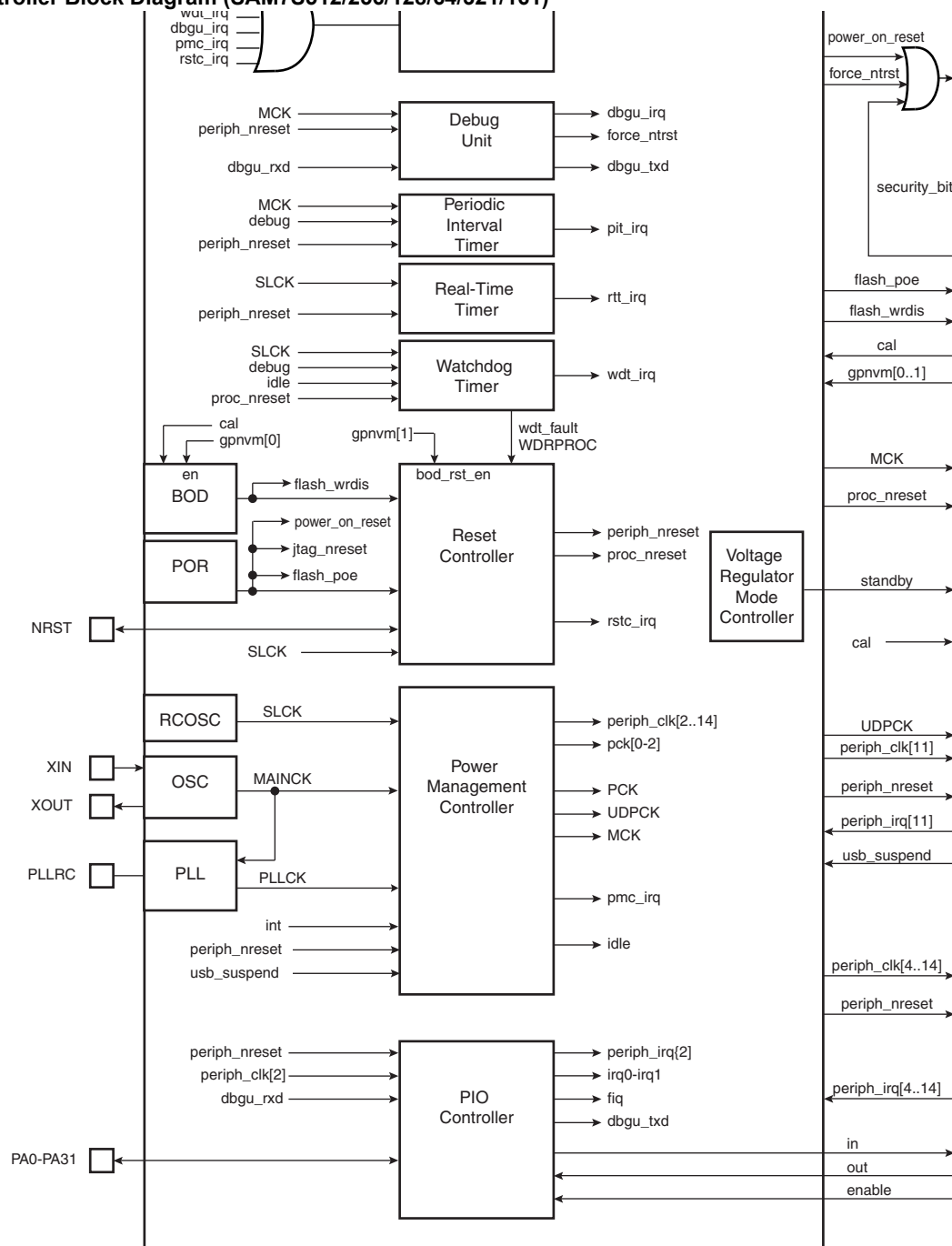


Figure 9-2. System Controller Block Diagram (SAM7S32/16)

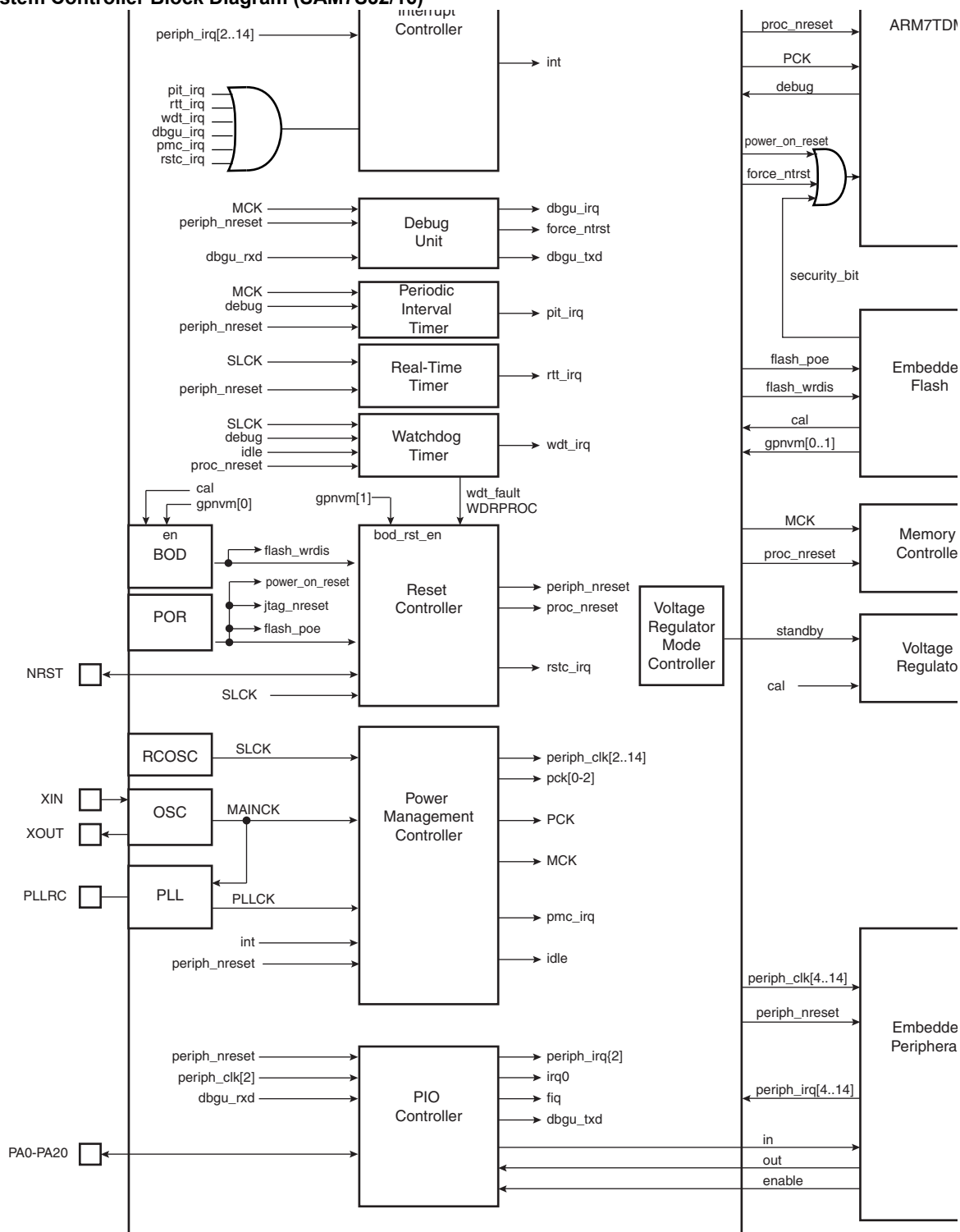
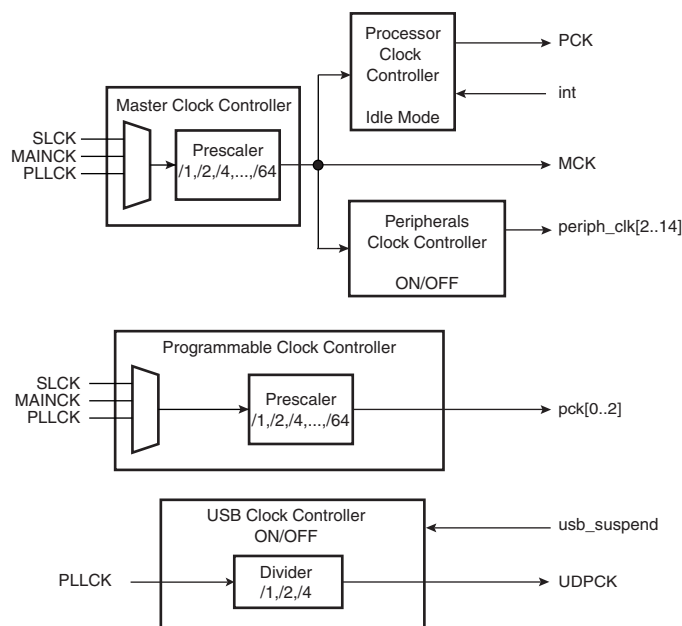


Figure 9-4. Power Management Controller Block Diagram



9.4 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of an ARM Processor
- Individually maskable and vectored interrupt sources
 - Source 0 is reserved for the Fast Interrupt Input (FIQ)
 - Source 1 is reserved for system peripherals RTT, PIT, EFC, PMC, DBGU, etc.)
 - Other sources control the peripheral interrupts or external interrupts
 - Programmable edge-triggered or level-sensitive internal sources
 - Programmable positive/negative edge-triggered or high/low level-sensitive external sources
- 8-level Priority Controller
 - Drives the normal interrupt of the processor
 - Handles priority of the interrupt sources
 - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
 - Optimizes interrupt service routine branch and execution
 - One 32-bit vector register per interrupt source
 - Interrupt vector register reads the corresponding current interrupt vector
- Protect Mode
 - Easy debugging by preventing automatic operations
- Fast Forcing
 - Permits redirecting any interrupt source on the fast interrupt
- General Interrupt Mask
 - Provides processor synchronization on events without triggering an interrupt

9.5 Debug Unit

- Comprises:
 - One two-pin UART
 - One Interface for the Debug Communication Channel (DCC) support

10.5 Serial Peripheral Interface

- Supports communication with external serial devices
 - Four chip selects with external decoder allow communication with up to 15 peripherals
 - Serial memories, such as DataFlash® and 3-wire EEPROMs
 - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
 - External co-processors
- Master or slave serial peripheral bus interface
 - 8- to 16-bit programmable data length per chip select
 - Programmable phase and polarity per chip select
 - Programmable transfer delays between consecutive transfers and between clock and data per chip select
 - Programmable delay between consecutive transfers
 - Selectable mode fault detection
 - Maximum frequency at up to Master Clock

10.6 Two-wire Interface

- Master Mode only (SAM7S512/256/128/64/321/32)
- Master, Multi-Master and Slave Mode support (SAM7S161/16)
- General Call supported in Slave Mode (SAM7S161/16)
- Compatibility with I²C compatible devices (refer to the TWI sections of the datasheet)
- One, two or three bytes internal address registers for easy Serial Memory access
- 7-bit or 10-bit slave addressing
- Sequential read/write operations

10.7 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
 - 1, 1.5 or 2 stop bits in Asynchronous Mode
 - 1 or 2 stop bits in Synchronous Mode
 - Parity generation and error detection
 - Framing error detection, overrun error detection
 - MSB or LSB first
 - Optional break generation and detection
 - By 8 or by 16 over-sampling receiver frequency
 - Hardware handshaking RTS - CTS
 - Modem Signals Management DTR-DSR-DCD-RI on USART1 (not present on SAM7S32/16)
 - Receiver time-out and transmitter timeguard
 - Multi-drop Mode with address generation and detection
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
 - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
 - Communication at up to 115.2 Kbps
- Test Modes
 - Remote Loopback, Local Loopback, Automatic Echo

- Programmable center or left aligned output waveform

10.11 USB Device Port (Does not pertain to SAM7S32/16)

- USB V2.0 full-speed compliant, 12 Mbits per second.
- Embedded USB V2.0 full-speed transceiver
- Embedded 328-byte dual-port RAM for endpoints
- Four endpoints
 - Endpoint 0: 8 bytes
 - Endpoint 1 and 2: 64 bytes ping-pong
 - Endpoint 3: 64 bytes
 - Ping-pong Mode (two memory banks) for isochronous and bulk endpoints
- Suspend/resume logic

10.12 Analog-to-digital Converter

- 8-channel ADC
- 10-bit 384 Ksamples/sec. or 8-bit 583 Ksamples/sec. Successive Approximation Register ADC
- ± 2 LSB Integral Non Linearity, ± 1 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger source
 - Hardware or software trigger
 - External trigger pin
 - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer
 - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels
- Four of eight analog inputs shared with digital signals

Table 11-2. 64-lead LQFP Package Dimensions (in mm)

Symbol						
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.383 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.383 BSC		
R2	0.08	–	0.20	0.003	–	0.008
R1	0.08	–	–	0.003	–	–
q	0°	3.5°	7°	0°	3.5°	7°
θ ₁	0°	–	–	0°	–	–
θ ₂	11°	12°	13°	11°	12°	13°
θ ₃	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	7.50			0.285		
E2	7.50			0.285		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Table 11-3. 48-pad QFN Package Dimensions (in mm)

Symbol						
A	–	–	090	–	–	0.035
A1	–	–	0.050	–	–	0.002
A2	–	0.65	0.70	–	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.18	0.20	0.23	0.007	0.008	0.009
D	7.00 bsc			0.276 bsc		
D2	5.45	5.60	5.75	0.215	0.220	0.226
E	7.00 bsc			0.276 bsc		
E2	5.45	5.60	5.75	0.215	0.220	0.226
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 bsc			0.020 bsc		
R	0.09	–	–	0.004	–	–
Tolerances of Form and Position						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

Table 11-4. 64-pad QFN Package Dimensions (in mm)

Symbol						
A	–	–	090	–	–	0.035
A1	–	–	0.05	–	–	0.001
A2	–	0.65	0.70	–	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.23	0.25	0.28	0.009	0.010	0.011
D	9.00 bsc			0.354 bsc		
D2	6.95	7.10	7.25	0.274	0.280	0.285
E	9.00 bsc			0.354 bsc		
E2	6.95	7.10	7.25	0.274	0.280	0.285
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 bsc			0.020 bsc		
R	0.125	–	–	0.0005	–	–
Tolerances of Form and Position						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		



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