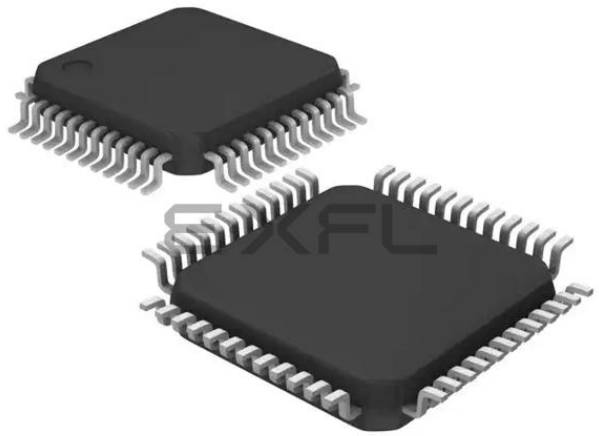

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	I²C, SPI, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam7s32-au-001

- Debug Unit (DBGU)
  - 2-wire UART and Support for Debug Communication Channel interrupt, Programmable ICE Access Prevention
  - Mode for General Purpose 2-wire UART Serial Communication
- Periodic Interval Timer (PIT)
  - 20-bit Programmable Counter plus 12-bit Interval Counter
- Windowed Watchdog (WDT)
  - 12-bit key-protected Programmable Counter
  - Provides Reset or Interrupt Signals to the System
  - Counter May Be Stopped While the Processor is in Debug State or in Idle Mode
- Real-time Timer (RTT)
  - 32-bit Free-running Counter with Alarm
  - Runs Off the Internal RC Oscillator
- One Parallel Input/Output Controller (PIOA)
  - Thirty-two (SAM7S512/256/128/64/321/161) or twenty-one (SAM7S32/16) Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up resistor and Synchronous Output
- Eleven (SAM7S512/256/128/64/321/161) or Nine (SAM7S32/16) Peripheral DMA Controller (PDC) Channels
- One USB 2.0 Full Speed (12 Mbits per Second) Device Port (Except for the SAM7S32/16).
  - On-chip Transceiver, 328-byte Configurable Integrated FIFOs
- One Synchronous Serial Controller (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Two (SAM7S512/256/128/64/321/161) or One (SAM7S32/16) Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
  - Full Modem Line Support on USART1 (SAM7S512/256/128/64/321/161)
- One Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counter (TC)
  - Three External Clock Input and Two Multi-purpose I/O Pins per Channel (SAM7S512/256/128/64/321/161)
  - One External Clock Input and Two Multi-purpose I/O Pins for the first Two Channels Only (SAM7S32/16)
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- One Four-channel 16-bit PWM Controller (PWMC)
- One Two-wire Interface (TWI)
  - Master Mode Support Only, All Two-wire Atmel EEPROMs and I²C Compatible Devices Supported (SAM7S512/256/128/64/321/32)
  - Master, Multi-Master and Slave Mode Support, All Two-wire Atmel EEPROMs and I²C Compatible Devices Supported (SAM7S161/16)
- One 8-channel 10-bit Analog-to-Digital Converter, Four Channels Multiplexed with Digital I/Os
- SAM-BA™ Boot Assistant
  - Default Boot program
  - Interface with SAM-BA Graphic User Interface
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- 5V-tolerant I/Os, including Four High-current Drive I/O lines, Up to 16 mA Each (SAM7S161/16 I/Os Not 5V-tolerant)
- Power Supplies
  - Embedded 1.8V Regulator, Drawing up to 100 mA for the Core and External Components
  - 3.3V or 1.8V VDDIO I/O Lines Power Supply, Independent 3.3V VDDFLASH Flash Power Supply
  - 1.8V VDDCORE Core Power Supp

3. Signal Description

Table 3-1. Signal Description List

VDDIN	Voltage and ADC Regulator Power Supply Input	Power		3.0 to 3.6V
VDDOUT	Voltage Regulator Output	Power		1.85V nominal
VDDFLASH	Flash Power Supply	Power		3.0V to 3.6V
VDDIO	I/O Lines Power Supply	Power		3.0V to 3.6V or 1.65V to 1.95V
VDDCORE	Core Power Supply	Power		1.65V to 1.95V
VDDPLL	PLL	Power		1.65V to 1.95V
GND	Ground	Ground		
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
PLLRC	PLL Filter	Input		
PCK0 - PCK2	Programmable Clock Output	Output		
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor
JTAGSEL	JTAG Selection	Input		Pull-down resistor(1)
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	Pull-down resistor(1)
NRST	Microcontroller Reset	I/O	Low	Open-drain with pull-Up resistor
TST	Test Mode Select	Input	High	Pull-down resistor(1)
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
IRQ0 - IRQ1	External Interrupt Inputs	Input		IRQ1 not present on SAM7S32/16
FIQ	Fast Interrupt Input	Input		
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset PA0 - PA20 only on SAM7S32/16

Table 3-1. Signal Description List (Continued)

DDM	USB Device Port Data -	Analog		not present on SAM7S32/16
DDP	USB Device Port Data +	Analog		not present on SAM7S32/16
SCK0 - SCK1	Serial Clock	I/O		SCK1 not present on SAM7S32/16
TXD0 - TXD1	Transmit Data	I/O		TXD1 not present on SAM7S32/16
RXD0 - RXD1	Receive Data	Input		RXD1 not present on SAM7S32/16
RTS0 - RTS1	Request To Send	Output		RTS1 not present on SAM7S32/16
CTS0 - CTS1	Clear To Send	Input		CTS1 not present on SAM7S32/16
DCD1	Data Carrier Detect	Input		not present on SAM7S32/16
DTR1	Data Terminal Ready	Output		not present on SAM7S32/16
DSR1	Data Set Ready	Input		not present on SAM7S32/16
RI1	Ring Indicator	Input		not present on SAM7S32/16
TD	Transmit Data	Output		
RD	Receive Data	Input		
TK	Transmit Clock	I/O		
RK	Receive Clock	I/O		
TF	Transmit Frame Sync	I/O		
RF	Receive Frame Sync	I/O		
TCLK0 - TCLK2	External Clock Inputs	Input		TCLK1 and TCLK2 not present on SAM7S32/16
TIOA0 - TIOA2	I/O Line A	I/O		TIOA2 not present on SAM7S32/16
TIOB0 - TIOB2	I/O Line B	I/O		TIOB2 not present on SAM7S32/16
PWM0 - PWM3	PWM Channels	Output		
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
SPCK	SPI Serial Clock	I/O		
NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
NPCS1-NPCS3	SPI Peripheral Chip Select 1 to 3	Output	Low	

4. Package and Pinout

The SAM7S512/256/128/64/321 are available in a 64-lead LQFP or 64-pad QFN package.

The SAM7S161 is available in a 64-Lead LQFP package.

The SAM7S32/16 are available in a 48-lead LQFP or 48-pad QFN package.

4.1 64-lead LQFP and 64-pad QFN Package Outlines

Figure 4-1 and Figure 4-2 show the orientation of the 64-lead LQFP and the 64-pad QFN package. A detailed mechanical description is given in the section Mechanical Characteristics of the full datasheet.

Figure 4-1. 64-lead LQFP Package (Top View)

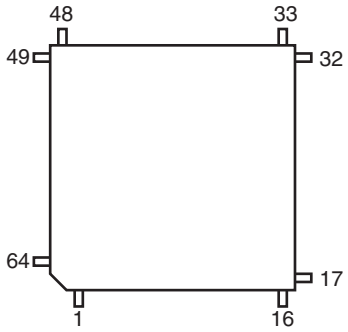
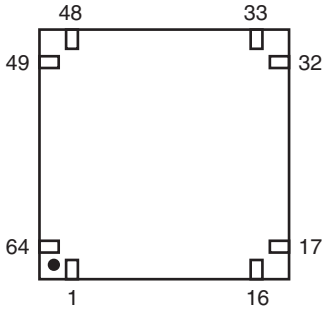


Figure 4-2. 64-pad QFN Package (Top View)



4.3 48-lead LQFP and 48-pad QFN Package Outlines

Figure 4-3 and Figure 4-4 show the orientation of the 48-lead LQFP and the 48-pad QFN package. A detailed mechanical description is given in the section Mechanical Characteristics of the full datasheet.

Figure 4-3. 48-lead LQFP Package (Top View)

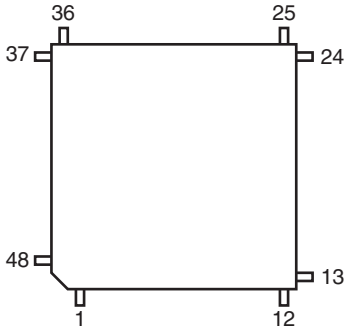
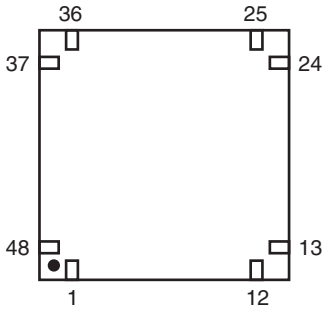


Figure 4-4. 48-pad QFN Package (Top View)



4.4 48-lead LQFP and 48-pad QFN Pinout

Table 4-2. SAM7S32/16 Pinout[1]

1	ADVREF	13	VDDIO	25	TDI	37	TDO
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	AD4	15	PA15/PGMD3	27	PA5/PGMRDY	39	TMS
4	AD5	16	PA14/PGMD2	28	PA4/PGMNCMD	40	TCK
5	AD6	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	AD7	18	VDDCORE	30	TST	42	ERASE
7	VDDIN	19	PA12/PGMD0	31	PA3	43	VDDFLASH
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	GND
9	PA17/PGMD5/AD0	21	PA10/PGMM2	33	VDDIO	45	XOUT
10	PA18/PGMD6/AD1	22	PA9/PGMM1	34	GND	46	XIN/PGMCK
11	PA19/PGMD7/AD2	23	PA8/PGMM0	35	PA1/PGMEN1	47	PLLRC
12	PA20/AD3	24	PA7/PGMNVALID	36	PA0/PGMEN0	48	VDDPLL

Note: 1. The bottom pad of the QFN package must be connected to ground.

Figure 5-1. 3.3V System Single Power Supply Schematic

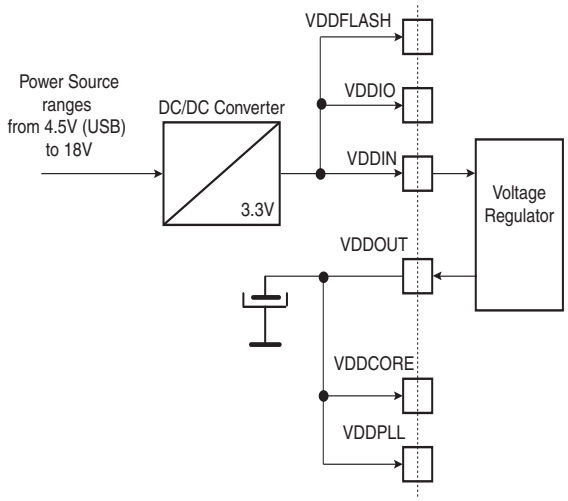
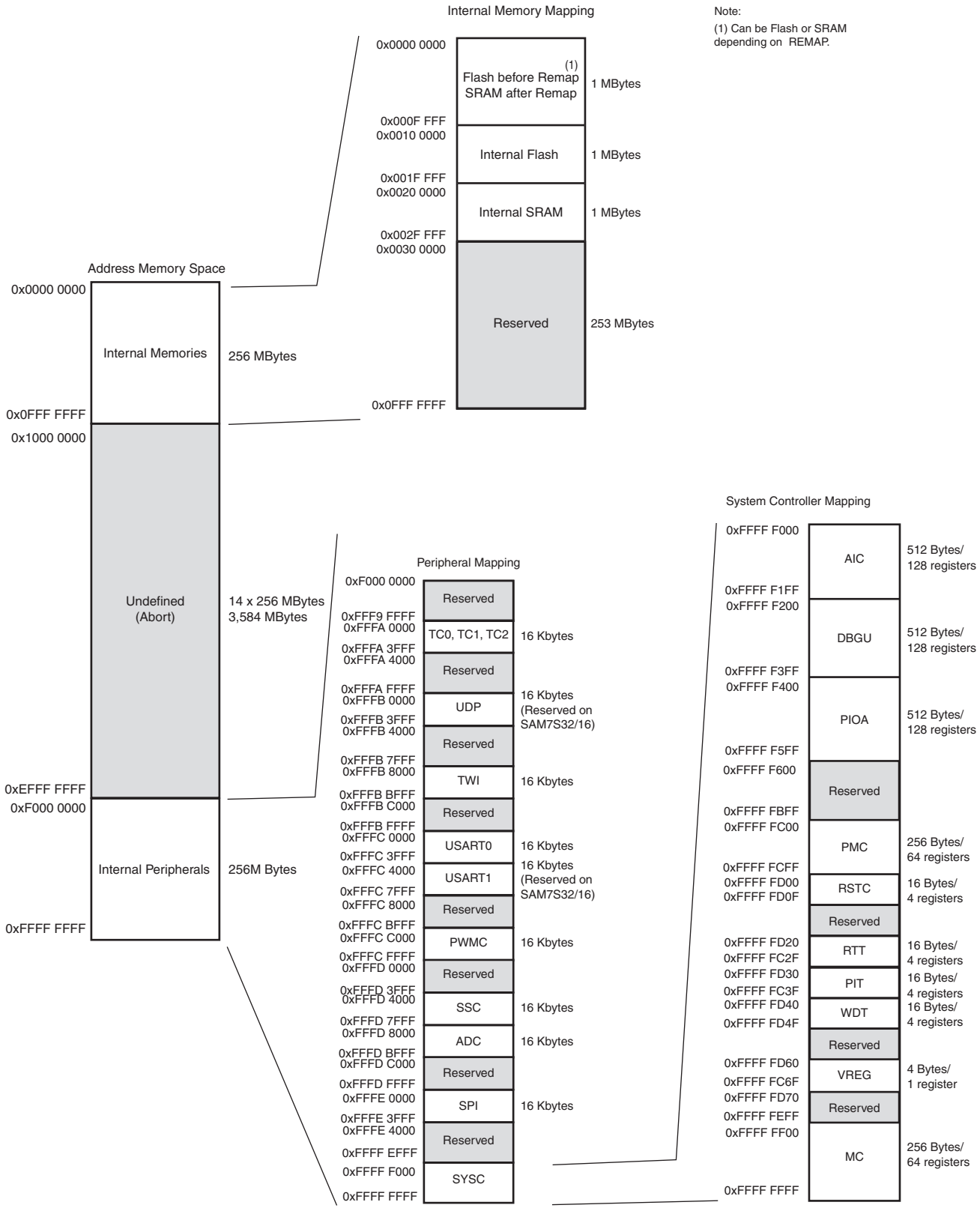


Figure 8-1. SAM SAM7S512/256/128/64/321/32/161/16 Memory Mapping



8.8.3 Lock Regions

8.8.3.1 SAM7S512

Two Embedded Flash Controllers each manage 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S512 contains 32 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 16 NVM bits (or 32 NVM bits) are software programmable through the corresponding EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.2 SAM7S256

The Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S256 contains 16 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 16 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.3 SAM7S128

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S128 contains 8 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 8 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.4 SAM7S64

The Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S64 contains 16 lock regions and each lock region contains 32 pages of 128 bytes. Each lock region has a size of 4 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 16 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.5 SAM7S321/32

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S321/32 contains 8 lock regions and each lock region contains 32 pages of 128 bytes. Each lock region has a size of 4 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

8.8.6 Calibration Bits

Eight NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

8.9 Fast Flash Programming Interface

The Fast Flash Programming Interface allows programming the device through either a serial JTAG interface or through a multiplexed fully-handshaked parallel port. It allows gang-programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when the TST pin and the PA0 and PA1 pins are all tied high and PA2 is tied low.

8.10 SAM-BA Boot Assistant

The SAM-BA® Boot Recovery restores the SAM-BA Boot in the first two sectors of the on-chip Flash memory. The SAM-BA Boot recovery is performed when the TST pin and the PA0, PA1 and PA2 pins are all tied high for 10 seconds. Then, a power cycle of the board is mandatory.

The SAM-BA Boot Assistant is a default Boot Program that provides an easy way to program in situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication through the DBGU or through the USB Device Port. (The SAM7S32/16 have no USB Device Port.)

- Communication through the DBGU supports a wide range of crystals from 3 to 20 MHz via software auto-detection.
- Communication through the USB Device Port is limited to an 18.432 MHz crystal. (

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

9. System Controller

The System Controller manages all vital blocks of the microcontroller: interrupts, clocks, power, time, debug and reset.

The System Controller peripherals are all mapped to the highest 4 Kbytes of address space, between addresses 0xFFFF F000 and 0xFFFF FFFF.

Figure 9-1 on page 26 and Figure 9-2 on page 27 show the product specific System Controller Block Diagrams.

Figure 8-1 on page 20 shows the mapping of the of the User Interface of the System Controller peripherals. Note that the memory controller configuration user interface is also mapped within this address space.

9.1 Reset Controller

The Reset Controller is based on a power-on reset cell and one brownout detector. It gives the status of the last reset, indicating whether it is a power-up reset, a software reset, a user reset, a watchdog reset or a brownout reset. In addition, it controls the internal resets and the NRST pin open-drain output. It allows to shape a signal on the NRST line, guaranteeing that the length of the pulse meets any requirement.

Note that if NRST is used as a reset output signal for external devices during power-off, the brownout detector must be activated.

9.1.1 Brownout Detector and Power-on Reset

The SAM7S Series embeds a brownout detection circuit and a power-on reset cell. Both are supplied with and monitor VDDCORE. Both signals are provided to the Flash to prevent any code corruption during power-up or power-down sequences or if brownouts occur on the VDDCORE power supply.

The power-on reset cell has a limited-accuracy threshold at around 1.5V. Its output remains low during power-up until VDDCORE goes over this voltage level. This signal goes to the reset controller and allows a full re-initialization of the device.

The brownout detector monitors the VDDCORE level during operation by comparing it to a fixed trigger level. It secures system operations in the most difficult environments and prevents code corruption in case of brownout on the VDDCORE.

Only VDDCORE is monitored.

When the brownout detector is enabled and VDDCORE decreases to a value below the trigger level (Vbot-, defined as Vbot - hyst/2), the brownout output is immediately activated.

When VDDCORE increases above the trigger level (Vbot+, defined as Vbot + hyst/2), the reset is released. The brownout detector only detects a drop if the voltage on VDDCORE stays below the threshold voltage for longer than about 1µs.

The threshold voltage has a hysteresis of about 50 mV, to ensure spike free brownout detection. The typical value of the brownout detector threshold is 1.68V with an accuracy of ± 2% and is factory calibrated.

The brownout detector is low-power, as it consumes less than 20 µA static current. However, it can be deactivated to save its static current. In this case, it consumes less than 1µA. The deactivation is configured through the GPNVM bit 0 of the Flash.

- One set of Chip ID Registers
- One Interface providing ICE Access Prevention

- Two-pin UART
  - Implemented features are compatible with the USART
  - Programmable Baud Rate Generator
  - Parity, Framing and Overrun Error
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
- Debug Communication Channel Support
  - Offers visibility of COMMRX and COMMTX signals from the ARM Processor
- Chip ID Registers
  - Identification of the device revision, sizes of the embedded memories, set of peripherals
  - Chip ID is 0x270B0A40 for AT91SAM7S512 Rev A
  - Chip ID is 0x270B0A4F for AT91SAM7S512 Rev B
  - Chip ID is 0x270D0940 for AT91SAM7S256 Rev A
  - Chip ID is 0x270B0941 for AT91SAM7S256 Rev B
  - Chip ID is 0x270B0942 for AT91SAM7S256 Rev C
  - Chip ID is TBD for AT91SAM7S256 Rev D
  - Chip ID is 0x270C0740 for AT91SAM7S128 Rev A
  - Chip ID is 0x270A0741 for AT91SAM7S128 Rev B
  - Chip ID is 0x270A0742 for AT91SAM7S128 Rev C
  - Chip ID is TBD for AT91SAM7S128 Rev D
  - Chip ID is 0x27090540 for AT91SAM7S64 Rev A
  - Chip ID is 0x27090543 for AT91SAM7S64 Rev B
  - Chip ID is 0x27090544 for AT91SAM7S64 Rev C
  - Chip ID is 0x27080342 for AT91SAM7S321 Rev A
  - Chip ID is 0x27080340 for AT91SAM7S32 Rev A
  - Chip ID is 0x27080341 for AT91SAM7S32 Rev B
  - Chip ID is 0x27050241 for AT9SAM7S161 Rev A
  - Chip ID is 0x27050240 for AT91SAM7S16 Rev A

Note: Refer to the errata section of the datasheet for updates on chip ID.

9.6 Periodic Interval Timer

- 20-bit programmable counter plus 12-bit interval counter

9.7 Watchdog Timer

- 12-bit key-protected Programmable Counter running on prescaled SCLK
- Provides reset or interrupt signals to the system
- Counter may be stopped while the processor is in debug state or in idle mode

9.8 Real-time Timer

- 32-bit free-running counter with alarm running on prescaled SCLK
- Programmable 16-bit prescaler for SLCK accuracy compensation

Table 11-4. 64-pad QFN Package Dimensions (in mm)

Symbol						
A	–	–	090	–	–	0.035
A1	–	–	0.05	–	–	0.001
A2	–	0.65	0.70	–	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.23	0.25	0.28	0.009	0.010	0.011
D	9.00 bsc			0.354 bsc		
D2	6.95	7.10	7.25	0.274	0.280	0.285
E	9.00 bsc			0.354 bsc		
E2	6.95	7.10	7.25	0.274	0.280	0.285
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 bsc			0.020 bsc		
R	0.125	–	–	0.0005	–	–
Tolerances of Form and Position						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

Revision History

6175AS	First issue - Unqualified on Intranet Corresponds to 6175A full datasheet approval loop. Qualified on Intranet.	
6175BS	Section 8. “Memories” on page 18 updated: 2 ms => 3 ms, 10 ms => 15 ms, 4 ms => 6 ms	CSR05-529
6175CS	Section 12. ”SAM7S Ordering Information” AT91SAM7S321 changed in Table 12-1 on page 47	#2342
6175DS	“Features” , Table 1-1, “Configuration Summary,” on page 3, Section 4. ”Package and Pinout” Section 12. ”SAM7S Ordering Information” QFN package information added	#2444
6175ES	Section 10.11 on page 39 USB Device port, Ping-pong Mode includes Isochronous endpoints. “Features” on page 1, and global: AT91SAM7S512 added to series. Reference to Manchester Encoder removed from USART. Section 8. ”Memories” Reformatted Memories, Consolidated Memory Mapping in Figure 8-1 on page 20 Section 10. ”Peripherals” Reordered sub sections. Section 11. ”Package Drawings” QFN, LQFP package drawings added. “ice_nreset” signals changed to” power_on_reset” in System Controller block diagrams, Figure 9-1 on page 26 and Figure 9-2 on page 27. Section 4. ”Package and Pinout” LQFP and QFN Package Outlines replace Mechanical Overview. Section 10.1 ”User Interface”, User peripherals are mapped between 0xF000 0000 and 0xFFFF EFFF. SYSIRQ changed to SYSC in “Peripheral Identifiers” Table 10-1 and Table 10-2	specs #2748 #2832 (DBGU IP) rfo review
6175FS	AT91SAM7S161 and AT91SAM7S16 added to product family **Features:** Timer Counter, on page 2 product specific information rewritten, Table 1-1, “Configuration Summary,” on page 3, footnote explains TC on AT91SAM7S32/16 has only two channels accessible via PIO, and in Section 10.9 ”Timer Counter”, precisions added to “compare and capture” output/input. Section 10.6 ”Two-wire Interface”, updated reference to I^2C compatibility, internal address registers, slave addressing, Modes for AT91SAM7S161/16 “One Two-wire Interface (TWI)” on page 2, updated in Features Section 10.12 ”Analog-to-digital Converter”, updated Successive Approximation Register ADC and the INL, DNL ± values of LSB. Section 8.8.3 ”Lock Regions”, locked-region’s erase or program command updated Section 9.5 ”Debug Unit”, Chip ID updated. Section 6. ”I/O Lines Considerations”, JTAG Port Pin, Test Pin, Erase Pin, updated.	BDs 4208 rfo review 4325 5063

6175GS	“Features” ,“Debug Unit (DBGU)” updated with “Mode for General Purpose 2-wire UART Serial Communication” Section 7.4 ”Peripheral DMA Controller”, added list of PDC priorities. Section 9. ”System Controller”, Figure 9-1 and Figure 9-2 RTT is reset by “power_on_reset”. Section 9.1.1 ”Brownout Detector and Power-on Reset”, fourth paragraph reduced. Section 9.5 ”Debug Unit”, the list; Section I ”Chip ID Registers”, chip IDs updated, added SAM7S32 Rev B and SAM7S64 Rev B to the list. Section 12. ”SAM7S Ordering Information”, Updated product ordering information by MRL A and MRL B versions.	5846 5913 5224 5685 rfo
6175HS	Section 6.2 ”Test Pin”, added to SAM-BA Boot recovery procedure, a power cycle of the board is mandatory. Section 8.10 ”SAM-BA Boot Assistant”, added to SAM-BA Boot recovery procedure, a power cycle of the board is mandatory.	6068
6175IS	Section 9.5 ”Debug Unit”, Chip ID Registers list updated. MRL C column added to Table 12-1, “SAM7S Series Ordering Information”.	7185
6175JS	Product Series Naming Convention Except for part ordering and library references, AT91 prefix dropped from most nomenclature. AT91SAM7S becomes SAM7S. Debug Unit: “Chip ID Registers” on page 31, Chip ID is 0x270B0A4F for AT91SAM7S512 Rev B	rfo 7945
6175KS	Section 9.5 ”Debug Unit”, Chip ID Registers list updated. Added Chip ID for SAM7S128 Rev D and SAM7S256 Rev D Table 12-1, “SAM7S Series Ordering Information”.Added SAM7S128 Rev D and SAM7S256 Rev D	8380/8467

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