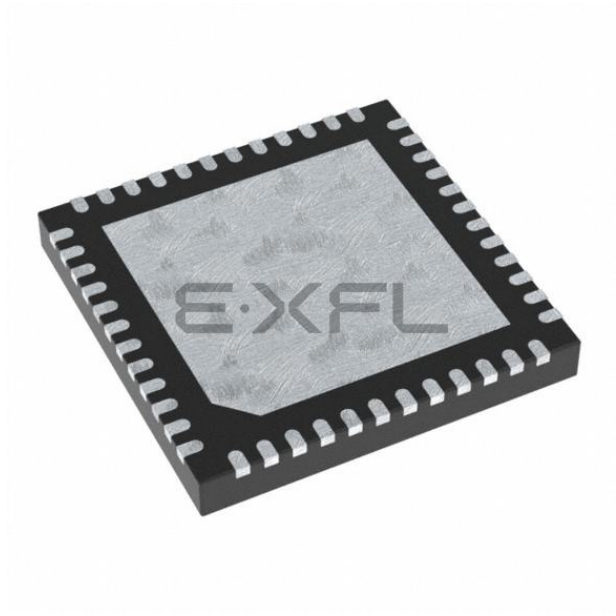

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	I²C, SPI, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam7s32-mu-999

Table 3-1. Signal Description List (Continued)

TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		
AD0-AD3	Analog Inputs	Analog		Digital pulled-up inputs at reset
AD4-AD7	Analog Inputs	Analog		Analog Inputs
ADTRG	ADC Trigger	Input		
ADVREF	ADC Reference	Analog		
PGMEN0-PGMEN2	Programming Enabling	Input		
PGMM0-PGMM3	Programming Mode	Input		
PGMD0-PGMD15	Programming Data	I/O		PGMD0-PGMD7 only on SAM7S32/16
PGMRDY	Programming Ready	Output	High	
PGMNVALID	Data Direction	Output	Low	
PGMNOE	Programming Read	Input	Low	
PGMCK	Programming Clock	Input		
PGMNCMD	Programming Command	Input	Low	

Note: 1. Refer to Section 6. “I/O Lines Considerations” on page 14.

4. Package and Pinout

The SAM7S512/256/128/64/321 are available in a 64-lead LQFP or 64-pad QFN package.

The SAM7S161 is available in a 64-Lead LQFP package.

The SAM7S32/16 are available in a 48-lead LQFP or 48-pad QFN package.

4.1 64-lead LQFP and 64-pad QFN Package Outlines

Figure 4-1 and Figure 4-2 show the orientation of the 64-lead LQFP and the 64-pad QFN package. A detailed mechanical description is given in the section Mechanical Characteristics of the full datasheet.

Figure 4-1. 64-lead LQFP Package (Top View)

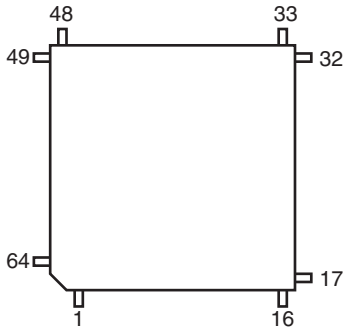
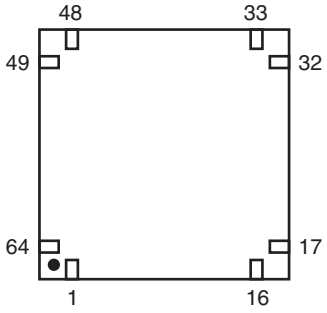


Figure 4-2. 64-pad QFN Package (Top View)



4.2 64-lead LQFP and 64-pad QFN Pinout

Table 4-1. SAM7S512/256/128/64/321/161 Pinout[1]

1	ADVREF	17	GND	33	TDI	49	TDO
2	GND	18	VDDIO	34	PA6/PGMNOE	50	JTAGSEL
3	AD4	19	PA16/PGMD4	35	PA5/PGMRDY	51	TMS
4	AD5	20	PA15/PGMD3	36	PA4/PGMNCMD	52	PA31
5	AD6	21	PA14/PGMD2	37	PA27/PGMD15	53	TCK
6	AD7	22	PA13/PGMD1	38	PA28	54	VDDCORE
7	VDDIN	23	PA24/PGMD12	39	NRST	55	ERASE
8	VDDOUT	24	VDDCORE	40	TST	56	DDM
9	PA17/PGMD5/AD0	25	PA25/PGMD13	41	PA29	57	DDP
10	PA18/PGMD6/AD1	26	PA26/PGMD14	42	PA30	58	VDDIO
11	PA21/PGMD9	27	PA12/PGMD0	43	PA3	59	VDDFLASH
12	VDDCORE	28	PA11/PGMM3	44	PA2/PGMEN2	60	GND
13	PA19/PGMD7/AD2	29	PA10/PGMM2	45	VDDIO	61	XOUT
14	PA22/PGMD10	30	PA9/PGMM1	46	GND	62	XIN/PGMCK
15	PA23/PGMD11	31	PA8/PGMM0	47	PA1/PGMEN1	63	PLLRC
16	PA20/PGMD8/AD3	32	PA7/PGMNVALID	48	PA0/PGMEN0	64	VDDPLL

Note: 1. The bottom pad of the QFN package must be connected to ground.

4.3 48-lead LQFP and 48-pad QFN Package Outlines

Figure 4-3 and Figure 4-4 show the orientation of the 48-lead LQFP and the 48-pad QFN package. A detailed mechanical description is given in the section Mechanical Characteristics of the full datasheet.

Figure 4-3. 48-lead LQFP Package (Top View)

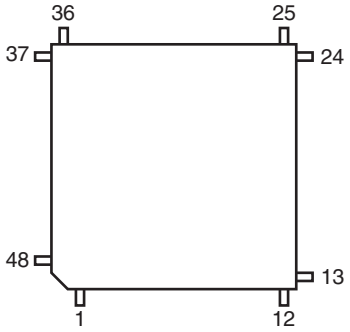
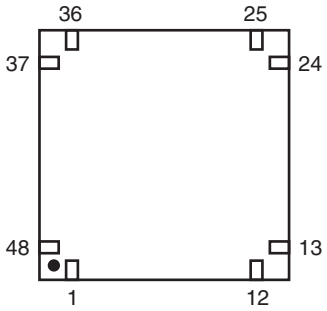


Figure 4-4. 48-pad QFN Package (Top View)



4.4 48-lead LQFP and 48-pad QFN Pinout

Table 4-2. SAM7S32/16 Pinout[1]

1	ADVREF	13	VDDIO	25	TDI	37	TDO
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	AD4	15	PA15/PGMD3	27	PA5/PGMRDY	39	TMS
4	AD5	16	PA14/PGMD2	28	PA4/PGMNCMD	40	TCK
5	AD6	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	AD7	18	VDDCORE	30	TST	42	ERASE
7	VDDIN	19	PA12/PGMD0	31	PA3	43	VDDFLASH
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	GND
9	PA17/PGMD5/AD0	21	PA10/PGMM2	33	VDDIO	45	XOUT
10	PA18/PGMD6/AD1	22	PA9/PGMM1	34	GND	46	XIN/PGMCK
11	PA19/PGMD7/AD2	23	PA8/PGMM0	35	PA1/PGMEN1	47	PLLRC
12	PA20/AD3	24	PA7/PGMNVALID	36	PA0/PGMEN0	48	VDDPLL

Note: 1. The bottom pad of the QFN package must be connected to ground.

5. Power Considerations

5.1 Power Supplies

The SAM7S Series has six types of power supply pins and integrates a voltage regulator, allowing the device to be supplied with only one voltage. The six power supply pin types are:

- VDDIN pin. It powers the voltage regulator and the ADC; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDOUT pin. It is the output of the 1.8V voltage regulator.
- VDDIO pin. It powers the I/O lines and the USB transceivers; dual voltage range is supported. Ranges from 3.0V to 3.6V, 3.3V nominal or from 1.65V to 1.95V, 1.8V nominal. Note that supplying less than 3.0V to VDDIO prevents any use of the USB transceivers.
- VDDFLASH pin. It powers a part of the Flash and is required for the Flash to operate correctly; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDCORE pins. They power the logic of the device; voltage ranges from 1.65V to 1.95V, 1.8V typical. It can be connected to the VDDOUT pin with decoupling capacitor. VDDCORE is required for the device, including its embedded Flash, to operate correctly.

During startup, core supply voltage (VDDCORE) slope must be superior or equal to 6V/ms.

- VDDPLL pin. It powers the oscillator and the PLL. It can be connected directly to the VDDOUT pin.

No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

In order to decrease current consumption, if the voltage regulator and the ADC are not used, VDDIN, ADVREF, AD4, AD5, AD6 and AD7 should be connected to GND. In this case VDDOUT should be left unconnected.

5.2 Power Consumption

The SAM7S Series has a static current of less than 60 µA on VDDCORE at 25°C, including the RC oscillator, the voltage regulator and the power-on reset. When the brown-out detector is activated, 20 µA static current is added.

The dynamic power consumption on VDDCORE is less than 50 mA at full speed when running out of the Flash. Under the same conditions, the power consumption on VDDFLASH does not exceed 10 mA.

5.3 Voltage Regulator

The SAM7S Series embeds a voltage regulator that is managed by the System Controller.

In Normal Mode, the voltage regulator consumes less than 100 µA static current and draws 100 mA of output current.

The voltage regulator also has a Low-power Mode. In this mode, it consumes less than 25 µA static current and draws 1 mA of output current.

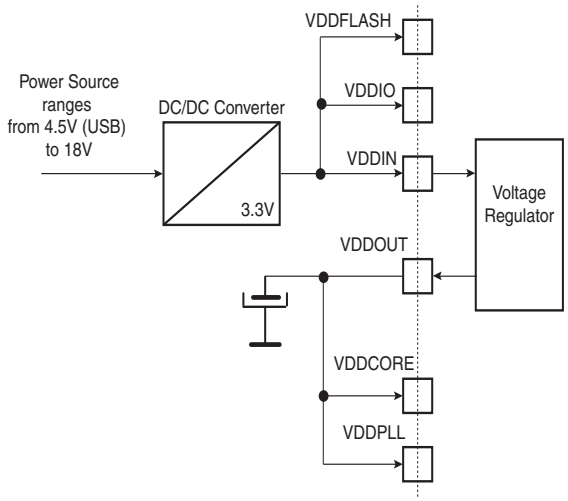
Adequate output supply decoupling is mandatory for VDDOUT to reduce ripple and avoid oscillations. The best way to achieve this is to use two capacitors in parallel: one external 470 pF (or 1 nF) NPO capacitor must be connected between VDDOUT and GND as close to the chip as possible. One external 2.2 µF (or 3.3 µF) X7R capacitor must be connected between VDDOUT and GND.

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop. The input decoupling capacitor should be placed close to the chip. For example, two capacitors can be used in parallel: 100 nF NPO and 4.7 µF X7R.

5.4 Typical Powering Schematics

The SAM7S Series supports a 3.3V single supply mode. The internal regulator is connected to the 3.3V source and its output feeds VDDCORE and the VDDPLL. Figure 5-1 shows the power schematics to be used for USB bus-powered systems.

Figure 5-1. 3.3V System Single Power Supply Schematic



6. I/O Lines Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are schmitt trigger inputs. TMS and TCK are 5-V tolerant, TDI is not. TMS, TDI and TCK do not integrate a pull-up resistor.

TDO is an output, driven at up to VDDIO, and has no pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. The JTAGSEL pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

6.2 Test Pin

The TST pin is used for manufacturing test, fast programming mode or SAM-BA Boot Recovery of the SAM7S Series when asserted high. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

To enter fast programming mode, the TST pin and the PA0 and PA1 pins should be tied high and PA2 tied to low.

To enter SAM-BA Boot Recovery, the TST pin and the PA0, PA1 and PA2 pins should be tied high for at least 10 seconds. Then a power cycle of the board is mandatory.

Driving the TST pin at a high level while PA0 or PA1 is driven at 0 leads to unpredictable results.

6.3 Reset Pin

The NRST pin is bidirectional with an open drain output buffer. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. There is no constraint on the length of the reset pulse, and the reset controller can guarantee a minimum pulse length. This allows connection of a simple push-button on the pin NRST as system user reset, and the use of the signal NRST to reset all the components of the system.

The NRST pin integrates a permanent pull-up resistor to VDDIO.

6.4 ERASE Pin

The ERASE pin is used to re-initialize the Flash content and some of its NVM bits. It integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

6.5 PIO Controller A Lines

- All the I/O lines PA0 to PA31on SAM7S512/256/128/64/321 (PA0 to PA20 on SAM7S32) are 5V-tolerant and all integrate a programmable pull-up resistor.
- All the I/O lines PA0 to PA31 on SAM7S161 (PA0 to PA20 on SAM7S16) are **not** 5V-tolerant and all integrate a programmable pull-up resistor.

Programming of this pull-up resistor is performed independently for each I/O line through the PIO controllers.

5V-tolerant means that the I/O lines can drive voltage level according to VDDIO, but can be driven with a voltage of up to 5.5V. However, driving an I/O line with a voltage over VDDIO while the programmable pull-up resistor is enabled will create a current path through the pull-up resistor from the I/O line to VDDIO. Care should be taken, in particular at reset, as all the I/O lines default to input with the pull-up resistor enabled at reset.

6.6 I/O Line Drive Levels

The PIO lines PA0 to PA3 are high-drive current capable. Each of these I/O lines can drive up to 16 mA permanently.

The remaining I/O lines can draw only 8 mA.

However, the total current drawn by all the I/O lines cannot exceed 150 mA (100 mA for SAM7S32/16).

- Fast access time, 30 MHz single-cycle access in Worst Case conditions
- Page programming time: 6 ms, including page auto-erase
- Page programming without auto-erase: 3 ms
- Full chip erase time: 15 ms
- 10,000 write cycles, 10-year data retention capability
- 16 lock bits, protecting 16 sectors of 32 pages
- Protection Mode to secure contents of the Flash

- 16 Kbytes of Fast SRAM
  - Single-cycle access at full speed

8.5 SAM7S321/32

- 32 Kbytes of Flash Memory, single plane
  - 256 pages of 128 bytes
  - Fast access time, 30 MHz single-cycle access in Worst Case conditions
  - Page programming time: 6 ms, including page auto-erase
  - Page programming without auto-erase: 3 ms
  - Full chip erase time: 15 ms
  - 10,000 write cycles, 10-year data retention capability
  - 8 lock bits, protecting 8 sectors of 32 pages
  - Protection Mode to secure contents of the Flash
- 8 Kbytes of Fast SRAM
  - Single-cycle access at full speed

8.6 SAM7S161/16

- 16 Kbytes of Flash Memory, single plane
  - 256 pages of 64 bytes
  - Fast access time, 30 MHz single-cycle access in Worst Case conditions
  - Page programming time: 6 ms, including page auto-erase
  - Page programming without auto-erase: 3 ms
  - Full chip erase time: 15 ms
  - 10,000 write cycles, 10-year data retention capability
  - 8 lock bits, protecting 8 sectors of 32 pages
  - Protection Mode to secure contents of the Flash
- 4 Kbytes of Fast SRAM
  - Single-cycle access at full speed

8.8.3 Lock Regions

8.8.3.1 SAM7S512

Two Embedded Flash Controllers each manage 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S512 contains 32 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 16 NVM bits (or 32 NVM bits) are software programmable through the corresponding EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.2 SAM7S256

The Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S256 contains 16 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 16 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.3 SAM7S128

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S128 contains 8 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 8 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.4 SAM7S64

The Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S64 contains 16 lock regions and each lock region contains 32 pages of 128 bytes. Each lock region has a size of 4 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 16 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.5 SAM7S321/32

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S321/32 contains 8 lock regions and each lock region contains 32 pages of 128 bytes. Each lock region has a size of 4 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

Figure 9-1. System Controller Block Diagram (SAM7S512/256/128/64/321/161)

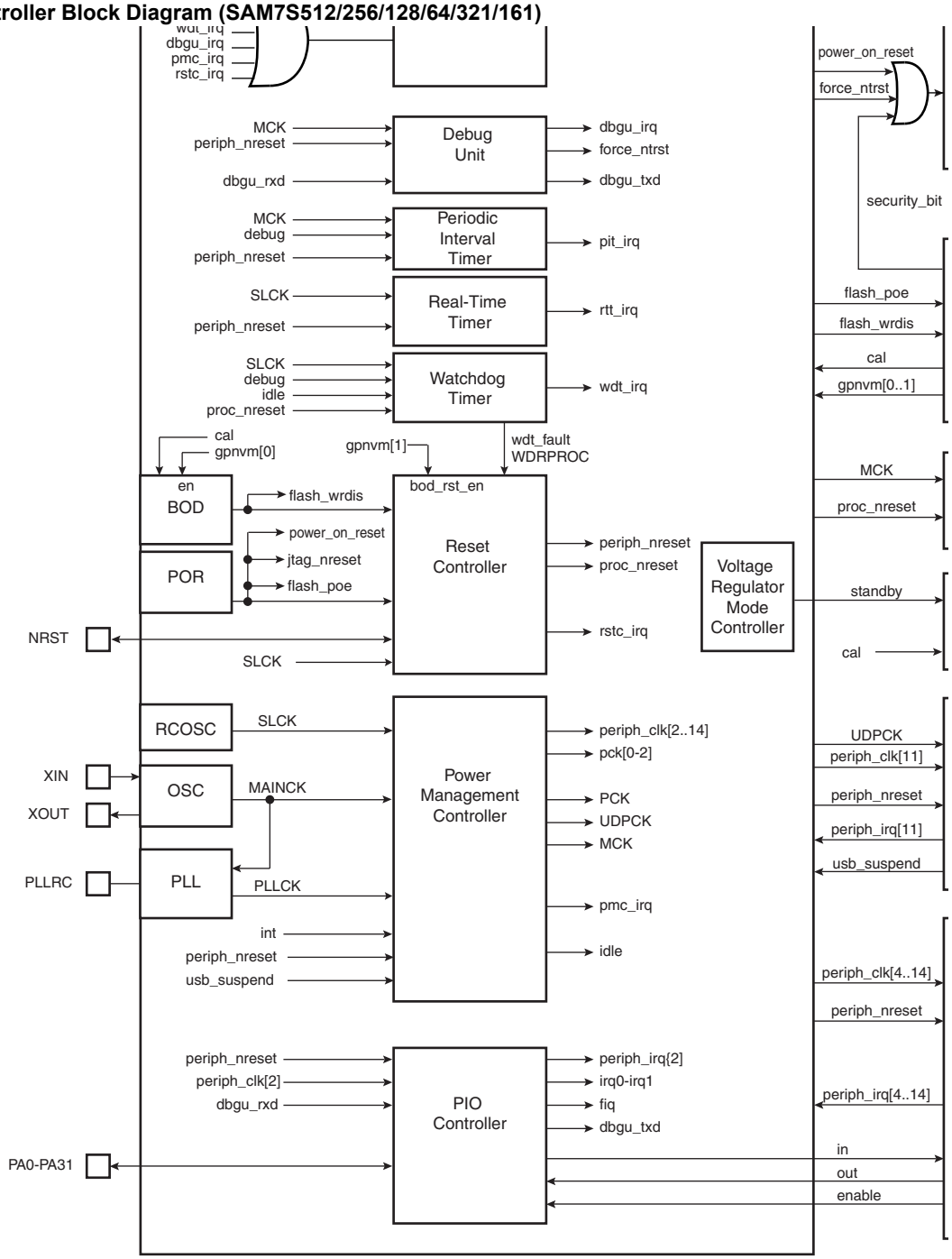
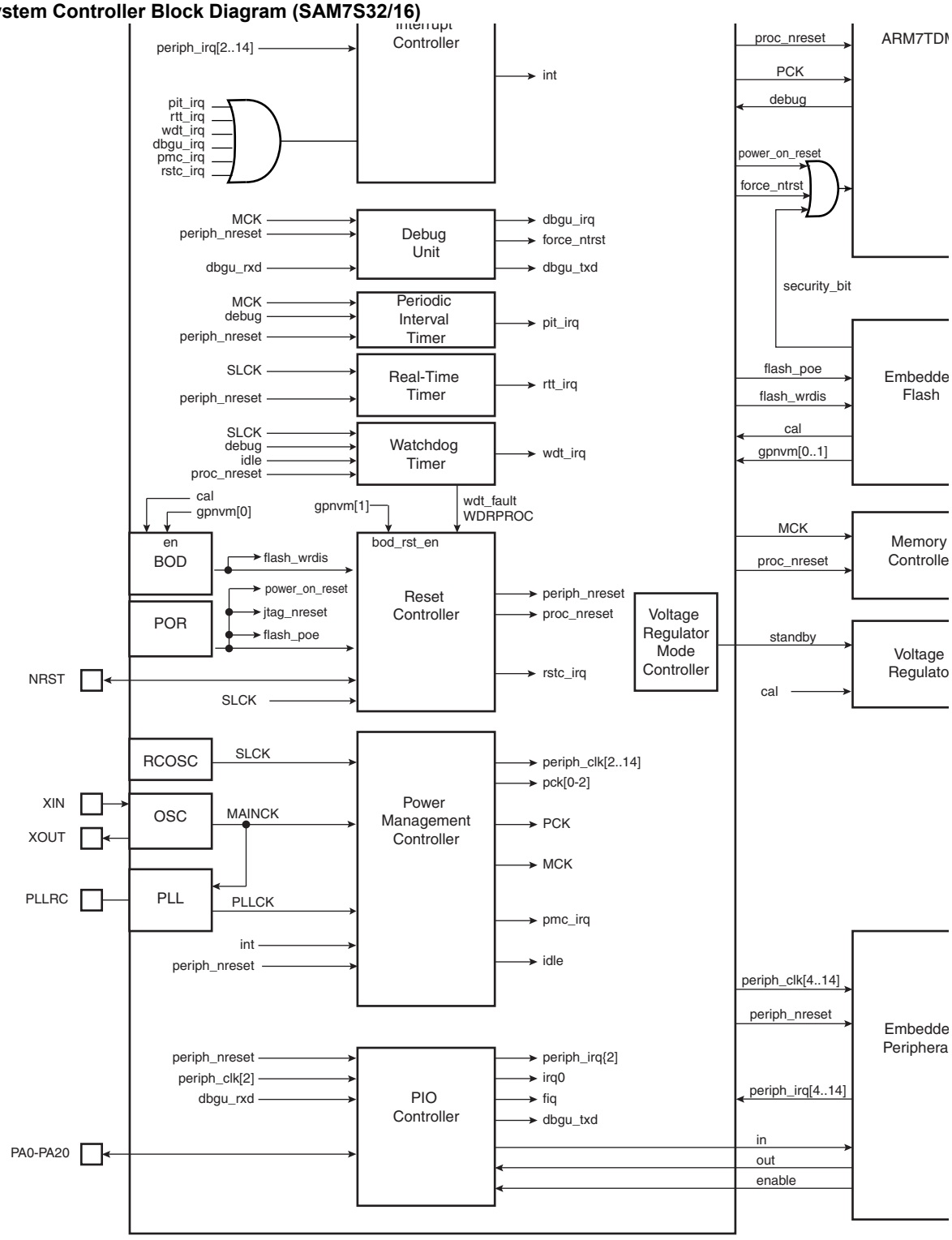


Figure 9-2. System Controller Block Diagram (SAM7S32/16)



10. Peripherals

10.1 User Interface

The User Peripherals are mapped in the 256 MBytes of address space between 0xF000 0000 and 0xFFFF EFFF. Each peripheral is allocated 16 Kbytes of address space.

A complete memory map is provided in Figure 8-1 on page 20.

10.2 Peripheral Identifiers

The SAM7S Series embeds a wide range of peripherals. Table 10-1 defines the Peripheral Identifiers of the SAM7S512/256/128/64/321/161. Table 10-2 defines the Peripheral Identifiers of the SAM7S32/16. A peripheral identifier is required for the control of the peripheral interrupt with the Advanced Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 10-1. Peripheral Identifiers (SAM7S512/256/128/64/321/161)

0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC[1]	System	
2	PIOA	Parallel I/O Controller A	
3	Reserved		
4	ADC[1]	Analog-to Digital Converter	
5	SPI	Serial Peripheral Interface	
6	US0	USART 0	
7	US1	USART 1	
8	SSC	Synchronous Serial Controller	
9	TWI	Two-wire Interface	
10	PWMC	PWM Controller	
11	UDP	USB Device Port	
12	TC0	Timer/Counter 0	
13	TC1	Timer/Counter 1	
14	TC2	Timer/Counter 2	
15 - 29	Reserved		
30	AIC	Advanced Interrupt Controller	IRQ0
31	AIC	Advanced Interrupt Controller	IRQ1

Note: 1. Setting SYSC and ADC bits in the clock set/clear registers of the PMC has no effect. The System Controller is continuously clocked. The ADC clock is automatically started for the first conversion. In Sleep Mode the ADC clock is automatically stopped after each conversion.

Note: 1. Setting SYSC and ADC bits in the clock set/clear registers of the PMC has no effect. The System Controller is continuously clocked. The ADC clock is automatically started for the first conversion. In Sleep Mode the ADC clock is automatically stopped after each conversion.

10.5 Serial Peripheral Interface

- Supports communication with external serial devices
  - Four chip selects with external decoder allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash® and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
  - Maximum frequency at up to Master Clock

10.6 Two-wire Interface

- Master Mode only (SAM7S512/256/128/64/321/32)
- Master, Multi-Master and Slave Mode support (SAM7S161/16)
- General Call supported in Slave Mode (SAM7S161/16)
- Compatibility with I^2C compatible devices (refer to the TWI sections of the datasheet)
- One, two or three bytes internal address registers for easy Serial Memory access
- 7-bit or 10-bit slave addressing
- Sequential read/write operations

10.7 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode
  - 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB or LSB first
  - Optional break generation and detection
  - By 8 or by 16 over-sampling receiver frequency
  - Hardware handshaking RTS - CTS
  - Modem Signals Management DTR-DSR-DCD-RI on USART1 (not present on SAM7S32/16)
  - Receiver time-out and transmitter timeguard
  - Multi-drop Mode with address generation and detection
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

11. Package Drawings

The SAM7S series devices are available in LQFP and QFN package types.

11.1 LQFP Packages

Figure 11-1. 48-and 64-lead LQFP Package Drawing

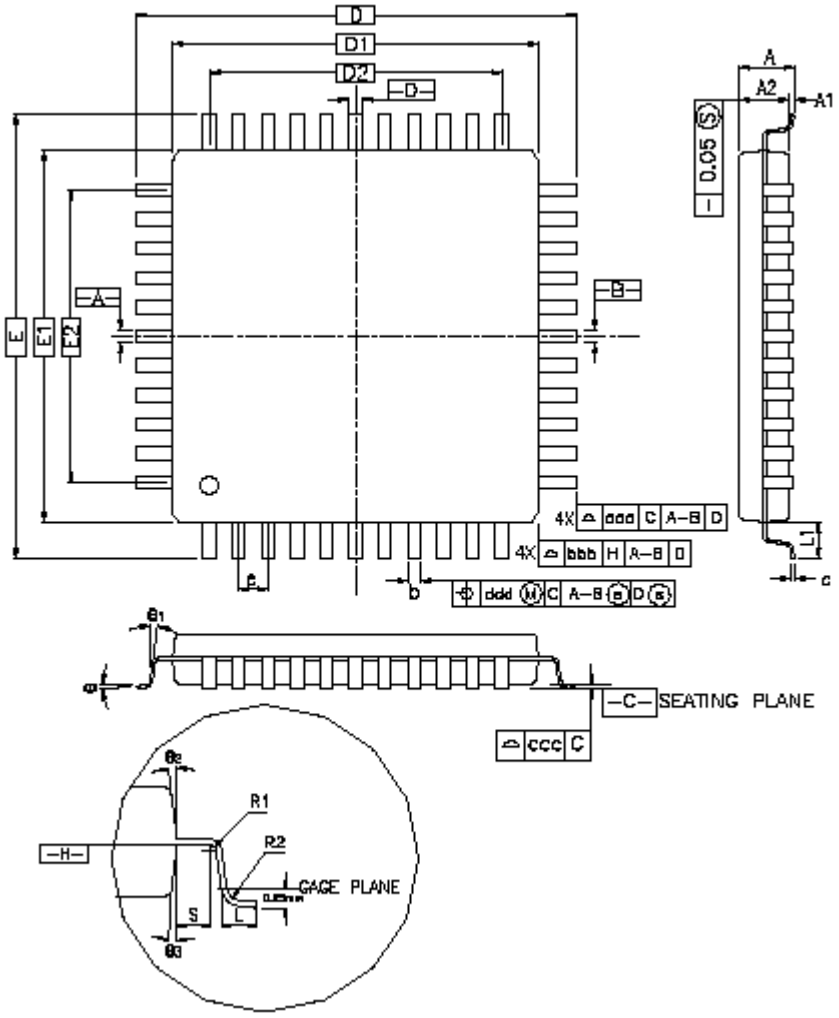


Table 11-2. 64-lead LQFP Package Dimensions (in mm)

Symbol						
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.383 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.383 BSC		
R2	0.08	–	0.20	0.003	–	0.008
R1	0.08	–	–	0.003	–	–
q	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	–	–	0°	–	–
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	7.50			0.285		
E2	7.50			0.285		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

11.2 QFN Packages

Figure 11-2. 48-pad QFN Package

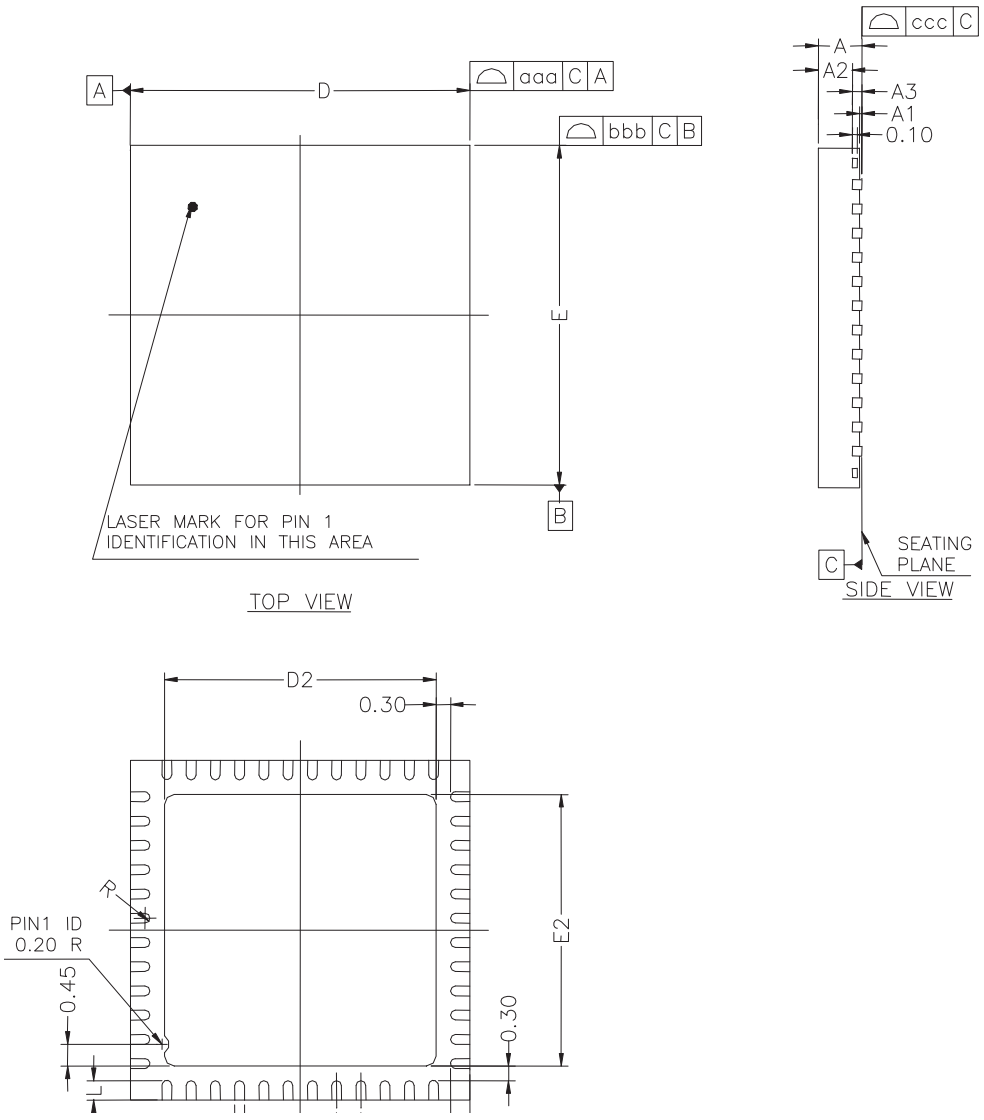


Figure 11-3. 64-pad QFN Package Drawing

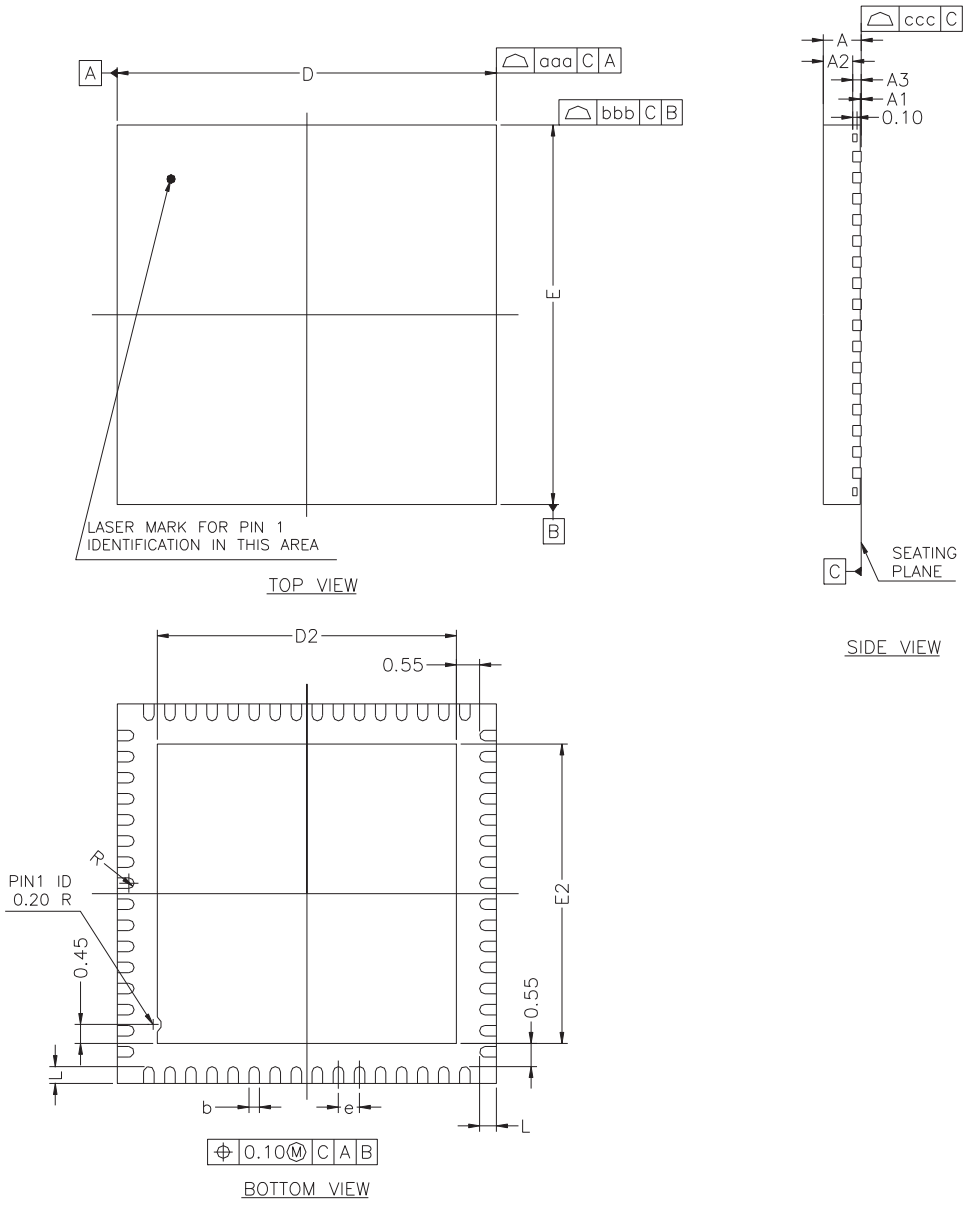


Table 11-4. 64-pad QFN Package Dimensions (in mm)

Symbol						
A	–	–	090	–	–	0.035
A1	–	–	0.05	–	–	0.001
A2	–	0.65	0.70	–	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.23	0.25	0.28	0.009	0.010	0.011
D	9.00 bsc			0.354 bsc		
D2	6.95	7.10	7.25	0.274	0.280	0.285
E	9.00 bsc			0.354 bsc		
E2	6.95	7.10	7.25	0.274	0.280	0.285
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 bsc			0.020 bsc		
R	0.125	–	–	0.0005	–	–
Tolerances of Form and Position						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

Revision History

6175AS	First issue - Unqualified on Intranet Corresponds to 6175A full datasheet approval loop. Qualified on Intranet.	
6175BS	Section 8. “Memories” on page 18 updated: 2 ms => 3 ms, 10 ms => 15 ms, 4 ms => 6 ms	CSR05-529
6175CS	Section 12. ”SAM7S Ordering Information” AT91SAM7S321 changed in Table 12-1 on page 47	#2342
6175DS	“Features” , Table 1-1, “Configuration Summary,” on page 3, Section 4. ”Package and Pinout” Section 12. ”SAM7S Ordering Information” QFN package information added	#2444
6175ES	Section 10.11 on page 39 USB Device port, Ping-pong Mode includes Isochronous endpoints. “Features” on page 1, and global: AT91SAM7S512 added to series. Reference to Manchester Encoder removed from USART. Section 8. ”Memories” Reformatted Memories, Consolidated Memory Mapping in Figure 8-1 on page 20 Section 10. ”Peripherals” Reordered sub sections. Section 11. ”Package Drawings” QFN, LQFP package drawings added. “ice_nreset” signals changed to” power_on_reset” in System Controller block diagrams, Figure 9-1 on page 26 and Figure 9-2 on page 27. Section 4. ”Package and Pinout” LQFP and QFN Package Outlines replace Mechanical Overview. Section 10.1 ”User Interface”, User peripherals are mapped between 0xF000 0000 and 0xFFFF EFFF. SYSIRQ changed to SYSC in “Peripheral Identifiers” Table 10-1 and Table 10-2	specs #2748 #2832 (DBGU IP) rfo review
6175FS	AT91SAM7S161 and AT91SAM7S16 added to product family **Features:** Timer Counter, on page 2 product specific information rewritten, Table 1-1, “Configuration Summary,” on page 3, footnote explains TC on AT91SAM7S32/16 has only two channels accessible via PIO, and in Section 10.9 ”Timer Counter”, precisions added to “compare and capture” output/input. Section 10.6 ”Two-wire Interface”, updated reference to I^2C compatibility, internal address registers, slave addressing, Modes for AT91SAM7S161/16 “One Two-wire Interface (TWI)” on page 2, updated in Features Section 10.12 ”Analog-to-digital Converter”, updated Successive Approximation Register ADC and the INL, DNL ± values of LSB. Section 8.8.3 ”Lock Regions”, locked-region’s erase or program command updated Section 9.5 ”Debug Unit”, Chip ID updated. Section 6. ”I/O Lines Considerations”, JTAG Port Pin, Test Pin, Erase Pin, updated.	BDs 4208 rfo review 4325 5063