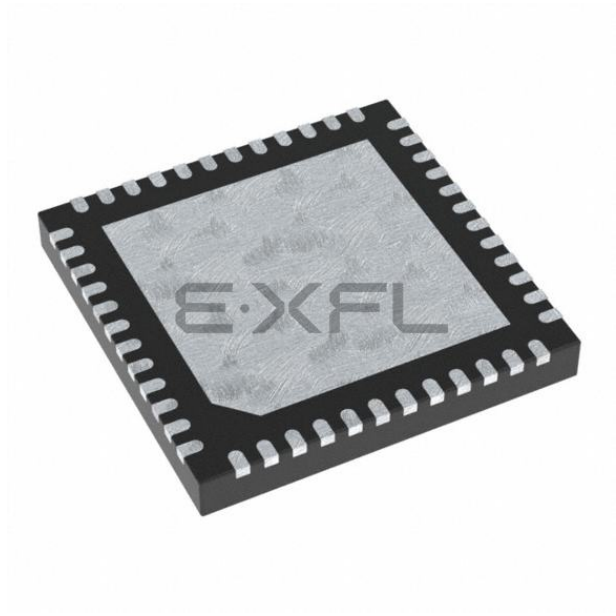

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	I²C, SPI, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam7s32-mu

- **Fully Static Operation: Up to 55 MHz at 1.65V and 85° C Worst Case Conditions**
- **Available in 64-lead LQFP Green or 64-pad QFN Green Package (SAM7S512/256/128/64/321/161) and 48-lead LQFP Green or 48-pad QFN Green Package (SAM7S32/16)**

1. Description

Atmel's SAM7S is a series of low pincount Flash microcontrollers based on the 32-bit ARM RISC processor. It features a high-speed Flash and an SRAM, a large set of peripherals, including a USB 2.0 device (except for the SAM7S32 and SAM7S16), and a complete set of system functions minimizing the number of external components. The device is an ideal migration path for 8-bit microcontroller users looking for additional performance and extended memory.

The embedded Flash memory can be programmed in-system via the JTAG-ICE interface or via a parallel interface on a production programmer prior to mounting. Built-in lock bits and a security bit protect the firmware from accidental overwrite and preserves its confidentiality.

The SAM7S Series system controller includes a reset controller capable of managing the power-on sequence of the microcontroller and the complete system. Correct device operation can be monitored by a built-in brownout detector and a watchdog running off an integrated RC oscillator.

The SAM7S Series are general-purpose microcontrollers. Their integrated USB Device port makes them ideal devices for peripheral applications requiring connectivity to a PC or cellular phone. Their aggressive price point and high level of integration pushes their scope of use far into the cost-sensitive, high-volume consumer market.

1.1 Configuration Summary of the SAM7S512, SAM7S256, SAM7S128, SAM7S64, SAM7S321, SAM7S32, SAM7S161 and SAM7S16

The SAM7S512, SAM7S256, SAM7S128, SAM7S64, SAM7S321, SAM7S32, SAM7S161 and SAM7S16 differ in memory size, peripheral set and package. Table 1-1 summarizes the configuration of the six devices.

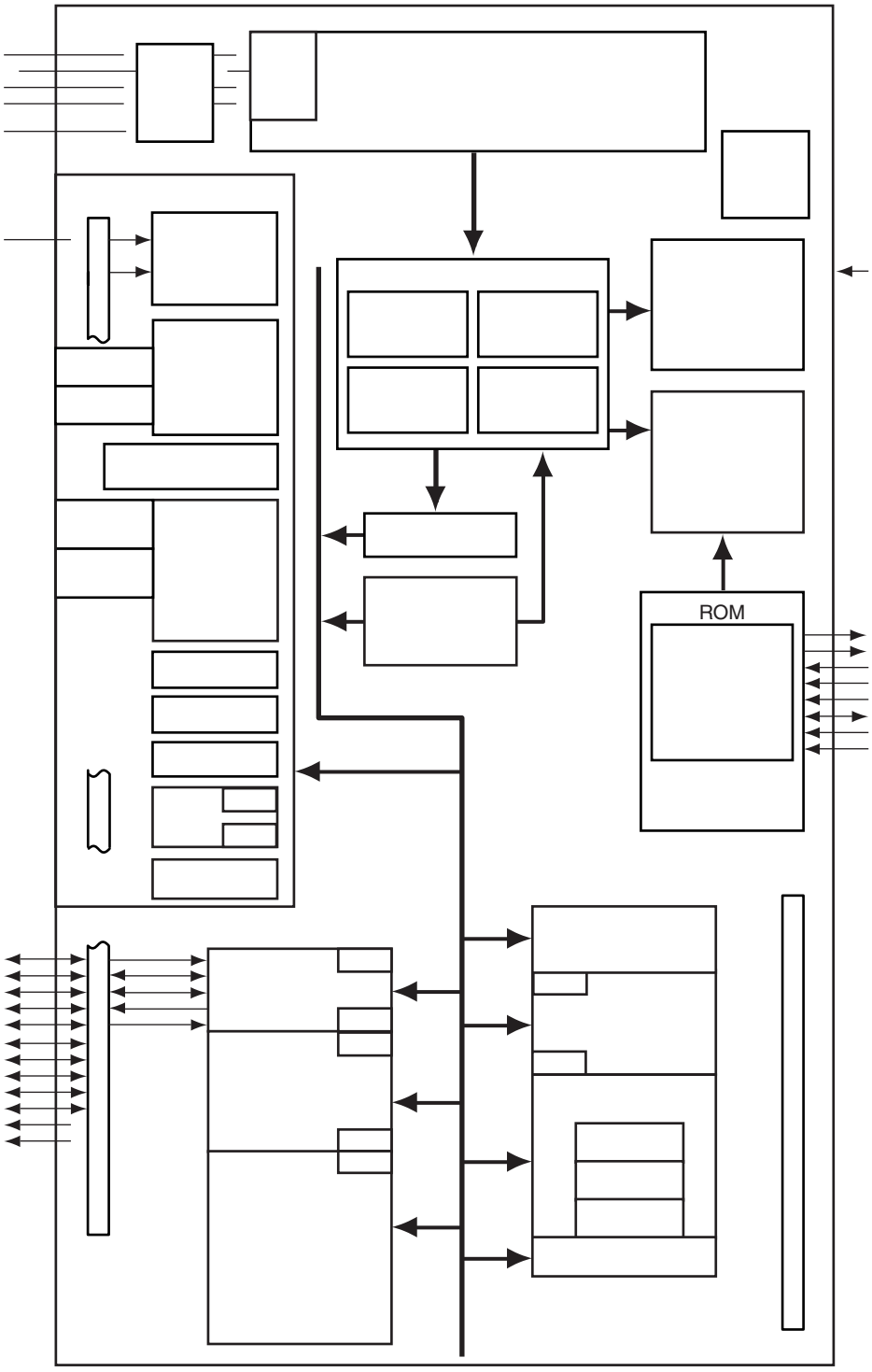
Except for the SAM7S32/16, all other SAM7S devices are package and pinout compatible.

Table 1-1. Configuration Summary

SAM7S512	512 Kbytes	Master	dual plane	64 Kbytes	1	2[1] [2]	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S256	256 Kbytes	Master	single plane	64 Kbytes	1	2[1]						

Notes: 1. Fractional Baud Rate.
2. Full modem line support on USART1.
3. Only two TC channels are accessible through the PIO.

Figure 2-2. SAM7S32/16 Block Diagram



3. Signal Description

Table 3-1. Signal Description List

VDDIN	Voltage and ADC Regulator Power Supply Input	Power		3.0 to 3.6V
VDDOUT	Voltage Regulator Output	Power		1.85V nominal
VDDFLASH	Flash Power Supply	Power		3.0V to 3.6V
VDDIO	I/O Lines Power Supply	Power		3.0V to 3.6V or 1.65V to 1.95V
VDDCORE	Core Power Supply	Power		1.65V to 1.95V
VDDPLL	PLL	Power		1.65V to 1.95V
GND	Ground	Ground		
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
PLLRC	PLL Filter	Input		
PCK0 - PCK2	Programmable Clock Output	Output		
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor
JTAGSEL	JTAG Selection	Input		Pull-down resistor(1)
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	Pull-down resistor(1)
NRST	Microcontroller Reset	I/O	Low	Open-drain with pull-Up resistor
TST	Test Mode Select	Input	High	Pull-down resistor(1)
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
IRQ0 - IRQ1	External Interrupt Inputs	Input		IRQ1 not present on SAM7S32/16
FIQ	Fast Interrupt Input	Input		
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset PA0 - PA20 only on SAM7S32/16

Table 3-1. Signal Description List (Continued)

TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		
AD0-AD3	Analog Inputs	Analog		Digital pulled-up inputs at reset
AD4-AD7	Analog Inputs	Analog		Analog Inputs
ADTRG	ADC Trigger	Input		
ADVREF	ADC Reference	Analog		
PGMEN0-PGMEN2	Programming Enabling	Input		
PGMM0-PGMM3	Programming Mode	Input		
PGMD0-PGMD15	Programming Data	I/O		PGMD0-PGMD7 only on SAM7S32/16
PGMRDY	Programming Ready	Output	High	
PGMNVALID	Data Direction	Output	Low	
PGMNOE	Programming Read	Input	Low	
PGMCK	Programming Clock	Input		
PGMNCMD	Programming Command	Input	Low	

Note: 1. Refer to Section 6. “I/O Lines Considerations” on page 14.

4.2 64-lead LQFP and 64-pad QFN Pinout

Table 4-1. SAM7S512/256/128/64/321/161 Pinout[1]

1	ADVREF	17	GND	33	TDI	49	TDO
2	GND	18	VDDIO	34	PA6/PGMNOE	50	JTAGSEL
3	AD4	19	PA16/PGMD4	35	PA5/PGMRDY	51	TMS
4	AD5	20	PA15/PGMD3	36	PA4/PGMNCMD	52	PA31
5	AD6	21	PA14/PGMD2	37	PA27/PGMD15	53	TCK
6	AD7	22	PA13/PGMD1	38	PA28	54	VDDCORE
7	VDDIN	23	PA24/PGMD12	39	NRST	55	ERASE
8	VDDOUT	24	VDDCORE	40	TST	56	DDM
9	PA17/PGMD5/AD0	25	PA25/PGMD13	41	PA29	57	DDP
10	PA18/PGMD6/AD1	26	PA26/PGMD14	42	PA30	58	VDDIO
11	PA21/PGMD9	27	PA12/PGMD0	43	PA3	59	VDDFLASH
12	VDDCORE	28	PA11/PGMM3	44	PA2/PGMEN2	60	GND
13	PA19/PGMD7/AD2	29	PA10/PGMM2	45	VDDIO	61	XOUT
14	PA22/PGMD10	30	PA9/PGMM1	46	GND	62	XIN/PGMCK
15	PA23/PGMD11	31	PA8/PGMM0	47	PA1/PGMEN1	63	PLLRC
16	PA20/PGMD8/AD3	32	PA7/PGMNVALID	48	PA0/PGMEN0	64	VDDPLL

Note: 1. The bottom pad of the QFN package must be connected to ground.

4.3 48-lead LQFP and 48-pad QFN Package Outlines

Figure 4-3 and Figure 4-4 show the orientation of the 48-lead LQFP and the 48-pad QFN package. A detailed mechanical description is given in the section Mechanical Characteristics of the full datasheet.

Figure 4-3. 48-lead LQFP Package (Top View)

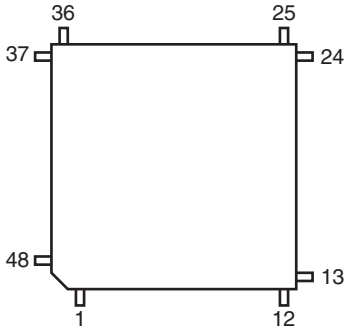
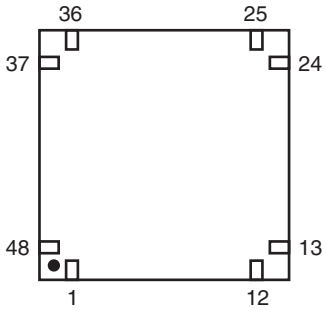


Figure 4-4. 48-pad QFN Package (Top View)



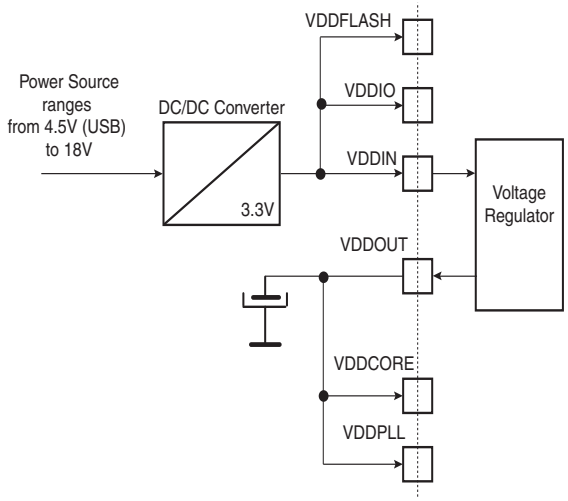
4.4 48-lead LQFP and 48-pad QFN Pinout

Table 4-2. SAM7S32/16 Pinout[1]

1	ADVREF	13	VDDIO	25	TDI	37	TDO
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	AD4	15	PA15/PGMD3	27	PA5/PGMRDY	39	TMS
4	AD5	16	PA14/PGMD2	28	PA4/PGMNCMD	40	TCK
5	AD6	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	AD7	18	VDDCORE	30	TST	42	ERASE
7	VDDIN	19	PA12/PGMD0	31	PA3	43	VDDFLASH
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	GND
9	PA17/PGMD5/AD0	21	PA10/PGMM2	33	VDDIO	45	XOUT
10	PA18/PGMD6/AD1	22	PA9/PGMM1	34	GND	46	XIN/PGMCK
11	PA19/PGMD7/AD2	23	PA8/PGMM0	35	PA1/PGMEN1	47	PLLRC
12	PA20/AD3	24	PA7/PGMNVALID	36	PA0/PGMEN0	48	VDDPLL

Note: 1. The bottom pad of the QFN package must be connected to ground.

Figure 5-1. 3.3V System Single Power Supply Schematic



6. I/O Lines Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are schmitt trigger inputs. TMS and TCK are 5-V tolerant, TDI is not. TMS, TDI and TCK do not integrate a pull-up resistor.

TDO is an output, driven at up to VDDIO, and has no pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. The JTAGSEL pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

6.2 Test Pin

The TST pin is used for manufacturing test, fast programming mode or SAM-BA Boot Recovery of the SAM7S Series when asserted high. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

To enter fast programming mode, the TST pin and the PA0 and PA1 pins should be tied high and PA2 tied to low.

To enter SAM-BA Boot Recovery, the TST pin and the PA0, PA1 and PA2 pins should be tied high for at least 10 seconds. Then a power cycle of the board is mandatory.

Driving the TST pin at a high level while PA0 or PA1 is driven at 0 leads to unpredictable results.

6.3 Reset Pin

The NRST pin is bidirectional with an open drain output buffer. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. There is no constraint on the length of the reset pulse, and the reset controller can guarantee a minimum pulse length. This allows connection of a simple push-button on the pin NRST as system user reset, and the use of the signal NRST to reset all the components of the system.

The NRST pin integrates a permanent pull-up resistor to VDDIO.

6.4 ERASE Pin

The ERASE pin is used to re-initialize the Flash content and some of its NVM bits. It integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

6.5 PIO Controller A Lines

- All the I/O lines PA0 to PA31on SAM7S512/256/128/64/321 (PA0 to PA20 on SAM7S32) are 5V-tolerant and all integrate a programmable pull-up resistorpulse leAlr40/29009328 TD(that88 Tm0 .563 8e7 Tw) are 5V)53.6s/290se leAll b

7. Processor and Architecture

7.1 ARM7TDMI Processor

- RISC processor based on ARMv4T Von Neumann architecture
  - Runs at up to 55 MHz, providing 0.9 MIPS/MHz
- Two instruction sets
  - ARM® high-performance 32-bit instruction set
  - Thumb® high code density 16-bit instruction set
- Three-stage pipeline architecture
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)

7.2 Debug and Test Features

- Integrated EmbeddedICE™ (embedded in-circuit emulator)
  - Two watchpoint units
  - Test access port accessible through a JTAG protocol
  - Debug communication channel
- Debug Unit
  - Two-pin UART
  - Debug communication channel interrupt handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on all digital pins

7.3 Memory Controller

- Bus Arbiter
  - Handles requests from the ARM7TDMI and the Peripheral DMA Controller
- Address decoder provides selection signals for
  - Three internal 1 Mbyte memory areas
  - One 256 Mbyte embedded peripheral area
- Abort Status Registers
  - Source, Type and all parameters of the access leading to an abort are saved
  -

8. Memories

8.1 SAM7S512

- 512 Kbytes of Flash Memory, dual plane
  - 2 contiguous banks of 1024 pages of 256 bytes
  - Fast access time, 30 MHz single-cycle access in Worst Case conditions
  - Page programming time: 6 ms, including page auto-erase
  - Page programming without auto-erase: 3 ms
  - Full chip erase time: 15 ms
  - 10,000 write cycles, 10-year data retention capability
  - 32 lock bits, protecting 32 sectors of 64 pages
  - Protection Mode to secure contents of the Flash
- 64 Kbytes of Fast SRAM
  - Single-cycle access at full speed

8.2 SAM7S256

- 256 Kbytes of Flash Memory, single plane
  - 1024 pages of 256 bytes
  - Fast access time, 30 MHz single-cycle access in Worst Case conditions
  - Page programming time: 6 ms, including page auto-erase
  - Page programming without auto-erase: 3 ms
  - Full chip erase time: 15 ms
  - 10,000 write cycles, 10-year data retention capability
  - 16 lock bits, protecting 16 sectors of 64 pages
  - Protection Mode to secure contents of the Flash
- 64 Kbytes of Fast SRAM
  - Single-cycle access at full speed

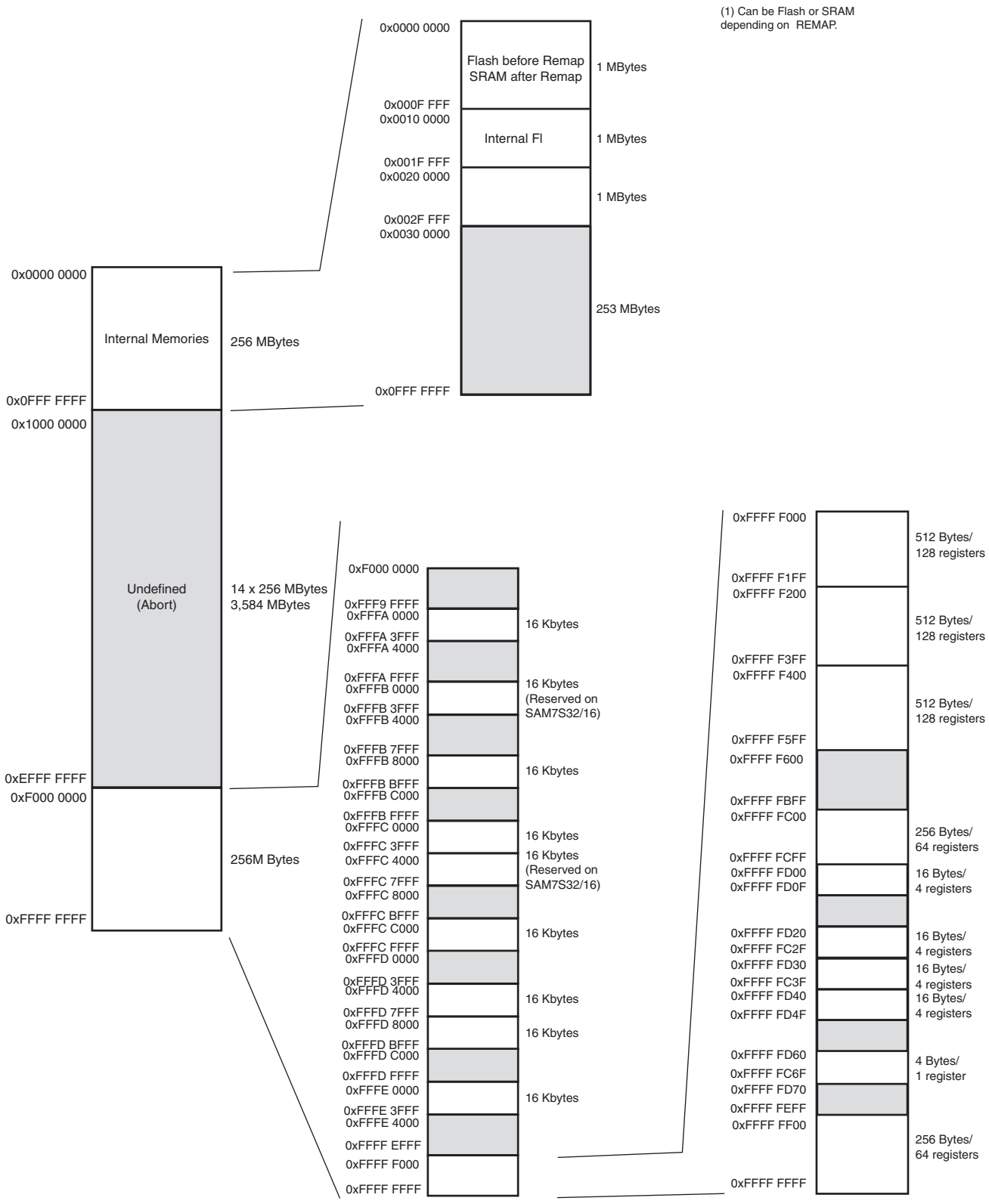
8.3 SAM7S128

- 128 Kbytes of Flash Memory, single plane
  - 512 pages of 256 bytes
  - Fast access time, 30 MHz single-cycle access in Worst Case conditions
  - Page programming time: 6 ms, including page auto-erase
  - Page programming without auto-erase: 3 ms
  - Full chip erase time: 15 ms
  - 10,000 write cycles, 10-year data retention capability
  - 8 lock bits, protecting 8 sectors of 64 pages
  - Protection Mode to secure contents of the Flash
- 32 Kbytes of Fast SRAM
  - Single-cycle access at full speed

8.4 SAM7S64

- 64 Kbytes of Flash Memory, single plane
  - 512 pages of 128 bytes

Figure 8-1. SAM SAM7S512/256/128/64/321/32/161/16 Memory Mapping



8.7 Memory Mapping

8.7.1 Internal SRAM

- The SAM7S512 embeds a high-speed 64-Kbyte SRAM bank.
- The SAM7S256 embeds a high-speed 64-Kbyte SRAM bank.
- The SAM7S128 embeds a high-speed 32-Kbyte SRAM bank.
- The SAM7S64 embeds a high-speed 16-Kbyte SRAM bank.
- The SAM7S321 embeds a high-speed 8-Kbyte SRAM bank.
- The SAM7S32 embeds a high-speed 8-Kbyte SRAM bank.
- The SAM7S161 embeds a high-speed 4-Kbyte SRAM bank.
- The SAM7S16 embeds a high-speed 4-Kbyte SRAM bank

After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x0020 0000. After Remap, the SRAM also becomes available at address 0x0.

8.7.2 Internal ROM

The SAM7S Series embeds an Internal ROM. The ROM contains the FFPI and the SAM-BA program.

The internal ROM is not mapped by default.

8.7.3 Internal Flash

- The SAM7S512 features two contiguous banks (dual plane) of 256 Kbytes of Flash.
- The SAM7S256 features one bank (single plane) of 256 Kbytes of Flash.
- The SAM7S128 features one bank (single plane) of 128 Kbytes of Flash.
- The SAM7S64 features one bank (single plane) of 64 Kbytes of Flash.
- The SAM7S321/32 features one bank (single plane) of 32 Kbytes of Flash.
- The SAM7S161/16 features one bank (single plane) of 16 Kbytes of Flash.

At any time, the Flash is mapped to address 0x0010 0000. It is also accessible at address 0x0 after the reset and before the Remap Command.

Figure 8-2. Internal Memory Mapping

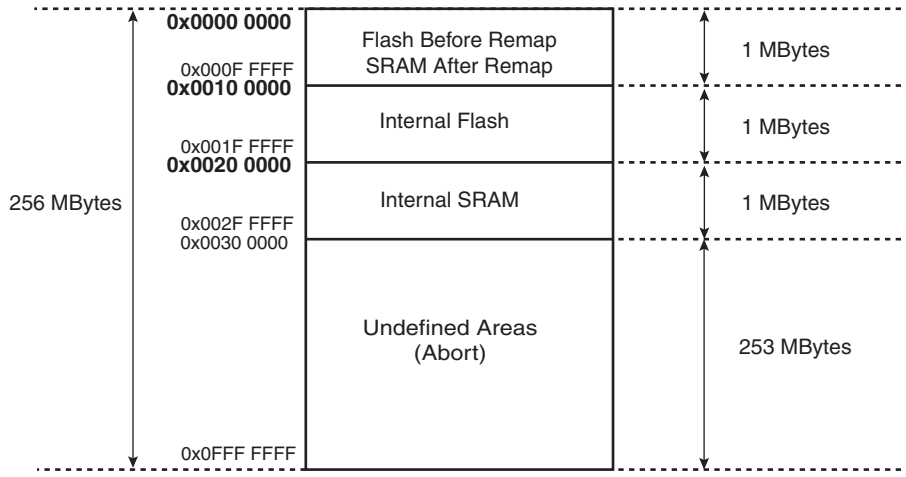
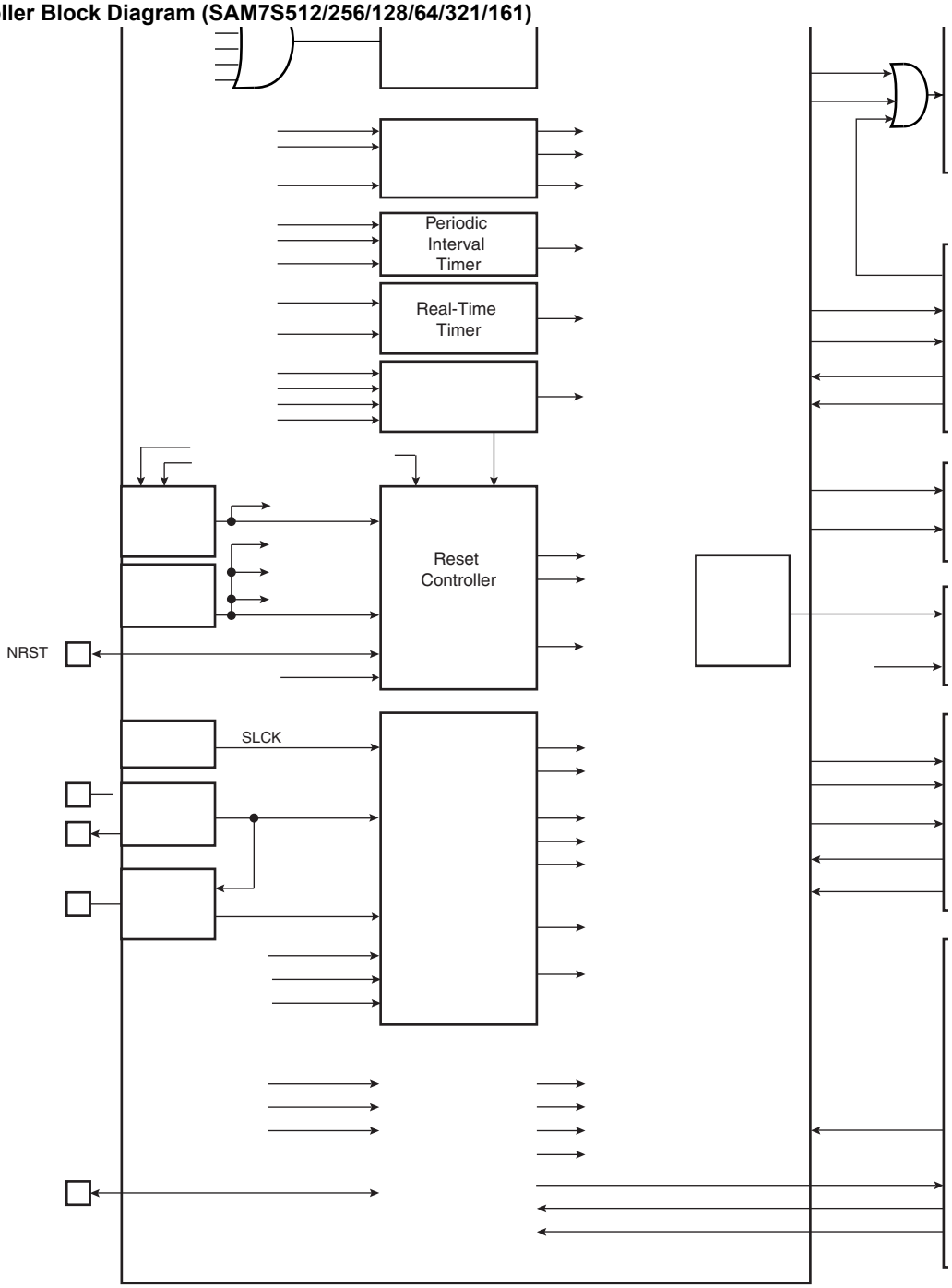


Figure 9-1. System Controller Block Diagram (SAM7S512/256/128/64/321/161)



9.9 PIO Controller

- One PIO Controller, controlling 32 I/O lines (21 for SAM7S32/16)
- Fully programmable through set/clear registers
- Multiplexing of two peripheral functions per I/O line
- For each I/O line (whether assigned to a peripheral or used as general-purpose I/O)
  - Input change interrupt
  - Half a clock period glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull-up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

9.10 Voltage Regulator Controller

The aim of this controller is to select the Power Mode of the Voltage Regulator between Normal Mode (bit 0 is cleared) or Standby Mode (bit 0 is set).

11. Package Drawings

The SAM7S series devices are available in LQFP and QFN package types.

11.1 LQFP Packages

Figure 11-1. 48-and 64-lead LQFP Package Drawing

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The SAM7S series devices are available in LQFP and QFN package types.

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Figure 11-1. 48-and 64-lead LQFP Package Drawing

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