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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM7® |
| Core Size | 16/32-Bit |
| Speed | 55MHz |
| Connectivity | I²C, SPI, SSC, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 32 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 1.95V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-QFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/atmel/at91sam7s321-mu |

# 2. Block Diagram

**Figure 2-1. SAM7S512/256/128/64/321/161 Block Diagram**

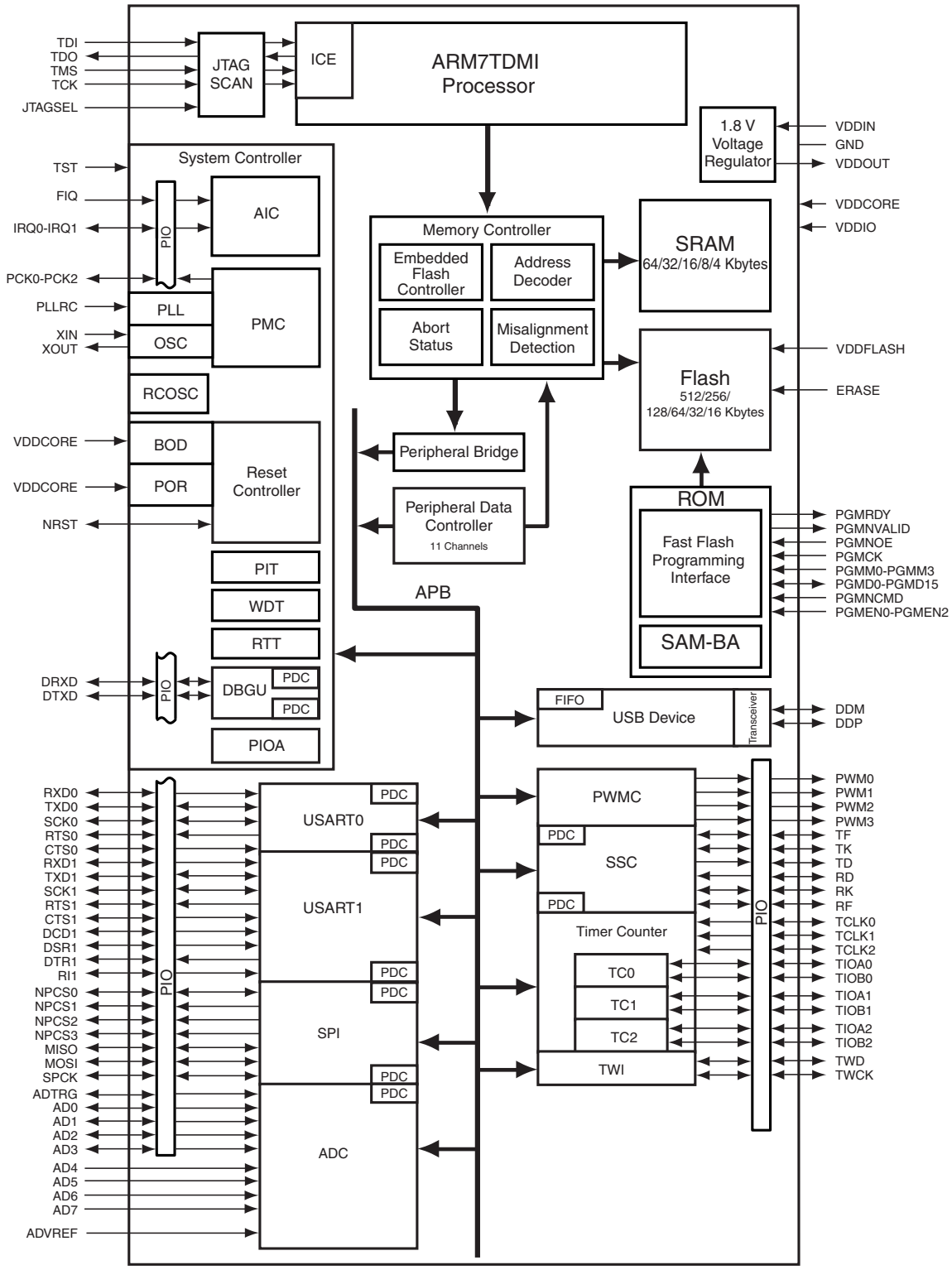
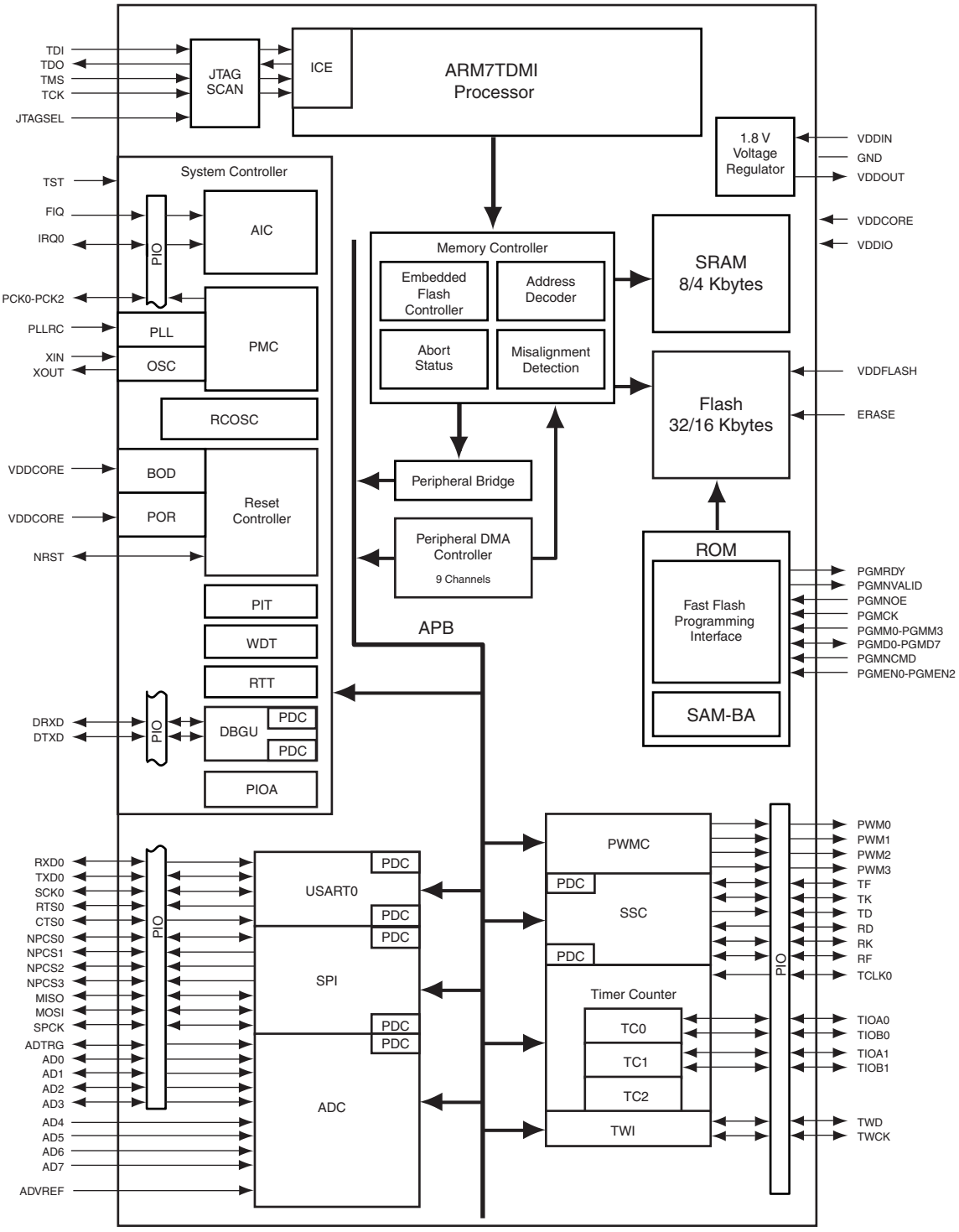


**Figure 2-2. SAM7S32/16 Block Diagram**



# 3. Signal Description

**Table 3-1. Signal Description List**

| | | | | |
|---|---|---|---|---|
| | | | | |
| VDDIN | Voltage and ADC Regulator Power Supply Input | Power | | 3.0 to 3.6V |
| VDDOUT | Voltage Regulator Output | Power | | 1.85V nominal |
| VDDFLASH | Flash Power Supply | Power | | 3.0V to 3.6V |
| VDDIO | I/O Lines Power Supply | Power | | 3.0V to 3.6V or 1.65V to 1.95V |
| VDDCORE | Core Power Supply | Power | | 1.65V to 1.95V |
| VDDPLL | PLL | Power | | 1.65V to 1.95V |
| GND | Ground | Ground | | |
| | | | | |
| XIN | Main Oscillator Input | Input | | |
| XOUT | Main Oscillator Output | Output | | |
| PLLRC | PLL Filter | Input | | |
| PCK0 - PCK2 | Programmable Clock Output | Output | | |
| | | | | |
| TCK | Test Clock | Input | | No pull-up resistor |
| TDI | Test Data In | Input | | No pull-up resistor |
| TDO | Test Data Out | Output | | |
| TMS | Test Mode Select | Input | | No pull-up resistor |
| JTAGSEL | JTAG Selection | Input | | Pull-down resistor(1) |
| | | | | |
| ERASE | Flash and NVM Configuration Bits Erase Command | Input | High | Pull-down resistor(1) |
| | | | | |
| NRST | Microcontroller Reset | I/O | Low | Open-drain with pull-Up resistor |
| TST | Test Mode Select | Input | High | Pull-down resistor(1) |
| | | | | |
| DRXD | Debug Receive Data | Input | | |
| DTXD | Debug Transmit Data | Output | | |
| | | | | |
| IRQ0 - IRQ1 | External Interrupt Inputs | Input | | IRQ1 not present on SAM7S32/16 |
| FIQ | Fast Interrupt Input | Input | | |
| | | | | |
| PA0 - PA31 | Parallel IO Controller A | I/O | | Pulled-up input at reset<br>PA0 - PA20 only on SAM7S32/16 |

**Table 3-1. Signal Description List (Continued)**

| | | | | |
|---|---|---|---|---|
| | | | | |
| TWD | Two-wire Serial Data | I/O | | |
| TWCK | Two-wire Serial Clock | I/O | | |
| | | | | |
| AD0-AD3 | Analog Inputs | Analog | | Digital pulled-up inputs at reset |
| AD4-AD7 | Analog Inputs | Analog | | Analog Inputs |
| ADTRG | ADC Trigger | Input | | |
| ADVREF | ADC Reference | Analog | | |
| | | | | |
| PGMEN0-PGMEN2 | Programming Enabling | Input | | |
| PGMM0-PGMM3 | Programming Mode | Input | | |
| PGMD0-PGMD15 | Programming Data | I/O | | PGMD0-PGMD7 only on SAM7S32/16 |
| PGMRDY | Programming Ready | Output | High | |
| PGMNVALID | Data Direction | Output | Low | |
| PGMNOE | Programming Read | Input | Low | |
| PGMCK | Programming Clock | Input | | |
| PGMNCMD | Programming Command | Input | Low | |

Note: 1. Refer to Section 6. “I/O Lines Considerations” on page 14.

# 4. Package and Pinout

The SAM7S512/256/128/64/321 are available in a 64-lead LQFP or 64-pad QFN package.

The SAM7S161 is available in a 64-Lead LQFP package.

The SAM7S32/16 are available in a 48-lead LQFP or 48-pad QFN package.

## 4.1 64-lead LQFP and 64-pad QFN Package Outlines

Figure 4-1 and Figure 4-2 show the orientation of the 64-lead LQFP and the 64-pad QFN package. A detailed mechanical description is given in the section Mechanical Characteristics of the full datasheet.

**Figure 4-1. 64-lead LQFP Package (Top View)**

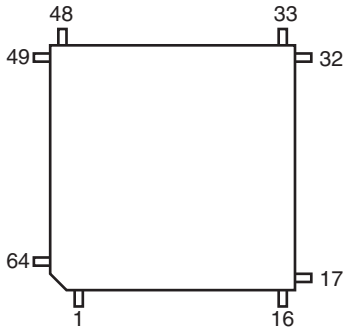
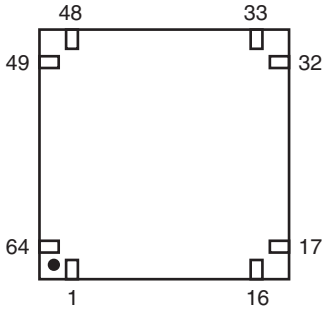



**Figure 4-2. 64-pad QFN Package (Top View)**



## 4.2 64-lead LQFP and 64-pad QFN Pinout

**Table 4-1. SAM7S512/256/128/64/321/161 Pinout**[1]

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | ADVREF | 17 | GND | 33 | TDI | 49 | TDO |
| 2 | GND | 18 | VDDIO | 34 | PA6/PGMNOE | 50 | JTAGSEL |
| 3 | AD4 | 19 | PA16/PGMD4 | 35 | PA5/PGMRDY | 51 | TMS |
| 4 | AD5 | 20 | PA15/PGMD3 | 36 | PA4/PGMNCMD | 52 | PA31 |
| 5 | AD6 | 21 | PA14/PGMD2 | 37 | PA27/PGMD15 | 53 | TCK |
| 6 | AD7 | 22 | PA13/PGMD1 | 38 | PA28 | 54 | VDDCORE |
| 7 | VDDIN | 23 | PA24/PGMD12 | 39 | NRST | 55 | ERASE |
| 8 | VDDOUT | 24 | VDDCORE | 40 | TST | 56 | DDM |
| 9 | PA17/PGMD5/AD0 | 25 | PA25/PGMD13 | 41 | PA29 | 57 | DDP |
| 10 | PA18/PGMD6/AD1 | 26 | PA26/PGMD14 | 42 | PA30 | 58 | VDDIO |
| 11 | PA21/PGMD9 | 27 | PA12/PGMD0 | 43 | PA3 | 59 | VDDFLASH |
| 12 | VDDCORE | 28 | PA11/PGMM3 | 44 | PA2/PGMEN2 | 60 | GND |
| 13 | PA19/PGMD7/AD2 | 29 | PA10/PGMM2 | 45 | VDDIO | 61 | XOUT |
| 14 | PA22/PGMD10 | 30 | PA9/PGMM1 | 46 | GND | 62 | XIN/PGMCK |
| 15 | PA23/PGMD11 | 31 | PA8/PGMM0 | 47 | PA1/PGMEN1 | 63 | PLLRC |
| 16 | PA20/PGMD8/AD3 | 32 | PA7/PGMNVALID | 48 | PA0/PGMEN0 | 64 | VDDPLL |

Note: 1. The bottom pad of the QFN package must be connected to ground.

## 4.3 48-lead LQFP and 48-pad QFN Package Outlines

Figure 4-3 and Figure 4-4 show the orientation of the 48-lead LQFP and the 48-pad QFN package. A detailed mechanical description is given in the section Mechanical Characteristics of the full datasheet.

**Figure 4-3. 48-lead LQFP Package (Top View)**

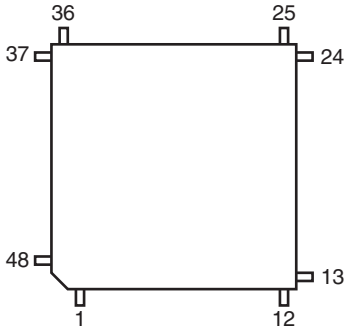
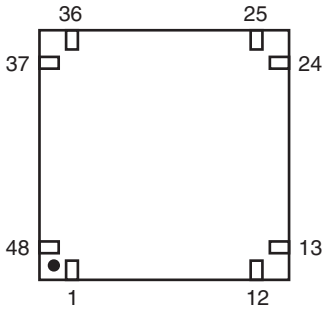



**Figure 4-4. 48-pad QFN Package (Top View)**



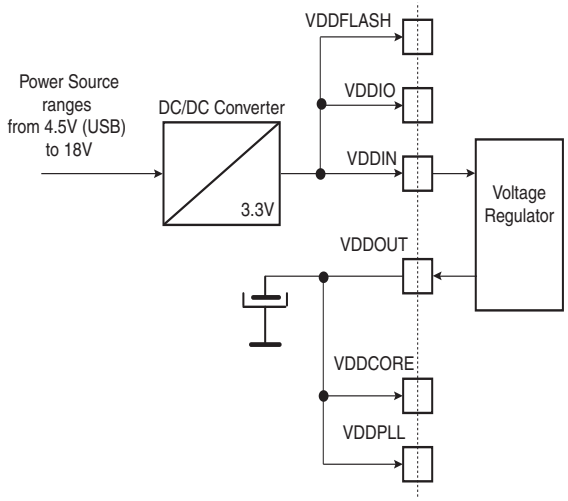

## 4.4 48-lead LQFP and 48-pad QFN Pinout

**Table 4-2. SAM7S32/16 Pinout**[1]

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | ADVREF | 13 | VDDIO | 25 | TDI | 37 | TDO |
| 2 | GND | 14 | PA16/PGMD4 | 26 | PA6/PGMNOE | 38 | JTAGSEL |
| 3 | AD4 | 15 | PA15/PGMD3 | 27 | PA5/PGMRDY | 39 | TMS |
| 4 | AD5 | 16 | PA14/PGMD2 | 28 | PA4/PGMNCMD | 40 | TCK |
| 5 | AD6 | 17 | PA13/PGMD1 | 29 | NRST | 41 | VDDCORE |
| 6 | AD7 | 18 | VDDCORE | 30 | TST | 42 | ERASE |
| 7 | VDDIN | 19 | PA12/PGMD0 | 31 | PA3 | 43 | VDDFLASH |
| 8 | VDDOUT | 20 | PA11/PGMM3 | 32 | PA2/PGMEN2 | 44 | GND |
| 9 | PA17/PGMD5/AD0 | 21 | PA10/PGMM2 | 33 | VDDIO | 45 | XOUT |
| 10 | PA18/PGMD6/AD1 | 22 | PA9/PGMM1 | 34 | GND | 46 | XIN/PGMCK |
| 11 | PA19/PGMD7/AD2 | 23 | PA8/PGMM0 | 35 | PA1/PGMEN1 | 47 | PLLRC |
| 12 | PA20/AD3 | 24 | PA7/PGMNVALID | 36 | PA0/PGMEN0 | 48 | VDDPLL |

Note: 1. The bottom pad of the QFN package must be connected to ground.

**Figure 5-1. 3.3V System Single Power Supply Schematic**



# 7. Processor and Architecture

## 7.1 ARM7TDMI Processor

- RISC processor based on ARMv4T Von Neumann architecture
  - Runs at up to 55 MHz, providing 0.9 MIPS/MHz
- Two instruction sets
  - ARM® high-performance 32-bit instruction set
  - Thumb® high code density 16-bit instruction set
- Three-stage pipeline architecture
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)

## 7.2 Debug and Test Features

- Integrated EmbeddedICE™ (embedded in-circuit emulator)
  - Two watchpoint units
  - Test access port accessible through a JTAG protocol
  - Debug communication channel
- Debug Unit
  - Two-pin UART
  - Debug communication channel interrupt handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on all digital pins

## 7.3 Memory Controller

- Bus Arbiter
  - Handles requests from the ARM7TDMI and the Peripheral DMA Controller
- Address decoder provides selection signals for
  - Three internal 1 Mbyte memory areas
  - One 256 Mbyte embedded peripheral area
- Abort Status Registers
  - Source, Type and all parameters of the access leading to an abort are saved
  - Facilitates debug by detection of bad pointers
- Misalignment Detector
  - Alignment checking of all data accesses
  - Abort generation in case of misalignment
- Remap Command
  - Remaps the SRAM in place of the embedded non-volatile memory
  - Allows handling of dynamic exception vectors
- Embedded Flash Controller
  - Embedded Flash interface, up to three programmable wait states
  - Prefetch buffer, buffering and anticipating the 16-bit requests, reducing the required wait states
  - Key-protected program, erase and lock/unlock sequencer
  - Single command for erasing, programming and locking operations
  - Interrupt generation in case of forbidden operation

# 8. Memories

## 8.1 SAM7S512

- 512 Kbytes of Flash Memory, dual plane
  - 2 contiguous banks of 1024 pages of 256 bytes
  - Fast access time, 30 MHz single-cycle access in Worst Case conditions
  - Page programming time: 6 ms, including page auto-erase
  - Page programming without auto-erase: 3 ms
  - Full chip erase time: 15 ms
  - 10,000 write cycles, 10-year data retention capability
  - 32 lock bits, protecting 32 sectors of 64 pages
  - Protection Mode to secure contents of the Flash
- 64 Kbytes of Fast SRAM
  - Single-cycle access at full speed

## 8.2 SAM7S256

- 256 Kbytes of Flash Memory, single plane
  - 1024 pages of 256 bytes
  - Fast access time, 30 MHz single-cycle access in Worst Case conditions
  - Page programming time: 6 ms, including page auto-erase
  - Page programming without auto-erase: 3 ms
  - Full chip erase time: 15 ms
  - 10,000 write cycles, 10-year data retention capability
  - 16 lock bits, protecting 16 sectors of 64 pages
  - Protection Mode to secure contents of the Flash
- 64 Kbytes of Fast SRAM
  - Single-cycle access at full speed

## 8.3 SAM7S128

- 128 Kbytes of Flash Memory, single plane
  - 512 pages of 256 bytes
  - Fast access time, 30 MHz single-cycle access in Worst Case conditions
  - Page programming time: 6 ms, including page auto-erase
  - Page programming without auto-erase: 3 ms
  - Full chip erase time: 15 ms
  - 10,000 write cycles, 10-year data retention capability
  - 8 lock bits, protecting 8 sectors of 64 pages
  - Protection Mode to secure contents of the Flash
- 32 Kbytes of Fast SRAM
  - Single-cycle access at full speed

## 8.4 SAM7S64

- 64 Kbytes of Flash Memory, single plane
  - 512 pages of 128 bytes

## 8.7 Memory Mapping

### 8.7.1 Internal SRAM

- The SAM7S512 embeds a high-speed 64-Kbyte SRAM bank.
- The SAM7S256 embeds a high-speed 64-Kbyte SRAM bank.
- The SAM7S128 embeds a high-speed 32-Kbyte SRAM bank.
- The SAM7S64 embeds a high-speed 16-Kbyte SRAM bank.
- The SAM7S321 embeds a high-speed 8-Kbyte SRAM bank.
- The SAM7S32 embeds a high-speed 8-Kbyte SRAM bank.
- The SAM7S161 embeds a high-speed 4-Kbyte SRAM bank.
- The SAM7S16 embeds a high-speed 4-Kbyte SRAM bank

After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x0020 0000. After Remap, the SRAM also becomes available at address 0x0.

### 8.7.2 Internal ROM

The SAM7S Series embeds an Internal ROM. The ROM contains the FFPI and the SAM-BA program.

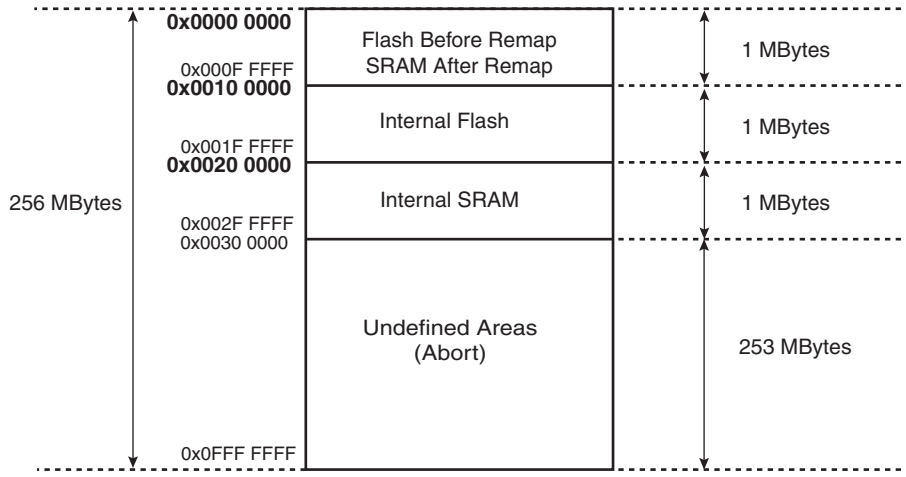
The internal ROM is not mapped by default.

### 8.7.3 Internal Flash

- The SAM7S512 features two contiguous banks (dual plane) of 256 Kbytes of Flash.
- The SAM7S256 features one bank (single plane) of 256 Kbytes of Flash.
- The SAM7S128 features one bank (single plane) of 128 Kbytes of Flash.
- The SAM7S64 features one bank (single plane) of 64 Kbytes of Flash.
- The SAM7S321/32 features one bank (single plane) of 32 Kbytes of Flash.
- The SAM7S161/16 features one bank (single plane) of 16 Kbytes of Flash.

At any time, the Flash is mapped to address 0x0010 0000. It is also accessible at address 0x0 after the reset and before the Remap Command.

**Figure 8-2. Internal Memory Mapping**



## 8.8 Embedded Flash

### 8.8.1 Flash Overview

- The Flash of the SAM7S512 is organized in two banks (dual plane) of 1024 pages of 256 bytes. The 524,288 bytes are organized in 32-bit words.
- The Flash of the SAM7S256 is organized in 1024 pages (single plane) of 256 bytes. The 262,144 bytes are organized in 32-bit words.
- The Flash of the SAM7S128 is organized in 512 pages (single plane) of 256 bytes. The 131,072 bytes are organized in 32-bit words.
- The Flash of the SAM7S64 is organized in 512 pages (single plane) of 128 bytes. The 65,536 bytes are organized in 32-bit words.
- The Flash of the SAM7S321/32 is organized in 256 pages (single plane) of 128 bytes. The 32,768 bytes are organized in 32-bit words.
- The Flash of the SAM7S161/16 is organized in 256 pages (single plane) of 64 bytes. The 16,384 bytes are organized in 32-bit words.
- The Flash of the SAM7S512/256/128 contains a 256-byte write buffer, accessible through a 32-bit interface.
- The Flash of the SAM7S64/321/32/161/16 contains a 128-byte write buffer, accessible through a 32-bit interface.

The Flash benefits from the integration of a power reset cell and from the brownout detector. This prevents code corruption during power supply changes, even in the worst conditions.

When Flash is not used (read or write access), it is automatically placed into standby mode.

### 8.8.2 Embedded Flash Controller

The Embedded Flash Controller (EFC) manages accesses performed by the masters of the system. It enables reading the Flash and writing the write buffer. It also contains a User Interface, mapped within the Memory Controller on the APB. The User Interface allows:

- programming of the access parameters of the Flash (number of wait states, timings, etc.)
- starting commands such as full erase, page erase, page program, NVM bit set, NVM bit clear, etc.
- getting the end status of the last command
- getting error status
- programming interrupts on the end of the last commands or on errors

The Embedded Flash Controller also provides a dual 32-bit prefetch buffer that optimizes 16-bit access to the Flash. This is particularly efficient when the processor is running in Thumb mode.

Two EFCs are embedded in the SAM7S512 to control each bank of 256 Kbytes. Dual plane organization allows concurrent Read and Program. Read from one memory plane may be performed even while program or erase functions are being executed in the other memory plane.

One EFC is embedded in the SAM7S256/128/64/32/321/161/16 to control the single plane 256/128/64/32/16 Kbytes.

The 8 NVM bits are software programmable through the EFC User Interface. The command “Set Lock Bit” enables the protection. The command “Clear Lock Bit” unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

#### 8.8.3.6 SAM7S161/16

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S161/16 contains 8 lock regions and each lock region contains 32 pages of 64 bytes. Each lock region has a size of 2 Kbytes.

If a locked-region’s erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 8 NVM bits are software programmable through the EFC User Interface. The command “Set Lock Bit” enables the protection. The command “Clear Lock Bit” unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

Table 8-1 summarizes the configuration of the eight devices.

**Table 8-1. Flash Configuration Summary**

| | | | |
|---|---|---|---|
| SAM7S512 | 32 | 64 | 256 bytes |
| SAM7S256 | 16 | 64 | 256 bytes |
| SAM7S128 | 8 | 64 | 256 bytes |
| SAM7S64 | 16 | 32 | 128 bytes |
| SAM7S321/32 | 8 | 32 | 128 bytes |
| SAM7S161/16 | 8 | 32 | 64 bytes |

### 8.8.4 Security Bit Feature

The SAM7S Series features a security bit, based on a specific NVM Bit. When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the Command “Set Security Bit” of the EFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full flash erase is performed. When the security bit is deactivated, all accesses to the flash are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 50 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

### 8.8.5 Non-volatile Brownout Detector Control

Two general purpose NVM (GPNVM) bits are used for controlling the brownout detector (BOD), so that even after a power loss, the brownout detector operations remain in their state.

These two GPNVM bits can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EFC User Interface.

- GPNVM Bit 0 is used as a brownout detector enable bit. Setting the GPNVM Bit 0 enables the BOD, clearing it disables the BOD. Asserting ERASE clears the GPNVM Bit 0 and thus disables the brownout detector by default.
- The GPNVM Bit 1 is used as a brownout reset enable signal for the reset controller. Setting the GPNVM Bit 1 enables the brownout reset when a brownout is detected, Clearing the GPNVM Bit 1 disables the brownout reset. Asserting ERASE disables the brownout reset by default.

**Figure 9-1. System Controller Block Diagram (SAM7S512/256/128/64/321/161)**

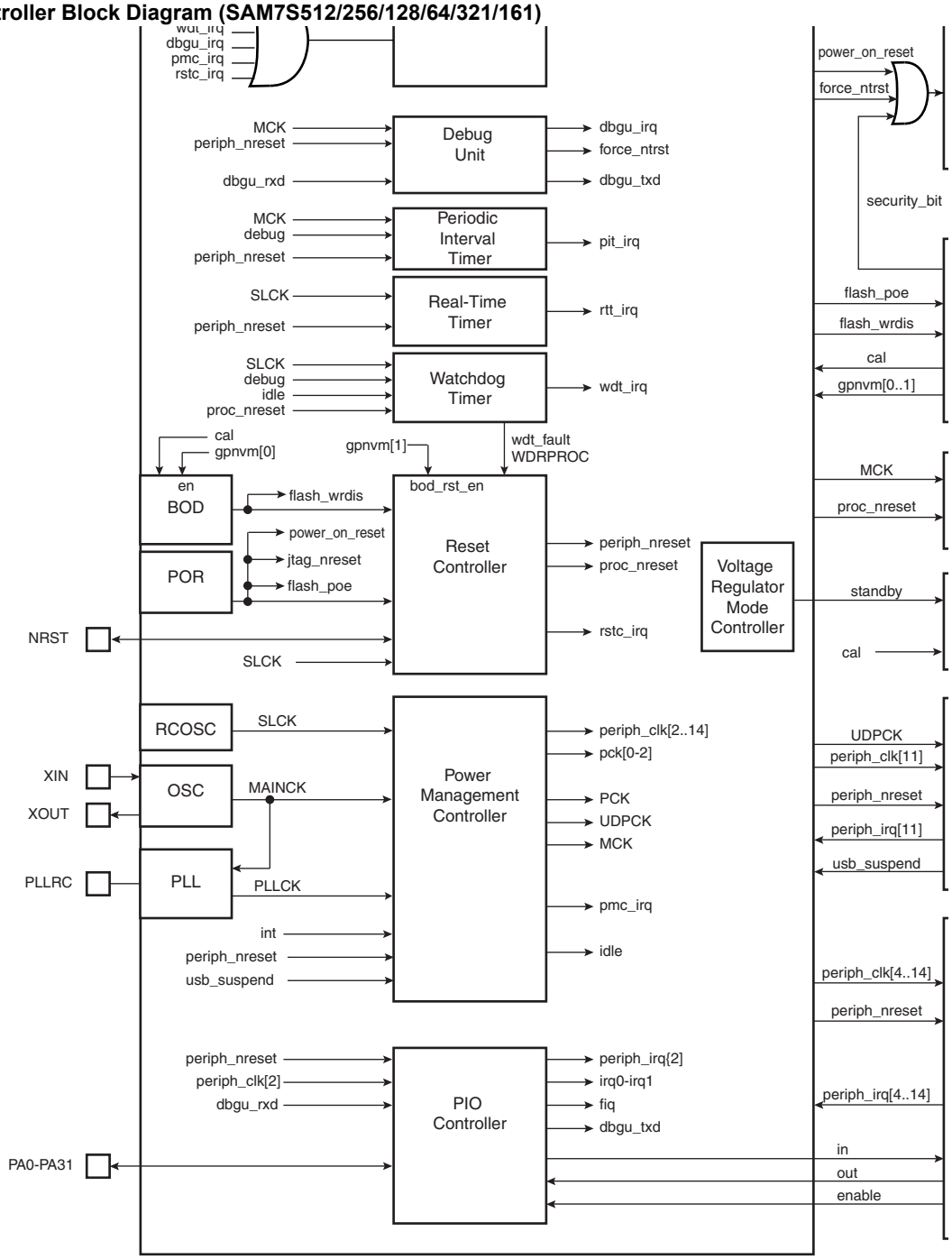


**Figure 9-2. System Controller Block Diagram (SAM7S32/16)**

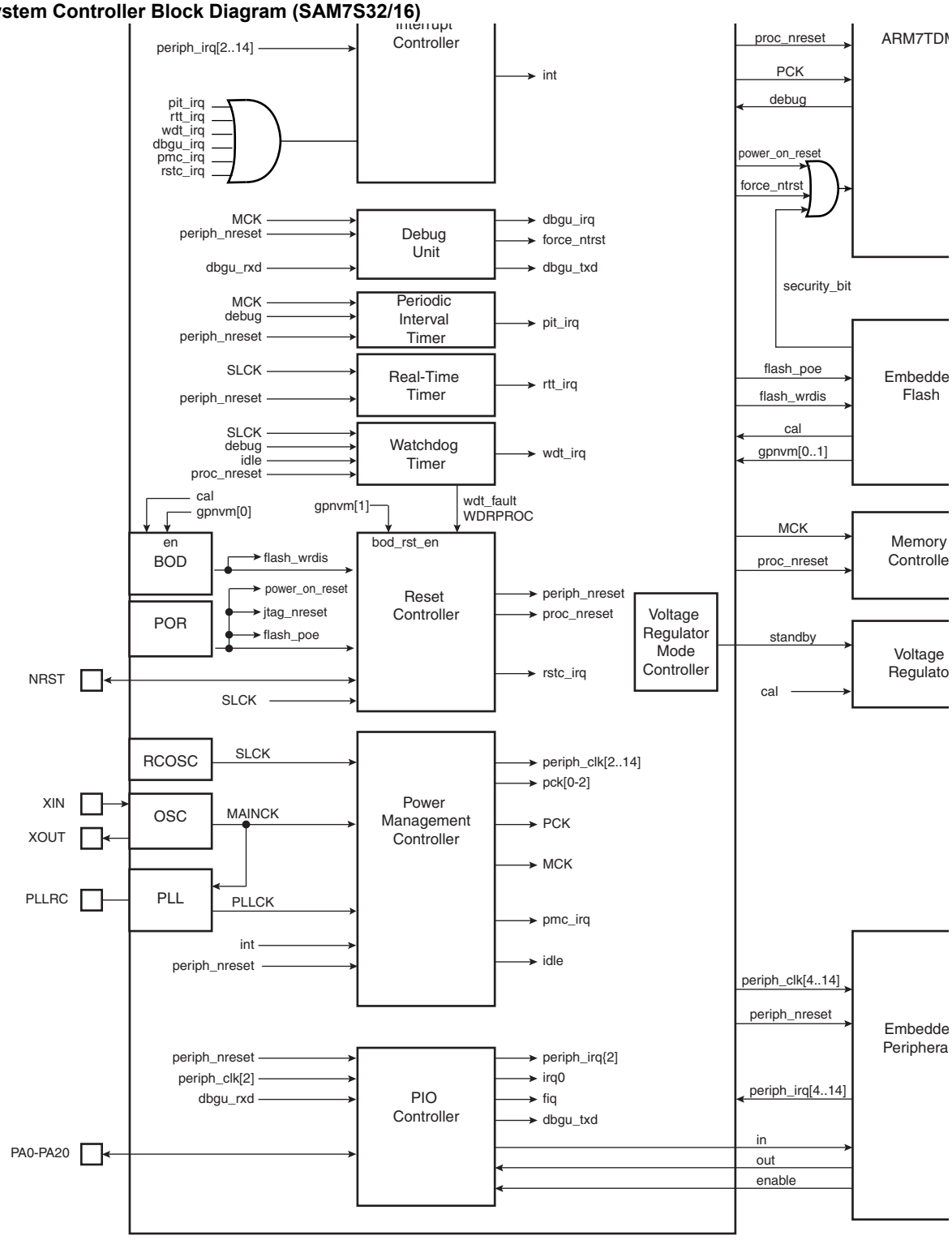


**Table 10-2. Peripheral Identifiers (SAM7S32/16)**

| | | | |
|---|---|---|---|
| 0 | AIC | Advanced Interrupt Controller | FIQ |
| 1 | SYSC[1] | System | |
| 2 | PIOA | Parallel I/O Controller A | |
| 3 | Reserved | | |
| 4 | ADC[1] | Analog-to Digital Converter | |
| 5 | SPI | Serial Peripheral Interface | |
| 6 | US | USART | |
| 7 | Reserved | | |
| 8 | SSC | Synchronous Serial Controller | |
| 9 | TWI | Two-wire Interface | |
| 10 | PWMC | PWM Controller | |
| 11 | Reserved | | |
| 12 | TC0 | Timer/Counter 0 | |
| 13 | TC1 | Timer/Counter 1 | |
| 14 | TC2 | Timer/Counter 2 | |
| 15 - 29 | Reserved | | |
| 30 | AIC | Advanced Interrupt Controller | IRQ0 |
| 31 | Reserved | | |

## 10.3 Peripheral Multiplexing on PIO Lines

The SAM7S Series features one PIO controller, PIOA, that multiplexes the I/O lines of the peripheral set.

PIO Controller A controls 32 lines (21 lines for SAM7S32/16). Each line can be assigned to one of two peripheral functions, A or B. Some of them can also be multiplexed with the analog inputs of the ADC Controller.

Table 10-3, “Multiplexing on PIO Controller A (SAM7S512/256/128/64/321/161),” on page 35 and Table 10-4, “Multiplexing on PIO Controller A (SAM7S32/16),” on page 36 define how the I/O lines of the peripherals A, B or the analog inputs are multiplexed on the PIO Controller A. The two columns “Function” and “Comments” have been inserted for the user’s own comments; they may be used to track how pins are defined in an application.

Note that some peripheral functions that are output only may be duplicated in the table.

All pins reset in their Parallel I/O lines function are configured as input with the programmable pull-up enabled, so that the device is maintained in a static state as soon as a reset is detected.

## 10.4 PIO Controller A Multiplexing

**Table 10-3. Multiplexing on PIO Controller A (SAM7S512/256/128/64/321/161)**

| | | | | | |
|---|---|---|---|---|---|
| | | | | | |
| PA0 | PWM0 | TIOA0 | High-Drive | | |
| PA1 | PWM1 | TIOB0 | High-Drive | | |
| PA2 | PWM2 | SCK0 | High-Drive | | |
| PA3 | TWD | NPCS3 | High-Drive | | |
| PA4 | TWCK | TCLK0 | | | |
| PA5 | RXD0 | NPCS3 | | | |
| PA6 | TXD0 | PCK0 | | | |
| PA7 | RTS0 | PWM3 | | | |
| PA8 | CTS0 | ADTRG | | | |
| PA9 | DRXD | NPCS1 | | | |
| PA10 | DTXD | NPCS2 | | | |
| PA11 | NPCS0 | PWM0 | | | |
| PA12 | MISO | PWM1 | | | |
| PA13 | MOSI | PWM2 | | | |
| PA14 | SPCK | PWM3 | | | |
| PA15 | TF | TIOA1 | | | |
| PA16 | TK | TIOB1 | | | |
| PA17 | TD | PCK1 | AD0 | | |
| PA18 | RD | PCK2 | AD1 | | |
| PA19 | RK | FIQ | AD2 | | |
| PA20 | RF | IRQ0 | AD3 | | |
| PA21 | RXD1 | PCK1 | | | |
| PA22 | TXD1 | NPCS3 | | | |
| PA23 | SCK1 | PWM0 | | | |
| PA24 | RTS1 | PWM1 | | | |
| PA25 | CTS1 | PWM2 | | | |
| PA26 | DCD1 | TIOA2 | | | |
| PA27 | DTR1 | TIOB2 | | | |
| PA28 | DSR1 | TCLK1 | | | |
| PA29 | RI1 | TCLK2 | | | |
| PA30 | IRQ1 | NPCS2 | | | |
| PA31 | NPCS1 | PCK2 | | | |

**Table 10-4. Multiplexing on PIO Controller A (SAM7S32/16)**

| | | | | | |
|---|---|---|---|---|---|
| | | | | | |
| PA0 | PWM0 | TIOA0 | High-Drive | | |
| PA1 | PWM1 | TIOB0 | High-Drive | | |
| PA2 | PWM2 | SCK0 | High-Drive | | |
| PA3 | TWD | NPCS3 | High-Drive | | |
| PA4 | TWCK | TCLK0 | | | |
| PA5 | RXD0 | NPCS3 | | | |
| PA6 | TXD0 | PCK0 | | | |
| PA7 | RTS0 | PWM3 | | | |
| PA8 | CTS0 | ADTRG | | | |
| PA9 | DRXD | NPCS1 | | | |
| PA10 | DTXD | NPCS2 | | | |
| PA11 | NPCS0 | PWM0 | | | |
| PA12 | MISO | PWM1 | | | |
| PA13 | MOSI | PWM2 | | | |
| PA14 | SPCK | PWM3 | | | |
| PA15 | TF | TIOA1 | | | |
| PA16 | TK | TIOB1 | | | |
| PA17 | TD | PCK1 | AD0 | | |
| PA18 | RD | PCK2 | AD1 | | |
| PA19 | RK | FIQ | AD2 | | |
| PA20 | RF | IRQ0 | AD3 | | |

**Table 11-3. 48-pad QFN Package Dimensions (in mm)**

| Symbol | | | | | | |
|---|---|---|---|---|---|---|
| | | | | | | |
| A | – | – | 090 | – | – | 0.035 |
| A1 | – | – | 0.050 | – | – | 0.002 |
| A2 | – | 0.65 | 0.70 | – | 0.026 | 0.028 |
| A3 | 0.20 REF | | | 0.008 REF | | |
| b | 0.18 | 0.20 | 0.23 | 0.007 | 0.008 | 0.009 |
| D | 7.00 bsc | | | 0.276 bsc | | |
| D2 | 5.45 | 5.60 | 5.75 | 0.215 | 0.220 | 0.226 |
| E | 7.00 bsc | | | 0.276 bsc | | |
| E2 | 5.45 | 5.60 | 5.75 | 0.215 | 0.220 | 0.226 |
| L | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| e | 0.50 bsc | | | 0.020 bsc | | |
| R | 0.09 | – | – | 0.004 | – | – |
| Tolerances of Form and Position | | | | | | |
| aaa | 0.10 | | | 0.004 | | |
| bbb | 0.10 | | | 0.004 | | |
| ccc | 0.05 | | | 0.002 | | |

# 12. SAM7S Ordering Information

**Table 12-1.** SAM7S Series Ordering Information

| MLR A Ordering Code | MLR B Ordering Code | MLR C Ordering Code | MLR D Ordering Code | Package | Package Type | Temperature Operating Range |
|---|---|---|---|---|---|---|
| AT91SAM7S16-AU<br>AT91SAM7S16-MU | – | – | – | LQFP 48<br>QFN 48 | Green | Industrial<br>(-40· C to 85· C) |
| AT91SAM7S161-AU | – | – | – | LQFP 64 | Green | Industrial<br>(-40· C to 85· C) |
| AT91SAM7S32-AU-001<br>AT91SAM7S32-MU | AT91SAM7S32B-AU<br>AT91SAM7S32B-MU | | | LQFP 48<br>QFN 48 | Green | Industrial<br>(-40· C to 85· C) |
| AT91SAM7S321-AU<br>AT91SAM7S321-MU | – | – | – | LQFP 64<br>QFN 64 | Green | Industrial<br>(-40· C to 85· C) |
| – | AT91SAM7S64B-AU<br>AT91SAM7S64B-MU | AT91SAM7S64C-AU<br>AT91SAM7S64C-MU | – | LQFP 64<br>QFN 64 | Green | Industrial<br>(-40· C to 85· C) |
| – | AT91SAM7S128-AU-001<br>AT91SAM7S128-MU | AT91SAM7S128C-AU<br>AT91SAM7S128C-MU | AT91SAM7S128D-AU<br>AT91SAM7S128D-MU | LQFP 64<br>QFN 64 | Green | Industrial<br>(-40· C to 85· C) |
| – | AT91SAM7S256-AU-001<br>AT91SAM7S256-MU | AT91SAM7S256C-AU<br>AT91SAM7S256C-MU | AT91SAM7S256D-AU<br>AT91SAM7S256D-MU | LQFP 64<br>QFN 64 | Green | Industrial<br>(-40· C to 85· C) |
| AT91SAM7S512-AU<br>AT91SAM7S512-MU | AT91SAM7S512B-AU<br>AT91SAM7S512B-MU | – | – | LQFP 64<br>QFN 64 | Green | Industrial<br>(-40· C to 85· C) |