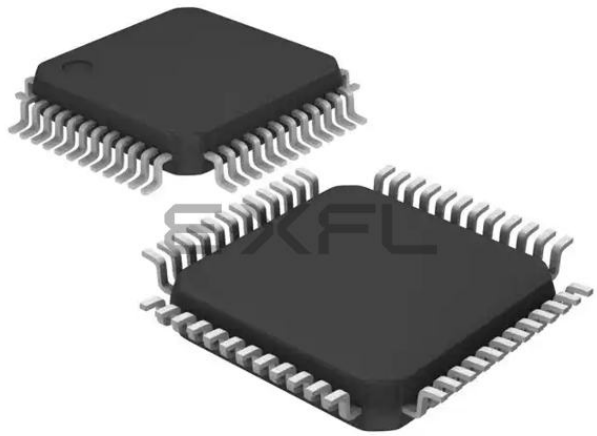

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	I²C, SPI, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam7s32b-au-999

- Debug Unit (DBGU)
  - 2-wire UART and Support for Debug Communication Channel interrupt, Programmable ICE Access Prevention
  - Mode for General Purpose 2-wire UART Serial Communication
- Periodic Interval Timer (PIT)
  - 20-bit Programmable Counter plus 12-bit Interval Counter
- Windowed Watchdog (WDT)
  - 12-bit key-protected Programmable Counter
  - Provides Reset or Interrupt Signals to the System
  - Counter May Be Stopped While the Processor is in Debug State or in Idle Mode
- Real-time Timer (RTT)
  - 32-bit Free-running Counter with Alarm
  - Runs Off the Internal RC Oscillator
- One Parallel Input/Output Controller (PIOA)
  - Thirty-two (SAM7S512/256/128/64/321/161) or twenty-one (SAM7S32/16) Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up resistor and Synchronous Output
- Eleven (SAM7S512/256/128/64/321/161) or Nine (SAM7S32/16) Peripheral DMA Controller (PDC) Channels
- One USB 2.0 Full Speed (12 Mbits per Second) Device Port (Except for the SAM7S32/16).
  - On-chip Transceiver, 328-byte Configurable Integrated FIFOs
- One Synchronous Serial Controller (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Two (SAM7S512/256/128/64/321/161) or One (SAM7S32/16) Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
  - Full Modem Line Support on USART1 (SAM7S512/256/128/64/321/161)
- One Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counter (TC)
  - Three External Clock Input and Two Multi-purpose I/O Pins per Channel (SAM7S512/256/128/64/321/161)
  - One External Clock Input and Two Multi-purpose I/O Pins for the first Two Channels Only (SAM7S32/16)
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- One Four-channel 16-bit PWM Controller (PWMC)
- One Two-wire Interface (TWI)
  - Master Mode Support Only, All Two-wire Atmel EEPROMs and I²C Compatible Devices Supported (SAM7S512/256/128/64/321/32)
  - Master, Multi-Master and Slave Mode Support, All Two-wire Atmel EEPROMs and I²C Compatible Devices Supported (SAM7S161/16)
- One 8-channel 10-bit Analog-to-Digital Converter, Four Channels Multiplexed with Digital I/Os
- SAM-BA™ Boot Assistant
  - Default Boot program
  - Interface with SAM-BA Graphic User Interface
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- 5V-tolerant I/Os, including Four High-current Drive I/O lines, Up to 16 mA Each (SAM7S161/16 I/Os Not 5V-tolerant)
- Power Supplies
  - Embedded 1.8V Regulator, Drawing up to 100 mA for the Core and External Components
  - 3.3V or 1.8V VDDIO I/O Lines Power Supply, Independent 3.3V VDDFLASH Flash Power Supply
  - 1.8V VDDCORE Core Power Supply with Brown-out Detector

- **Fully Static Operation: Up to 55 MHz at 1.65V and 85° C Worst Case Conditions**
- **Available in 64-lead LQFP Green or 64-pad QFN Green Package (SAM7S512/256/128/64/321/161) and 48-lead LQFP Green or 48-pad QFN Green Package (SAM7S32/16)**

1. Description

Atmel's SAM7S is a series of low pincount Flash microcontrollers based on the 32-bit ARM RISC processor. It features a high-speed Flash and an SRAM, a large set of peripherals, including a USB 2.0 device (except for the SAM7S32 and SAM7S16), and a complete set of system functions minimizing the number of external components. The device is an ideal migration path for 8-bit microcontroller users looking for additional performance and extended memory.

The embedded Flash memory can be programmed in-system via the JTAG-ICE interface or via a parallel interface on a production programmer prior to mounting. Built-in lock bits and a security bit protect the firmware from accidental overwrite and preserves its confidentiality.

The SAM7S Series system controller includes a reset controller capable of managing the power-on sequence of the microcontroller and the complete system. Correct device operation can be monitored by a built-in brownout detector and a watchdog running off an integrated RC oscillator.

The SAM7S Series are general-purpose microcontrollers. Their integrated USB Device port makes them ideal devices for peripheral applications requiring connectivity to a PC or cellular phone. Their aggressive price point and high level of integration pushes their scope of use far into the cost-sensitive, high-volume consumer market.

1.1 Configuration Summary of the SAM7S512, SAM7S256, SAM7S128, SAM7S64, SAM7S321, SAM7S32, SAM7S161 and SAM7S16

The SAM7S512, SAM7S256, SAM7S128, SAM7S64, SAM7S321, SAM7S32, SAM7S161 and SAM7S16 differ in memory size, peripheral set and package. Table 1-1 summarizes the configuration of the six devices.

Except for the SAM7S32/16, all other SAM7S devices are package and pinout compatible.

Table 1-1. Configuration Summary

SAM7S512	512 Kbytes	Master	dual plane	64 Kbytes	1	2(1) (2)	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S256	256 Kbytes	Master	single plane	64 Kbytes	1	2(1) (2)	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S128	128 Kbytes	Master	single plane	32 Kbytes	1	2(1) (2)	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S64	64 Kbytes	Master	single plane	16 Kbytes	1	2(2)	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S321	32 Kbytes	Master	single plane	8 Kbytes	1	2(2)	2	11	3	Yes	32	LQFP/ QFN 64
SAM7S32	32 Kbytes	Master	single plane	8 Kbytes	not present	1	1	9	3(3)	Yes	21	LQFP/ QFN 48
SAM7S161	16 Kbytes	Master/ Slave	single plane	4 Kbytes	1	2(2)	2	11	3	No	32	LQFP
SAM7S16	16 Kbytes	Master/ Slave	single plane	4 Kbytes	not present	1	1	9	3(3)	No	21	LQFP/ QFN 48

Notes: 1. Fractional Baud Rate.
2. Full modem line support on USART1.
3. Only two TC channels are accessible through the PIO.

2. Block Diagram

Figure 2-1. SAM7S512/256/128/64/321/161 Block Diagram

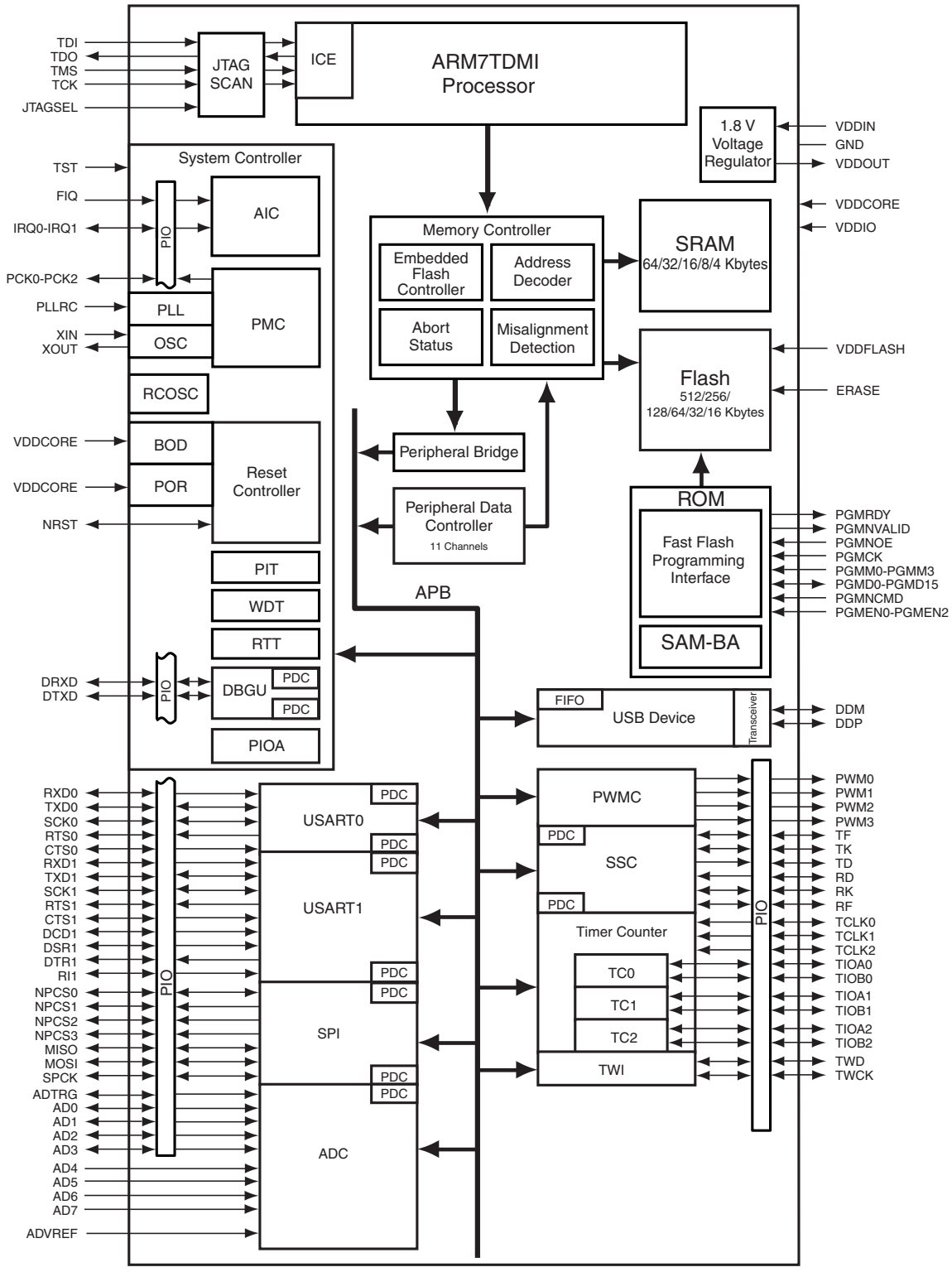


Figure 2-2. SAM7S32/16 Block Diagram

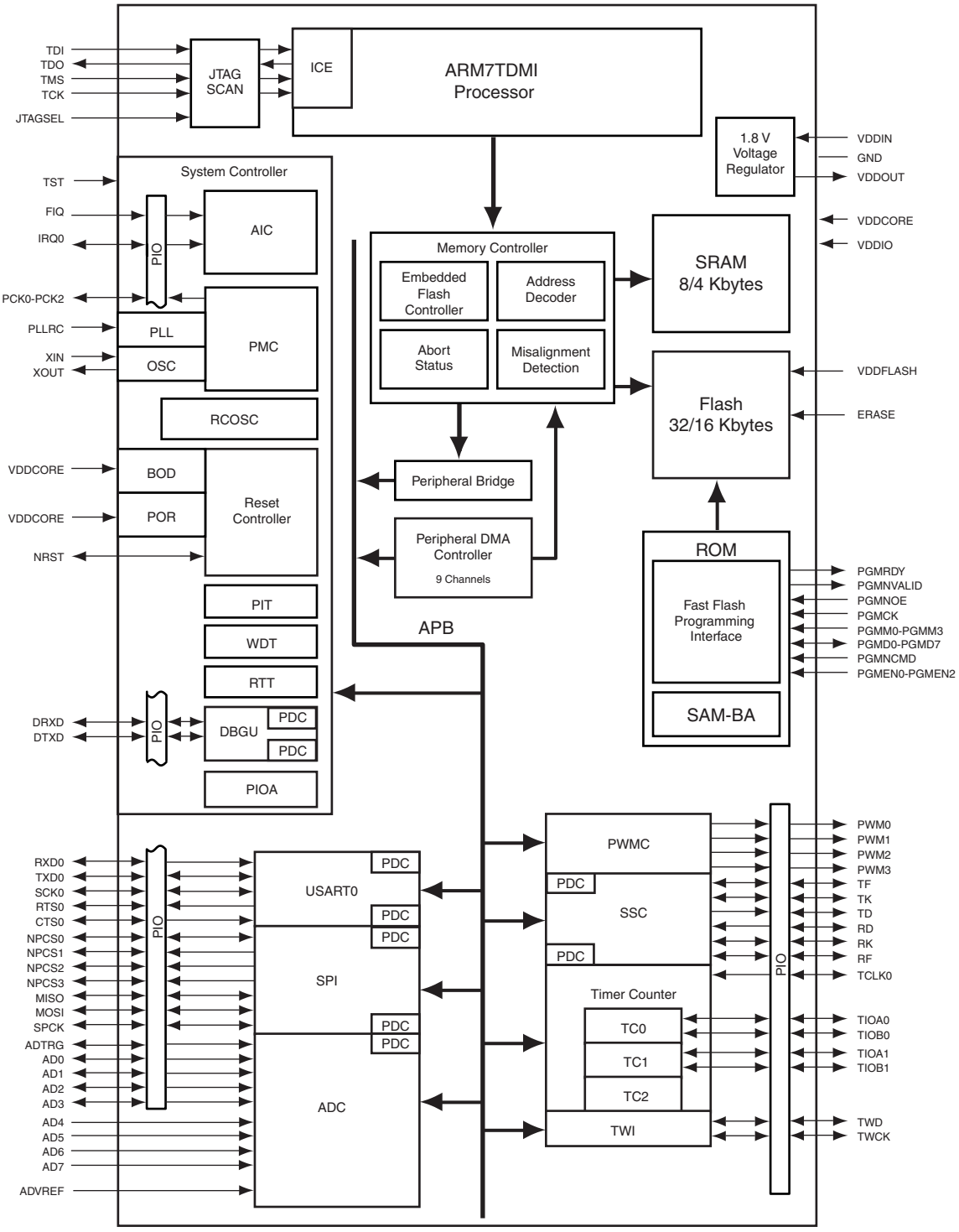


Table 3-1. Signal Description List (Continued)

DDM	USB Device Port Data -	Analog		not present on SAM7S32/16
DDP	USB Device Port Data +	Analog		not present on SAM7S32/16
SCK0 - SCK1	Serial Clock	I/O		SCK1 not present on SAM7S32/16
TXD0 - TXD1	Transmit Data	I/O		TXD1 not present on SAM7S32/16
RXD0 - RXD1	Receive Data	Input		RXD1 not present on SAM7S32/16
RTS0 - RTS1	Request To Send	Output		RTS1 not present on SAM7S32/16
CTS0 - CTS1	Clear To Send	Input		CTS1 not present on SAM7S32/16
DCD1	Data Carrier Detect	Input		not present on SAM7S32/16
DTR1	Data Terminal Ready	Output		not present on SAM7S32/16
DSR1	Data Set Ready	Input		not present on SAM7S32/16
RI1	Ring Indicator	Input		not present on SAM7S32/16
TD	Transmit Data	Output		
RD	Receive Data	Input		
TK	Transmit Clock	I/O		
RK	Receive Clock	I/O		
TF	Transmit Frame Sync	I/O		
RF	Receive Frame Sync	I/O		
TCLK0 - TCLK2	External Clock Inputs	Input		TCLK1 and TCLK2 not present on SAM7S32/16
TIOA0 - TIOA2	I/O Line A	I/O		TIOA2 not present on SAM7S32/16
TIOB0 - TIOB2	I/O Line B	I/O		TIOB2 not present on SAM7S32/16
PWM0 - PWM3	PWM Channels	Output		
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
SPCK	SPI Serial Clock	I/O		
NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
NPCS1-NPCS3	SPI Peripheral Chip Select 1 to 3	Output	Low	

4. Package and Pinout

The SAM7S512/256/128/64/321 are available in a 64-lead LQFP or 64-pad QFN package.

The SAM7S161 is available in a 64-Lead LQFP package.

The SAM7S32/16 are available in a 48-lead LQFP or 48-pad QFN package.

4.1 64-lead LQFP and 64-pad QFN Package Outlines

Figure 4-1 and Figure 4-2 show the orientation of the 64-lead LQFP and the 64-pad QFN package. A detailed mechanical description is given in the section Mechanical Characteristics of the full datasheet.

Figure 4-1. 64-lead LQFP Package (Top View)

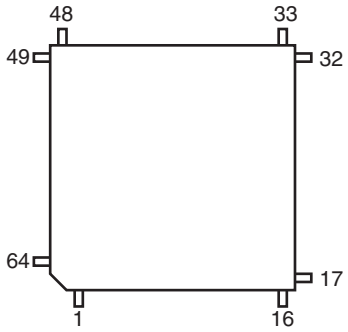
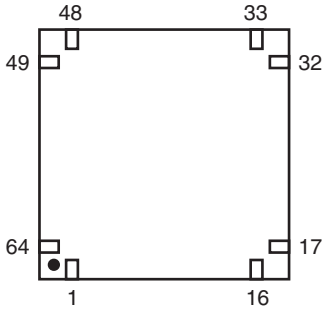


Figure 4-2. 64-pad QFN Package (Top View)



4.2 64-lead LQFP and 64-pad QFN Pinout

Table 4-1. SAM7S512/256/128/64/321/161 Pinout[1]

1	ADVREF	17	GND	33	TDI	49	TDO
2	GND	18	VDDIO	34	PA6/PGMNOE	50	JTAGSEL
3	AD4	19	PA16/PGMD4	35	PA5/PGMRDY	51	TMS
4	AD5	20	PA15/PGMD3	36	PA4/PGMNCMD	52	PA31
5	AD6	21	PA14/PGMD2	37	PA27/PGMD15	53	TCK
6	AD7	22	PA13/PGMD1	38	PA28	54	VDDCORE
7	VDDIN	23	PA24/PGMD12	39	NRST	55	ERASE
8	VDDOUT	24	VDDCORE	40	TST	56	DDM
9	PA17/PGMD5/AD0	25	PA25/PGMD13	41	PA29	57	DDP
10	PA18/PGMD6/AD1	26	PA26/PGMD14	42	PA30	58	VDDIO
11	PA21/PGMD9	27	PA12/PGMD0	43	PA3	59	VDDFLASH
12	VDDCORE	28	PA11/PGMM3	44	PA2/PGMEN2	60	GND
13	PA19/PGMD7/AD2	29	PA10/PGMM2	45	VDDIO	61	XOUT
14	PA22/PGMD10	30	PA9/PGMM1	46	GND	62	XIN/PGMCK
15	PA23/PGMD11	31	PA8/PGMM0	47	PA1/PGMEN1	63	PLLRC
16	PA20/PGMD8/AD3	32	PA7/PGMNVALID	48	PA0/PGMEN0	64	VDDPLL

Note: 1. The bottom pad of the QFN package must be connected to ground.

- Fast access time, 30 MHz single-cycle access in Worst Case conditions
- Page programming time: 6 ms, including page auto-erase
- Page programming without auto-erase: 3 ms
- Full chip erase time: 15 ms
- 10,000 write cycles, 10-year data retention capability
- 16 lock bits, protecting 16 sectors of 32 pages
- Protection Mode to secure contents of the Flash

- 16 Kbytes of Fast SRAM
  - Single-cycle access at full speed

8.5 SAM7S321/32

- 32 Kbytes of Flash Memory, single plane
  - 256 pages of 128 bytes
  - Fast access time, 30 MHz single-cycle access in Worst Case conditions
  - Page programming time: 6 ms, including page auto-erase
  - Page programming without auto-erase: 3 ms
  - Full chip erase time: 15 ms
  - 10,000 write cycles, 10-year data retention capability
  - z

8.7 Memory Mapping

8.7.1 Internal SRAM

- The SAM7S512 embeds a high-speed 64-Kbyte SRAM bank.
- The SAM7S256 embeds a high-speed 64-Kbyte SRAM bank.
- The SAM7S128 embeds a high-speed 32-Kbyte SRAM bank.
- The SAM7S64 embeds a high-speed 16-Kbyte SRAM bank.
- The SAM7S321 embeds a high-speed 8-Kbyte SRAM bank.
- The SAM7S32 embeds a high-speed 8-Kbyte SRAM bank.
- The SAM7S161 embeds a high-speed 4-Kbyte SRAM bank.
- The SAM7S16 embeds a high-speed 4-Kbyte SRAM bank

After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x0020 0000. After Remap, the SRAM also becomes available at address 0x0.

8.7.2 Internal ROM

The SAM7S Series embeds an Internal ROM. The ROM contains the FFPI and the SAM-BA program.

The internal ROM is not mapped by default.

8.7.3 Internal Flash

- The SAM7S512 features two contiguous banks (dual plane) of 256 Kbytes of Flash.
- The SAM7S256 features one bank (single plane) of 256 Kbytes of Flash.
- The SAM7S128 features one bank (single plane) of 128 Kbytes of Flash.
- The SAM7S64 features one bank (single plane) of 64 Kbytes of Flash.
- The SAM7S321/32 features one bank (single plane) of 32 Kbytes of Flash.
- The SAM7S161/16 features one bank (single plane) of 16 Kbytes of Flash.

At any time, the Flash is mapped to address 0x0010 0000. It is also accessible at address 0x0 after the reset and before the Remap Command.

Figure 8-2. Internal Memory Mapping

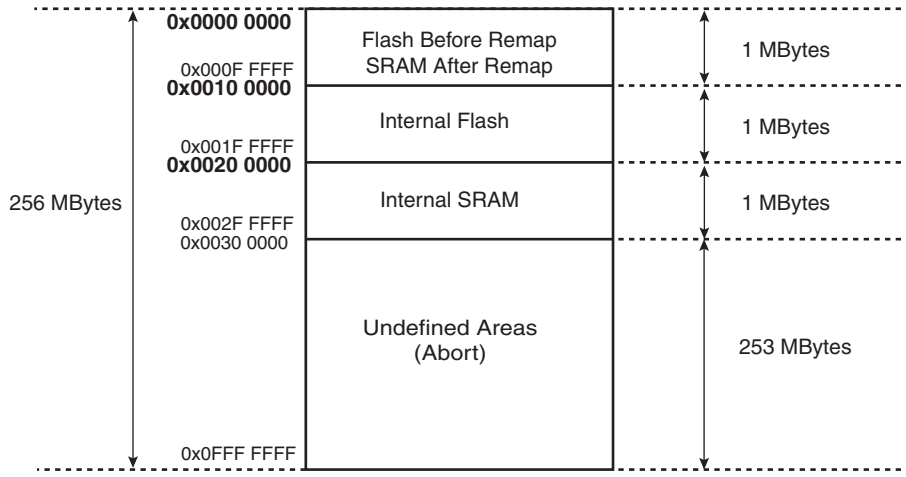
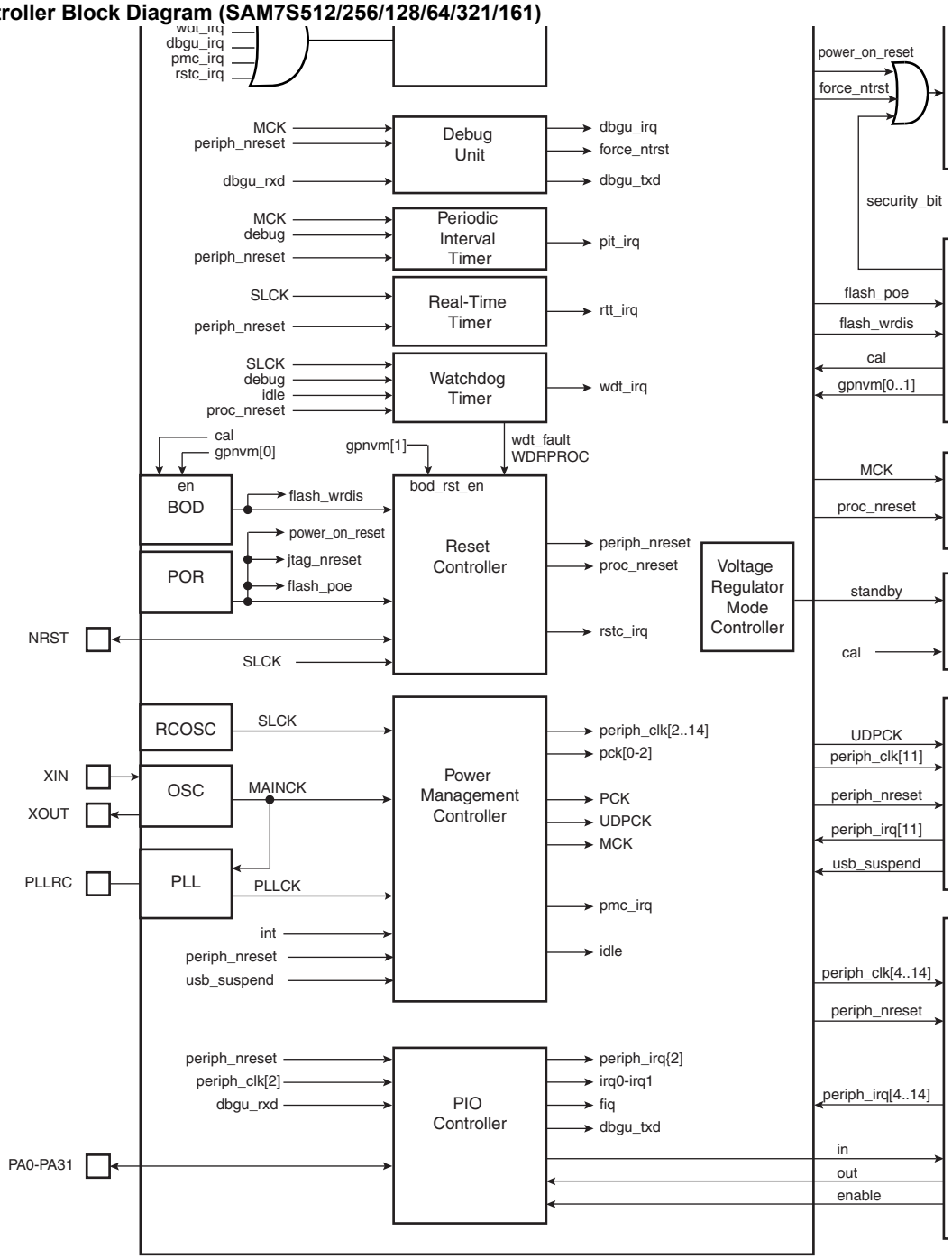


Figure 9-1. System Controller Block Diagram (SAM7S512/256/128/64/321/161)



- One set of Chip ID Registers
- One Interface providing ICE Access Prevention

- Two-pin UART
  - Implemented features are compatible with the USART
  - Programmable Baud Rate Generator
  - Parity, Framing and Overrun Error
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
- Debug Communication Channel Support
  - Offers visibility of COMMRX and COMMTX signals from the ARM Processor
- Chip ID Registers
  - Identification of the device revision, sizes of the embedded memories, set of peripherals
  - Chip ID is 0x270B0A40 for AT91SAM7S512 Rev A
  - Chip ID is 0x270B0A4F for AT91SAM7S512 Rev B
  - Chip ID is 0x270D0940 for AT91SAM7S256 Rev A
  - Chip ID is 0x270B0941 for AT91SAM7S256 Rev B
  - Chip ID is 0x270B0942 for AT91SAM7S256 Rev C
  - Chip ID is TBD for AT91SAM7S256 Rev D
  - Chip ID is 0x270C0740 for AT91SAM7S128 Rev A
  - Chip ID is 0x270A0741 for AT91SAM7S128 Rev B
  - Chip ID is 0x270A0742 for AT91SAM7S128 Rev C
  - Chip ID is TBD for AT91SAM7S128 Rev D
  - Chip ID is 0x27090540 for AT91SAM7S64 Rev A
  - Chip ID is 0x27090543 for AT91SAM7S64 Rev B
  - Chip ID is 0x27090544 for AT91SAM7S64 Rev C
  - Chip ID is 0x27080342 for AT91SAM7S321 Rev A
  - Chip ID is 0x27080340 for AT91SAM7S32 Rev A
  - Chip ID is 0x27080341 for AT91SAM7S32 Rev B
  - Chip ID is 0x27050241 for AT9SAM7S161 Rev A
  - Chip ID is 0x27050240 for AT91SAM7S16 Rev A

Note: Refer to the errata section of the datasheet for updates on chip ID.

9.6 Periodic Interval Timer

- 20-bit programmable counter plus 12-bit interval counter

9.7 Watchdog Timer

- 12-bit key-protected Programmable Counter running on prescaled SCLK
- Provides reset or interrupt signals to the system
- Counter may be stopped while the processor is in debug state or in idle mode

9.8 Real-time Timer

- 32-bit free-running counter with alarm running on prescaled SCLK
- Programmable 16-bit prescaler for SLCK accuracy compensation

9.9 PIO Controller

- One PIO Controller, controlling 32 I/O lines (21 for SAM7S32/16)
- Fully programmable through set/clear registers
- Multiplexing of two peripheral functions per I/O line
- For each I/O line (whether assigned to a peripheral or used as general-purpose I/O)
  - Input change interrupt
  - Half a clock period glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull-up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

9.10 Voltage Regulator Controller

The aim of this controller is to select the Power Mode of the Voltage Regulator between Normal Mode (bit 0 is cleared) or Standby Mode (bit 0 is set).

10.4 PIO Controller A Multiplexing

Table 10-3. Multiplexing on PIO Controller A (SAM7S512/256/128/64/321/161)

PA0	PWM0	TIOA0	High-Drive		
PA1	PWM1	TIOB0	High-Drive		
PA2	PWM2	SCK0	High-Drive		
PA3	TWD	NPCS3	High-Drive		
PA4	TWCK	TCLK0			
PA5	RXD0	NPCS3			
PA6	TXD0	PCK0			
PA7	RTS0	PWM3			
PA8	CTS0	ADTRG			
PA9	DRXD	NPCS1			
PA10	DTXD	NPCS2			
PA11	NPCS0	PWM0			
PA12	MISO	PWM1			
PA13	MOSI	PWM2			
PA14	SPCK	PWM3			
PA15	TF	TIOA1			
PA16	TK	TIOB1			
PA17	TD	PCK1	AD0		
PA18	RD	PCK2	AD1		
PA19	RK	FIQ	AD2		
PA20	RF	IRQ0	AD3		
PA21	RXD1	PCK1			
PA22	TXD1	NPCS3			
PA23	SCK1	PWM0			
PA24	RTS1	PWM1			
PA25	CTS1	PWM2			
PA26	DCD1	TIOA2			
PA27	DTR1	TIOB2			
PA28	DSR1	TCLK1			
PA29	RI1	TCLK2			
PA30	IRQ1	NPCS2			
PA31	NPCS1	PCK2			

10.8 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.9 Timer Counter

- Three 16-bit Timer Counter Channels
  - Two output compare or one input capture per channel (except for SAM7S32/16 which have only two channels connected to the PIO)
- Wide range of functions including:
  - Frequency measurement
  - Event counting
  - Interval measurement
  - Pulse generation
  - Delay timing
  - Pulse Width Modulation
  - Up/down capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs (The SAM7S32/16 have one)
  - Five internal clock inputs, as defined in Table 10-5

Table 10-5. Timer Counter Clocks Assignment

TIMER_CLOCK1	MCK/2
TIMER_CLOCK2	MCK/8
TIMER_CLOCK3	MCK/32
TIMER_CLOCK4	MCK/128
TIMER_CLOCK5	MCK/1024

  - Two multi-purpose input/output signals
  - Two global registers that act on all three TC channels

10.10 PWM Controller

- Four channels, one 16-bit counter per channel
- Common clock generator, providing thirteen different clocks
  - One Modulo n counter providing eleven clocks
  - Two independent linear dividers working on modulo n counter outputs
- Independent channel programming
  - Independent enable/disable commands
  - Independent clock selection
  - Independent period and duty cycle, with double buffering
  - Programmable selection of the output waveform polarity

Table 11-2. 64-lead LQFP Package Dimensions (in mm)

Symbol						
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.383 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.383 BSC		
R2	0.08	–	0.20	0.003	–	0.008
R1	0.08	–	–	0.003	–	–
q	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	–	–	0°	–	–
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	7.50			0.285		
E2	7.50			0.285		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Table 11-3. 48-pad QFN Package Dimensions (in mm)

Symbol						
A	–	–	090	–	–	0.035
A1	–	–	0.050	–	–	0.002
A2	–	0.65	0.70	–	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.18	0.20	0.23	0.007	0.008	0.009
D	7.00 bsc			0.276 bsc		
D2	5.45	5.60	5.75	0.215	0.220	0.226
E	7.00 bsc			0.276 bsc		
E2	5.45	5.60	5.75	0.215	0.220	0.226
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 bsc			0.020 bsc		
R	0.09	–	–	0.004	–	–
Tolerances of Form and Position						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

12. SAM7S Ordering Information

Table 12-1. SAM7S Series Ordering Information

MLR A Ordering Code	MLR B Ordering Code	MLR C Ordering Code	MLR D Ordering Code	Package	Package Type	Temperature Operating Range
AT91SAM7S16-AU AT91SAM7S16-MU	–	–	–	LQFP 48 QFN 48	Green	Industrial (-40· C to 85· C)
AT91SAM7S161-AU	–	–	–	LQFP 64	Green	Industrial (-40· C to 85· C)
AT91SAM7S32-AU-001 AT91SAM7S32-MU	AT91SAM7S32B-AU AT91SAM7S32B-MU			LQFP 48 QFN 48	Green	Industrial (-40· C to 85· C)
AT91SAM7S321-AU AT91SAM7S321-MU	–	–	–	LQFP 64 QFN 64	Green	Industrial (-40· C to 85· C)
–	AT91SAM7S64B-AU AT91SAM7S64B-MU	AT91SAM7S64C-AU AT91SAM7S64C-MU	–	LQFP 64 QFN 64	Green	Industrial (-40· C to 85· C)
–	AT91SAM7S128-AU-001 AT91SAM7S128-MU	AT91SAM7S128C-AU AT91SAM7S128C-MU	AT91SAM7S128D-AU AT91SAM7S128D-MU	LQFP 64 QFN 64	Green	Industrial (-40· C to 85· C)
–	AT91SAM7S256-AU-001 AT91SAM7S256-MU	AT91SAM7S256C-AU AT91SAM7S256C-MU	AT91SAM7S256D-AU AT91SAM7S256D-MU	LQFP 64 QFN 64	Green	Industrial (-40· C to 85· C)
AT91SAM7S512-AU AT91SAM7S512-MU	AT91SAM7S512B-AU AT91SAM7S512B-MU	–	–	LQFP 64 QFN 64	Green	Industrial (-40· C to 85· C)

Revision History

6175AS	First issue - Unqualified on Intranet Corresponds to 6175A full datasheet approval loop. Qualified on Intranet.	
6175BS	Section 8. “Memories” on page 18 updated: 2 ms => 3 ms, 10 ms => 15 ms, 4 ms => 6 ms	CSR05-529
6175CS	Section 12. ”SAM7S Ordering Information” AT91SAM7S321 changed in Table 12-1 on page 47	#2342
6175DS	“Features” , Table 1-1, “Configuration Summary,” on page 3, Section 4. ”Package and Pinout” Section 12. ”SAM7S Ordering Information” QFN package information added	#2444
6175ES	Section 10.11 on page 39 USB Device port, Ping-pong Mode includes Isochronous endpoints. “Features” on page 1, and global: AT91SAM7S512 added to series. Reference to Manchester Encoder removed from USART. Section 8. ”Memories” Reformatted Memories, Consolidated Memory Mapping in Figure 8-1 on page 20 Section 10. ”Peripherals” Reordered sub sections. Section 11. ”Package Drawings” QFN, LQFP package drawings added. “ice_nreset” signals changed to” power_on_reset” in System Controller block diagrams, Figure 9-1 on page 26 and Figure 9-2 on page 27. Section 4. ”Package and Pinout” LQFP and QFN Package Outlines replace Mechanical Overview. Section 10.1 ”User Interface”, User peripherals are mapped between 0xF000 0000 and 0xFFFF EFFF. SYSIRQ changed to SYSC in “Peripheral Identifiers” Table 10-1 and Table 10-2	specs #2748 #2832 (DBGU IP) rfo review
6175FS	AT91SAM7S161 and AT91SAM7S16 added to product family **Features:** Timer Counter, on page 2 product specific information rewritten, Table 1-1, “Configuration Summary,” on page 3, footnote explains TC on AT91SAM7S32/16 has only two channels accessible via PIO, and in Section 10.9 ”Timer Counter”, precisions added to “compare and capture” output/input. Section 10.6 ”Two-wire Interface”, updated reference to I^2C compatibility, internal address registers, slave addressing, Modes for AT91SAM7S161/16 “One Two-wire Interface (TWI)” on page 2, updated in Features Section 10.12 ”Analog-to-digital Converter”, updated Successive Approximation Register ADC and the INL, DNL ± values of LSB. Section 8.8.3 ”Lock Regions”, locked-region’s erase or program command updated Section 9.5 ”Debug Unit”, Chip ID updated. Section 6. ”I/O Lines Considerations”, JTAG Port Pin, Test Pin, Erase Pin, updated.	BDs 4208 rfo review 4325 5063

6175GS	“Features” ,“Debug Unit (DBGU)” updated with “Mode for General Purpose 2-wire UART Serial Communication” Section 7.4 ”Peripheral DMA Controller”, added list of PDC priorities. Section 9. ”System Controller”, Figure 9-1 and Figure 9-2 RTT is reset by “power_on_reset”. Section 9.1.1 ”Brownout Detector and Power-on Reset”, fourth paragraph reduced. Section 9.5 ”Debug Unit”, the list; Section I ”Chip ID Registers”, chip IDs updated, added SAM7S32 Rev B and SAM7S64 Rev B to the list. Section 12. ”SAM7S Ordering Information”, Updated product ordering information by MRL A and MRL B versions.	5846 5913 5224 5685 rfo
6175HS	Section 6.2 ”Test Pin”, added to SAM-BA Boot recovery procedure, a power cycle of the board is mandatory. Section 8.10 ”SAM-BA Boot Assistant”, added to SAM-BA Boot recovery procedure, a power cycle of the board is mandatory.	6068
6175IS	Section 9.5 ”Debug Unit”, Chip ID Registers list updated. MRL C column added to Table 12-1, “SAM7S Series Ordering Information”.	7185
6175JS	Product Series Naming Convention Except for part ordering and library references, AT91 prefix dropped from most nomenclature. AT91SAM7S becomes SAM7S. Debug Unit: “Chip ID Registers” on page 31, Chip ID is 0x270B0A4F for AT91SAM7S512 Rev B	rfo 7945
6175KS	Section 9.5 ”Debug Unit”, Chip ID Registers list updated. Added Chip ID for SAM7S128 Rev D and SAM7S256 Rev D Table 12-1, “SAM7S Series Ordering Information”.Added SAM7S128 Rev D and SAM7S256 Rev D	8380/8467