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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	I²C, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	32
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at91sam7s512-mu-999

- **Debug Unit (DBGU)**
 - 2-wire UART and Support for Debug Communication Channel interrupt, Programmable ICE Access Prevention
 - Mode for General Purpose 2-wire UART Serial Communication
- **Periodic Interval Timer (PIT)**
 - 20-bit Programmable Counter plus 12-bit Interval Counter
- **Windowed Watchdog (WDT)**
 - 12-bit key-protected Programmable Counter
 - Provides Reset or Interrupt Signals to the System
 - Counter May Be Stopped While the Processor is in Debug State or in Idle Mode
- **Real-time Timer (RTT)**
 - 32-bit Free-running Counter with Alarm
 - Runs Off the Internal RC Oscillator
- **One Parallel Input/Output Controller (PIOA)**
 - Thirty-two (SAM7S512/256/128/64/321/161) or twenty-one (SAM7S32/16) Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
 - Input Change Interrupt Capability on Each I/O Line
 - Individually Programmable Open-drain, Pull-up resistor and Synchronous Output
- **Eleven (SAM7S512/256/128/64/321/161) or Nine (SAM7S32/16) Peripheral DMA Controller (PDC) Channels**
- **One USB 2.0 Full Speed (12 Mbits per Second) Device Port (Except for the SAM7S32/16).**
 - On-chip Transceiver, 328-byte Configurable Integrated FIFOs
- **One Synchronous Serial Controller (SSC)**
 - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
 - I²S Analog Interface Support, Time Division Multiplex Support
 - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- **Two (SAM7S512/256/128/64/321/161) or One (SAM7S32/16) Universal Synchronous/Asynchronous Receiver Transmitters (USART)**
 - Individual Baud Rate Generator, IrDA[®] Infrared Modulation/Demodulation
 - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
 - Full Modem Line Support on USART1 (SAM7S512/256/128/64/321/161)
- **One Master/Slave Serial Peripheral Interface (SPI)**
 - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- **One Three-channel 16-bit Timer/Counter (TC)**
 - Three External Clock Input and Two Multi-purpose I/O Pins per Channel (SAM7S512/256/128/64/321/161)
 - One External Clock Input and Two Multi-purpose I/O Pins for the first Two Channels Only (SAM7S32/16)
 - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- **One Four-channel 16-bit PWM Controller (PWMC)**
- **One Two-wire Interface (TWI)**
 - Master Mode Support Only, All Two-wire Atmel EEPROMs and I²C Compatible Devices Supported (SAM7S512/256/128/64/321/32)
 - Master, Multi-Master and Slave Mode Support, All Two-wire Atmel EEPROMs and I²C Compatible Devices Supported (SAM7S161/16)
- **One 8-channel 10-bit Analog-to-Digital Converter, Four Channels Multiplexed with Digital I/Os**
- **SAM-BA[™] Boot Assistant**
 - Default Boot program
 - Interface with SAM-BA Graphic User Interface
- **IEEE[®] 1149.1 JTAG Boundary Scan on All Digital Pins**
- **5V-tolerant I/Os, including Four High-current Drive I/O lines, Up to 16 mA Each (SAM7S161/16 I/Os Not 5V-tolerant)**
- **Power Supplies**
 - Embedded 1.8V Regulator, Drawing up to 100 mA for the Core and External Components
 - 3.3V or 1.8V VDDIO I/O Lines Power Supply, Independent 3.3V VDDFLASH Flash Power Supply
 - 1.8V VDDCORE Core Power Supply with Brown-out Detector

3. Signal Description

Table 3-1. Signal Description List

VDDIN	Voltage and ADC Regulator Power Supply Input	Power		3.0 to 3.6V
VDDOUT	Voltage Regulator Output	Power		1.85V nominal
VDDFLASH	Flash Power Supply	Power		3.0V to 3.6V
VDDIO	I/O Lines Power Supply	Power		3.0V to 3.6V or 1.65V to 1.95V
VDDCORE	Core Power Supply	Power		1.65V to 1.95V
VDDPLL	PLL	Power		1.65V to 1.95V
GND	Ground	Ground		
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
PLLRC	PLL Filter	Input		
PCK0 - PCK2	Programmable Clock Output	Output		
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor
JTAGSEL	JTAG Selection	Input		Pull-down resistor ⁽¹⁾
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	Pull-down resistor ⁽¹⁾
NRST	Microcontroller Reset	I/O	Low	Open-drain with pull-Up resistor
TST	Test Mode Select	Input	High	Pull-down resistor ⁽¹⁾
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
IRQ0 - IRQ1	External Interrupt Inputs	Input		IRQ1 not present on SAM7S32/16
FIQ	Fast Interrupt Input	Input		
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset PA0 - PA20 only on SAM7S32/16

Table 3-1. Signal Description List (Continued)

TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		
AD0-AD3	Analog Inputs	Analog		Digital pulled-up inputs at reset
AD4-AD7	Analog Inputs	Analog		Analog Inputs
ADTRG	ADC Trigger	Input		
ADVREF	ADC Reference	Analog		
PGMEN0-PGMEN2	Programming Enabling	Input		
PGMM0-PGMM3	Programming Mode	Input		
PGMD0-PGMD15	Programming Data	I/O		PGMD0-PGMD7 only on SAM7S32/16
PGMRDY	Programming Ready	Output	High	
PGMNVALID	Data Direction	Output	Low	
PGMNOE	Programming Read	Input	Low	
PGMCK	Programming Clock	Input		
PGMNCMD	Programming Command	Input	Low	

Note: 1. Refer to [Section 6. "I/O Lines Considerations"](#) on page 14.

4.3 48-lead LQFP and 48-pad QFN Package Outlines

Figure 4-3 and Figure 4-4 show the orientation of the 48-lead LQFP and the 48-pad QFN package. A detailed mechanical description is given in the section Mechanical Characteristics of the full datasheet.

Figure 4-3. 48-lead LQFP Package (Top View)

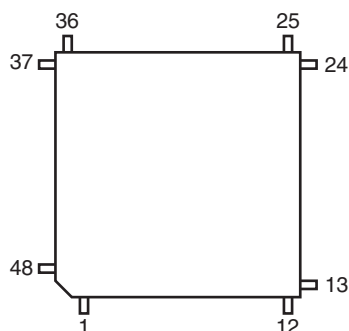
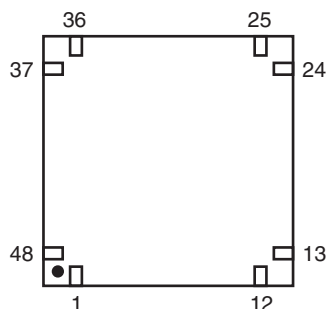


Figure 4-4. 48-pad QFN Package (Top View)



4.4 48-lead LQFP and 48-pad QFN Pinout

Table 4-2. SAM7S32/16 Pinout⁽¹⁾

1	ADVREF	13	VDDIO	25	TDI	37	TDO
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	AD4	15	PA15/PGMD3	27	PA5/PGMRDY	39	TMS
4	AD5	16	PA14/PGMD2	28	PA4/PGMNCMD	40	TCK
5	AD6	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	AD7	18	VDDCORE	30	TST	42	ERASE
7	VDDIN	19	PA12/PGMD0	31	PA3	43	VDDFLASH
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	GND
9	PA17/PGMD5/AD0	21	PA10/PGMM2	33	VDDIO	45	XOUT
10	PA18/PGMD6/AD1	22	PA9/PGMM1	34	GND	46	XIN/PGMCK
11	PA19/PGMD7/AD2	23	PA8/PGMM0	35	PA1/PGMEN1	47	PLLRC
12	PA20/AD3	24	PA7/PGMNVALID	36	PA0/PGMEN0	48	VDDPLL

Note: 1. The bottom pad of the QFN package must be connected to ground.

7. Processor and Architecture

7.1 ARM7TDMI Processor

- RISC processor based on ARMv4T Von Neumann architecture
 - Runs at up to 55 MHz, providing 0.9 MIPS/MHz
- Two instruction sets
 - ARM® high-performance 32-bit instruction set
 - Thumb® high code density 16-bit instruction set
- Three-stage pipeline architecture
 - Instruction Fetch (F)
 - Instruction Decode (D)
 - Execute (E)

7.2 Debug and Test Features

- Integrated EmbeddedICE™ (embedded in-circuit emulator)
 - Two watchpoint units
 - Test access port accessible through a JTAG protocol
 - Debug communication channel
- Debug Unit
 - Two-pin UART
 - Debug communication channel interrupt handling
 - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on all digital pins

7.3 Memory Controller

- Bus Arbiter
 - Handles requests from the ARM7TDMI and the Peripheral DMA Controller
- Address decoder provides selection signals for
 - Three internal 1 Mbyte memory areas
 - One 256 Mbyte embedded peripheral area
- Abort Status Registers
 - Source, Type and all parameters of the access leading to an abort are saved
 - Facilitates debug by detection of bad pointers
- Misalignment Detector
 - Alignment checking of all data accesses
 - Abort generation in case of misalignment
- Remap Command
 - Remaps the SRAM in place of the embedded non-volatile memory
 - Allows handling of dynamic exception vectors
- Embedded Flash Controller
 - Embedded Flash interface, up to three programmable wait states
 - Prefetch buffer, buffering and anticipating the 16-bit requests, reducing the required wait states
 - Key-protected program, erase and lock/unlock sequencer
 - Single command for erasing, programming and locking operations
 - Interrupt generation in case of forbidden operation

8. Memories

8.1 SAM7S512

- 512 Kbytes of Flash Memory, dual plane
 - 2 contiguous banks of 1024 pages of 256 bytes
 - Fast access time, 30 MHz single-cycle access in Worst Case conditions
 - Page programming time: 6 ms, including page auto-erase
 - Page programming without auto-erase: 3 ms
 - Full chip erase time: 15 ms
 - 10,000 write cycles, 10-year data retention capability
 - 32 lock bits, protecting 32 sectors of 64 pages
 - Protection Mode to secure contents of the Flash
- 64 Kbytes of Fast SRAM
 - Single-cycle access at full speed

8.2 SAM7S256

- 256 Kbytes of Flash Memory, single plane
 - 1024 pages of 256 bytes
 - Fast access time, 30 MHz single-cycle access in Worst Case conditions
 - Page programming time: 6 ms, including page auto-erase
 - Page programming without auto-erase: 3 ms
 - Full chip erase time: 15 ms
 - 10,000 write cycles, 10-year data retention capability
 - 16 lock bits, protecting 16 sectors of 64 pages
 - Protection Mode to secure contents of the Flash
- 64 Kbytes of Fast SRAM
 - Single-cycle access at full speed

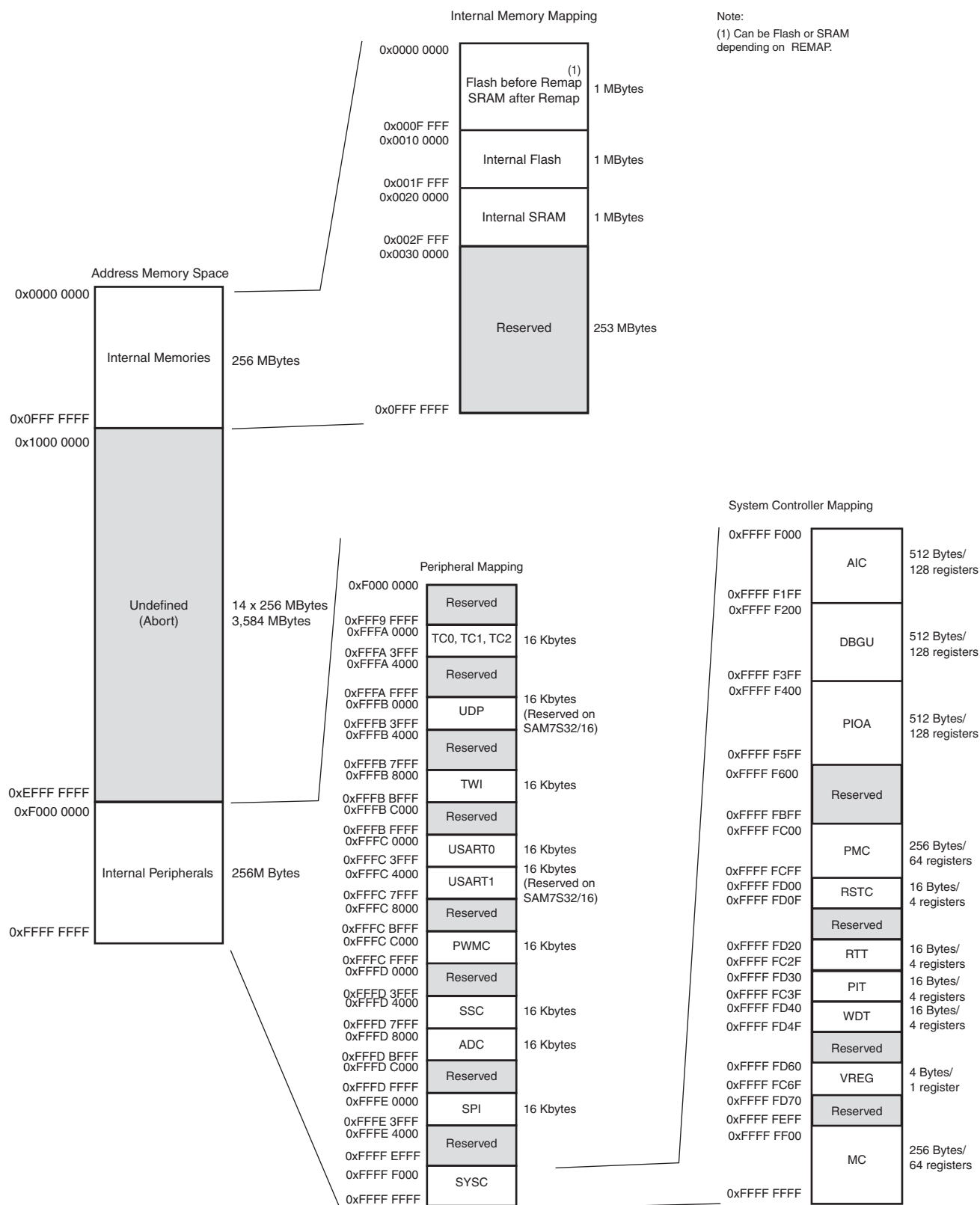
8.3 SAM7S128

- 128 Kbytes of Flash Memory, single plane
 - 512 pages of 256 bytes
 - Fast access time, 30 MHz single-cycle access in Worst Case conditions
 - Page programming time: 6 ms, including page auto-erase
 - Page programming without auto-erase: 3 ms
 - Full chip erase time: 15 ms
 - 10,000 write cycles, 10-year data retention capability
 - 8 lock bits, protecting 8 sectors of 64 pages
 - Protection Mode to secure contents of the Flash
- 32 Kbytes of Fast SRAM
 - Single-cycle access at full speed

8.4 SAM7S64

- 64 Kbytes of Flash Memory, single plane
 - 512 pages of 128 bytes

Figure 8-1. SAM SAM7S512/256/128/64/321/32/161/16 Memory Mapping



8.8.3 Lock Regions

8.8.3.1 SAM7S512

Two Embedded Flash Controllers each manage 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S512 contains 32 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 16 NVM bits (or 32 NVM bits) are software programmable through the corresponding EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.2 SAM7S256

The Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S256 contains 16 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 16 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.3 SAM7S128

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S128 contains 8 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 8 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.4 SAM7S64

The Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S64 contains 16 lock regions and each lock region contains 32 pages of 128 bytes. Each lock region has a size of 4 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 16 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.5 SAM7S321/32

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S321/32 contains 8 lock regions and each lock region contains 32 pages of 128 bytes. Each lock region has a size of 4 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 8 NVM bits are software programmable through the EFC User Interface. The command “Set Lock Bit” enables the protection. The command “Clear Lock Bit” unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.6 SAM7S161/16

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S161/16 contains 8 lock regions and each lock region contains 32 pages of 64 bytes. Each lock region has a size of 2 Kbytes.

If a locked-region’s erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 8 NVM bits are software programmable through the EFC User Interface. The command “Set Lock Bit” enables the protection. The command “Clear Lock Bit” unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

Table 8-1 summarizes the configuration of the eight devices.

Table 8-1. Flash Configuration Summary

SAM7S512	32	64	256 bytes
SAM7S256	16	64	256 bytes
SAM7S128	8	64	256 bytes
SAM7S64	16	32	128 bytes
SAM7S321/32	8	32	128 bytes
SAM7S161/16	8	32	64 bytes

8.8.4 Security Bit Feature

The SAM7S Series features a security bit, based on a specific NVM Bit. When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the Command “Set Security Bit” of the EFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full flash erase is performed. When the security bit is deactivated, all accesses to the flash are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 50 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

8.8.5 Non-volatile Brownout Detector Control

Two general purpose NVM (GPNVM) bits are used for controlling the brownout detector (BOD), so that even after a power loss, the brownout detector operations remain in their state.

These two GPNVM bits can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EFC User Interface.

- GPNVM Bit 0 is used as a brownout detector enable bit. Setting the GPNVM Bit 0 enables the BOD, clearing it disables the BOD. Asserting ERASE clears the GPNVM Bit 0 and thus disables the brownout detector by default.
- The GPNVM Bit 1 is used as a brownout reset enable signal for the reset controller. Setting the GPNVM Bit 1 enables the brownout reset when a brownout is detected, Clearing the GPNVM Bit 1 disables the brownout reset. Asserting ERASE disables the brownout reset by default.

- One set of Chip ID Registers
- One Interface providing ICE Access Prevention
- Two-pin UART
 - Implemented features are compatible with the USART
 - Programmable Baud Rate Generator
 - Parity, Framing and Overrun Error
 - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
- Debug Communication Channel Support
 - Offers visibility of COMMRX and COMMTX signals from the ARM Processor
- Chip ID Registers
 - Identification of the device revision, sizes of the embedded memories, set of peripherals
 - Chip ID is 0x270B0A40 for AT91SAM7S512 Rev A
 - Chip ID is 0x270B0A4F for AT91SAM7S512 Rev B
 - Chip ID is 0x270D0940 for AT91SAM7S256 Rev A
 - Chip ID is 0x270B0941 for AT91SAM7S256 Rev B
 - Chip ID is 0x270B0942 for AT91SAM7S256 Rev C
 - Chip ID is TBD for AT91SAM7S256 Rev D
 - Chip ID is 0x270C0740 for AT91SAM7S128 Rev A
 - Chip ID is 0x270A0741 for AT91SAM7S128 Rev B
 - Chip ID is 0x270A0742 for AT91SAM7S128 Rev C
 - Chip ID is TBD for AT91SAM7S128 Rev D
 - Chip ID is 0x27090540 for AT91SAM7S64 Rev A
 - Chip ID is 0x27090543 for AT91SAM7S64 Rev B
 - Chip ID is 0x27090544 for AT91SAM7S64 Rev C
 - Chip ID is 0x27080342 for AT91SAM7S321 Rev A
 - Chip ID is 0x27080340 for AT91SAM7S32 Rev A
 - Chip ID is 0x27080341 for AT91SAM7S32 Rev B
 - Chip ID is 0x27050241 for AT91SAM7S161 Rev A
 - Chip ID is 0x27050240 for AT91SAM7S16 Rev A

Note: Refer to the errata section of the datasheet for updates on chip ID.

9.6 Periodic Interval Timer

- 20-bit programmable counter plus 12-bit interval counter

9.7 Watchdog Timer

- 12-bit key-protected Programmable Counter running on prescaled SCLK
- Provides reset or interrupt signals to the system
- Counter may be stopped while the processor is in debug state or in idle mode

9.8 Real-time Timer

- 32-bit free-running counter with alarm running on prescaled SCLK
- Programmable 16-bit prescaler for SCLK accuracy compensation

9.9 PIO Controller

- One PIO Controller, controlling 32 I/O lines (21 for SAM7S32/16)
- Fully programmable through set/clear registers
- Multiplexing of two peripheral functions per I/O line
- For each I/O line (whether assigned to a peripheral or used as general-purpose I/O)
 - Input change interrupt
 - Half a clock period glitch filter
 - Multi-drive option enables driving in open drain
 - Programmable pull-up on each I/O line
 - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

9.10 Voltage Regulator Controller

The aim of this controller is to select the Power Mode of the Voltage Regulator between Normal Mode (bit 0 is cleared) or Standby Mode (bit 0 is set).

10. Peripherals

10.1 User Interface

The User Peripherals are mapped in the 256 MBytes of address space between 0xF000 0000 and 0xFFFF EFFF. Each peripheral is allocated 16 Kbytes of address space.

A complete memory map is provided in [Figure 8-1 on page 20](#).

10.2 Peripheral Identifiers

The SAM7S Series embeds a wide range of peripherals. [Table 10-1](#) defines the Peripheral Identifiers of the SAM7S512/256/128/64/321/161. [Table 10-2](#) defines the Peripheral Identifiers of the SAM7S32/16. A peripheral identifier is required for the control of the peripheral interrupt with the Advanced Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 10-1. Peripheral Identifiers (SAM7S512/256/128/64/321/161)

0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC ⁽¹⁾	System	
2	PIOA	Parallel I/O Controller A	
3	Reserved		
4	ADC ⁽¹⁾	Analog-to Digital Converter	
5	SPI	Serial Peripheral Interface	
6	US0	USART 0	
7	US1	USART 1	
8	SSC	Synchronous Serial Controller	
9	TWI	Two-wire Interface	
10	PWMC	PWM Controller	
11	UDP	USB Device Port	
12	TC0	Timer/Counter 0	
13	TC1	Timer/Counter 1	
14	TC2	Timer/Counter 2	
15 - 29	Reserved		
30	AIC	Advanced Interrupt Controller	IRQ0
31	AIC	Advanced Interrupt Controller	IRQ1

Note: 1. Setting SYSC and ADC bits in the clock set/clear registers of the PMC has no effect. The System Controller is continuously clocked. The ADC clock is automatically started for the first conversion. In Sleep Mode the ADC clock is automatically stopped after each conversion.

Note: 1. Setting SYSC and ADC bits in the clock set/clear registers of the PMC has no effect. The System Controller is continuously clocked. The ADC clock is automatically started for the first conversion. In Sleep Mode the ADC clock is automatically stopped after each conversion.

10.4 PIO Controller A Multiplexing

Table 10-3. Multiplexing on PIO Controller A (SAM7S512/256/128/64/321/161)

PA0	PWM0	TIOA0	High-Drive		
PA1	PWM1	TIOB0	High-Drive		
PA2	PWM2	SCK0	High-Drive		
PA3	TWD	NPCS3	High-Drive		
PA4	TWCK	TCLK0			
PA5	RXD0	NPCS3			
PA6	TXD0	PCK0			
PA7	RTS0	PWM3			
PA8	CTS0	ADTRG			
PA9	DRXD	NPCS1			
PA10	DTXD	NPCS2			
PA11	NPCS0	PWM0			
PA12	MISO	PWM1			
PA13	MOSI	PWM2			
PA14	SPCK	PWM3			
PA15	TF	TIOA1			
PA16	TK	TIOB1			
PA17	TD	PCK1	AD0		
PA18	RD	PCK2	AD1		
PA19	RK	FIQ	AD2		
PA20	RF	IRQ0	AD3		
PA21	RXD1	PCK1			
PA22	TXD1	NPCS3			
PA23	SCK1	PWM0			
PA24	RTS1	PWM1			
PA25	CTS1	PWM2			
PA26	DCD1	TIOA2			
PA27	DTR1	TIOB2			
PA28	DSR1	TCLK1			
PA29	RI1	TCLK2			
PA30	IRQ1	NPCS2			
PA31	NPCS1	PCK2			

- Programmable center or left aligned output waveform

10.11 USB Device Port (Does not pertain to SAM7S32/16)

- USB V2.0 full-speed compliant, 12 Mbits per second.
- Embedded USB V2.0 full-speed transceiver
- Embedded 328-byte dual-port RAM for endpoints
- Four endpoints
 - Endpoint 0: 8 bytes
 - Endpoint 1 and 2: 64 bytes ping-pong
 - Endpoint 3: 64 bytes
 - Ping-pong Mode (two memory banks) for isochronous and bulk endpoints
- Suspend/resume logic

10.12 Analog-to-digital Converter

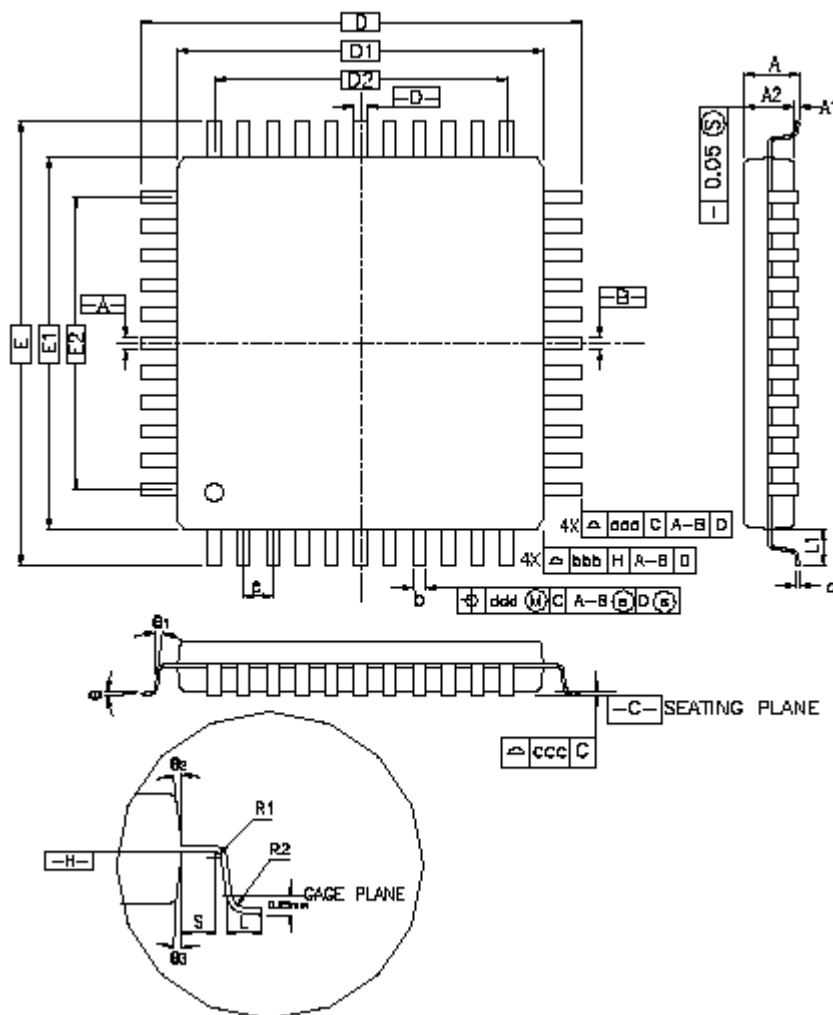
- 8-channel ADC
- 10-bit 384 Ksamples/sec. or 8-bit 583 Ksamples/sec. Successive Approximation Register ADC
- ± 2 LSB Integral Non Linearity, ± 1 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger source
 - Hardware or software trigger
 - External trigger pin
 - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer
 - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels
- Four of eight analog inputs shared with digital signals

11. Package Drawings

The SAM7S series devices are available in LQFP and QFN package types.

11.1 LQFP Packages

Figure 11-1. 48-and 64-lead LQFP Package Drawing



11.2 QFN Packages

Figure 11-2. 48-pad QFN Package

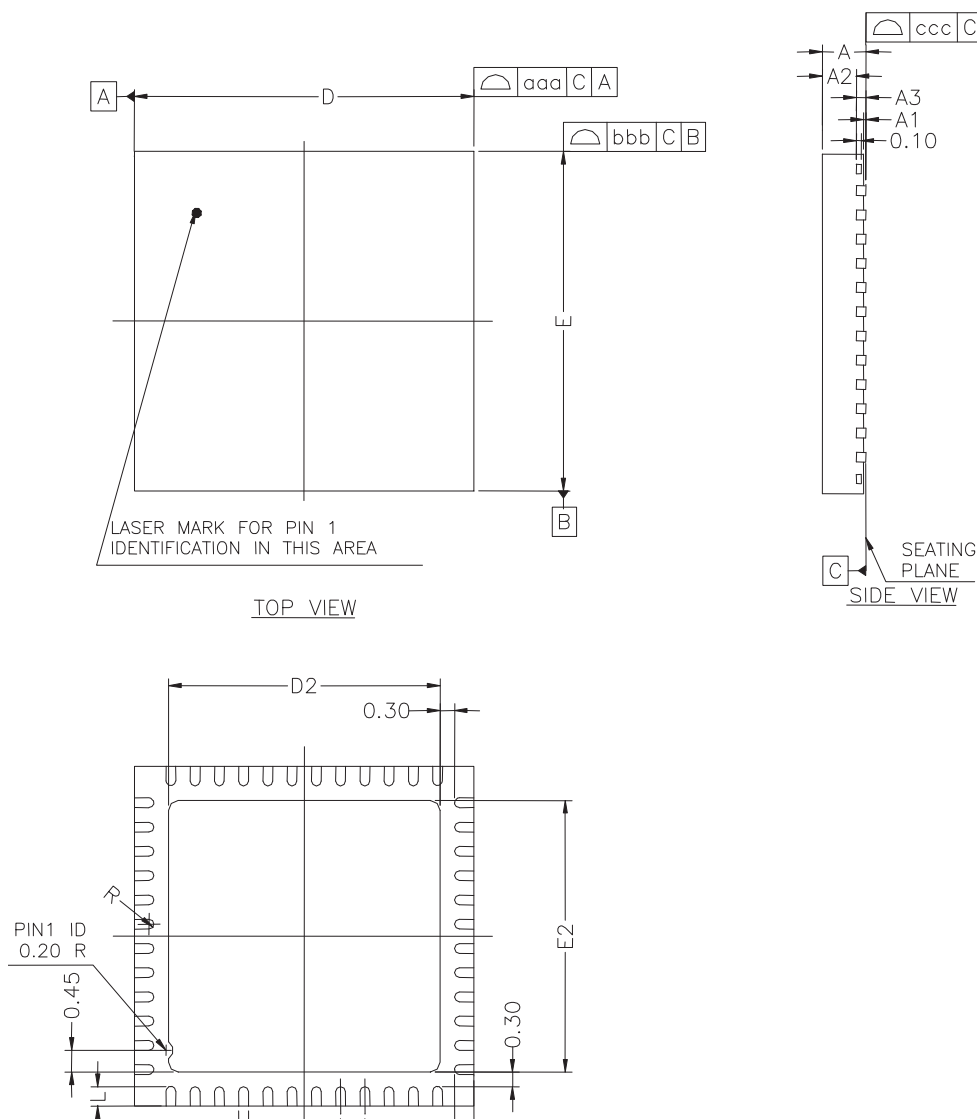


Table 11-4. 64-pad QFN Package Dimensions (in mm)

Symbol						
A	–	–	090	–	–	0.035
A1	–	–	0.05	–	–	0.001
A2	–	0.65	0.70	–	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.23	0.25	0.28	0.009	0.010	0.011
D	9.00 bsc			0.354 bsc		
D2	6.95	7.10	7.25	0.274	0.280	0.285
E	9.00 bsc			0.354 bsc		
E2	6.95	7.10	7.25	0.274	0.280	0.285
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 bsc			0.020 bsc		
R	0.125	–	–	0.0005	–	–
Tolerances of Form and Position						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

12. SAM7S Ordering Information

Table 12-1. SAM7S Series Ordering Information

MLR A Ordering Code	MLR B Ordering Code	MLR C Ordering Code	MLR D Ordering Code	Package	Package Type	Temperature Operating Range
AT91SAM7S16-AU AT91SAM7S16-MU	–	–	–	LQFP 48 QFN 48	Green	Industrial (-40° C to 85° C)
AT91SAM7S161-AU	–	–	–	LQFP 64	Green	Industrial (-40° C to 85° C)
AT91SAM7S32-AU-001 AT91SAM7S32-MU	AT91SAM7S32B-AU AT91SAM7S32B-MU			LQFP 48 QFN 48	Green	Industrial (-40° C to 85° C)
AT91SAM7S321-AU AT91SAM7S321-MU	–	–	–	LQFP 64 QFN 64	Green	Industrial (-40° C to 85° C)
–	AT91SAM7S64B-AU AT91SAM7S64B-MU	AT91SAM7S64C-AU AT91SAM7S64C-MU	–	LQFP 64 QFN 64	Green	Industrial (-40° C to 85° C)
–	AT91SAM7S128-AU-001 AT91SAM7S128-MU	AT91SAM7S128C-AU AT91SAM7S128C-MU	AT91SAM7S128D-AU AT91SAM7S128D-MU	LQFP 64 QFN 64	Green	Industrial (-40° C to 85° C)
–	AT91SAM7S256-AU-001 AT91SAM7S256-MU	AT91SAM7S256C-AU AT91SAM7S256C-MU	AT91SAM7S256D-AU AT91SAM7S256D-MU	LQFP 64 QFN 64	Green	Industrial (-40° C to 85° C)
AT91SAM7S512-AU AT91SAM7S512-MU	AT91SAM7S512B-AU AT91SAM7S512B-MU	–	–	LQFP 64 QFN 64	Green	Industrial (-40° C to 85° C)

Revision History

6175AS	First issue - Unqualified on Intranet Corresponds to 6175A full datasheet approval loop. Qualified on Intranet.	
6175BS	Section 8. "Memories" on page 18 updated: 2 ms => 3 ms, 10 ms => 15 ms, 4 ms => 6 ms	CSR05-529
6175CS	Section 12. "SAM7S Ordering Information" AT91SAM7S321 changed in Table 12-1 on page 47	#2342
6175DS	"Features" , Table 1-1, "Configuration Summary," on page 3 , Section 4. "Package and Pinout" Section 12. "SAM7S Ordering Information" QFN package information added	#2444
6175ES	Section 10.11 on page 39 USB Device port, Ping-pong Mode includes Isochronous endpoints. "Features" on page 1 , and global: AT91SAM7S512 added to series. Reference to Manchester Encoder removed from USART. Section 8. "Memories" Reformatted Memories, Consolidated Memory Mapping in Figure 8-1 on page 20 Section 10. "Peripherals" Reordered sub sections. Section 11. "Package Drawings" QFN, LQFP package drawings added. "ice_nreset" signals changed to "power_on_reset" in System Controller block diagrams, Figure 9-1 on page 26 and Figure 9-2 on page 27 . Section 4. "Package and Pinout" LQFP and QFN Package Outlines replace Mechanical Overview. Section 10.1 "User Interface" , User peripherals are mapped between 0xF000 0000 and 0xFFFF EFFF. SYSIRQ changed to SYSC in "Peripheral Identifiers" Table 10-1 and Table 10-2	specs #2748 #2832 (DBGU IP) rfo review
6175FS	AT91SAM7S161 and AT91SAM7S16 added to product family Features: Timer Counter, on page 2 product specific information rewritten, Table 1-1, "Configuration Summary," on page 3 , footnote explains TC on AT91SAM7S32/16 has only two channels accessible via PIO, and in Section 10.9 "Timer Counter" , precisions added to "compare and capture" output/input. Section 10.6 "Two-wire Interface" , updated reference to I ² C compatibility, internal address registers, slave addressing, Modes for AT91SAM7S161/16 "One Two-wire Interface (TWI)" on page 2 , updated in Features Section 10.12 "Analog-to-digital Converter" , updated Successive Approximation Register ADC and the INL, DNL ± values of LSB. Section 8.8.3 "Lock Regions" , locked-region's erase or program command updated Section 9.5 "Debug Unit" , Chip ID updated. Section 6. "I/O Lines Considerations" , JTAG Port Pin, Test Pin, Erase Pin, updated.	BDs 4208 rfo review 4325 5063

6175GS	<p>“Features” , “Debug Unit (DBGU)” updated with “Mode for General Purpose 2-wire UART Serial Communication”</p> <p>Section 7.4 “Peripheral DMA Controller”, added list of PDC priorities.</p> <p>Section 9. “System Controller”, Figure 9-1 and Figure 9-2 RTT is reset by “power_on_reset”.</p> <p>Section 9.1.1 “Brownout Detector and Power-on Reset”, fourth paragraph reduced.</p> <p>Section 9.5 “Debug Unit”, the list; Section I “Chip ID Registers”, chip IDs updated, added SAM7S32 Rev B and SAM7S64 Rev B to the list.</p> <p>Section 12. “SAM7S Ordering Information”, Updated product ordering information by MRL A and MRL B versions.</p>	<p>5846</p> <p>5913</p> <p>5224</p> <p>5685</p> <p>rfo</p>
6175HS	<p>Section 6.2 “Test Pin”, added to SAM-BA Boot recovery procedure, a power cycle of the board is mandatory.</p> <p>Section 8.10 “SAM-BA Boot Assistant”, added to SAM-BA Boot recovery procedure, a power cycle of the board is mandatory.</p>	6068
6175IS	<p>Section 9.5 “Debug Unit”, Chip ID Registers list updated.</p> <p>MRL C column added to Table 12-1, “SAM7S Series Ordering Information”.</p>	7185
6175JS	<p>Product Series Naming Convention</p> <p>Except for part ordering and library references, AT91 prefix dropped from most nomenclature.</p> <p>AT91SAM7S becomes SAM7S.</p> <p>Debug Unit:</p> <p>“Chip ID Registers” on page 31, Chip ID is 0x270B0A4F for AT91SAM7S512 Rev B</p>	<p>rfo</p> <p>7945</p>
6175KS	<p>Section 9.5 “Debug Unit”, Chip ID Registers list updated. Added Chip ID for SAM7S128 Rev D and SAM7S256 Rev D</p> <p>Table 12-1, “SAM7S Series Ordering Information”. Added SAM7S128 Rev D and SAM7S256 Rev D</p>	8380/8467