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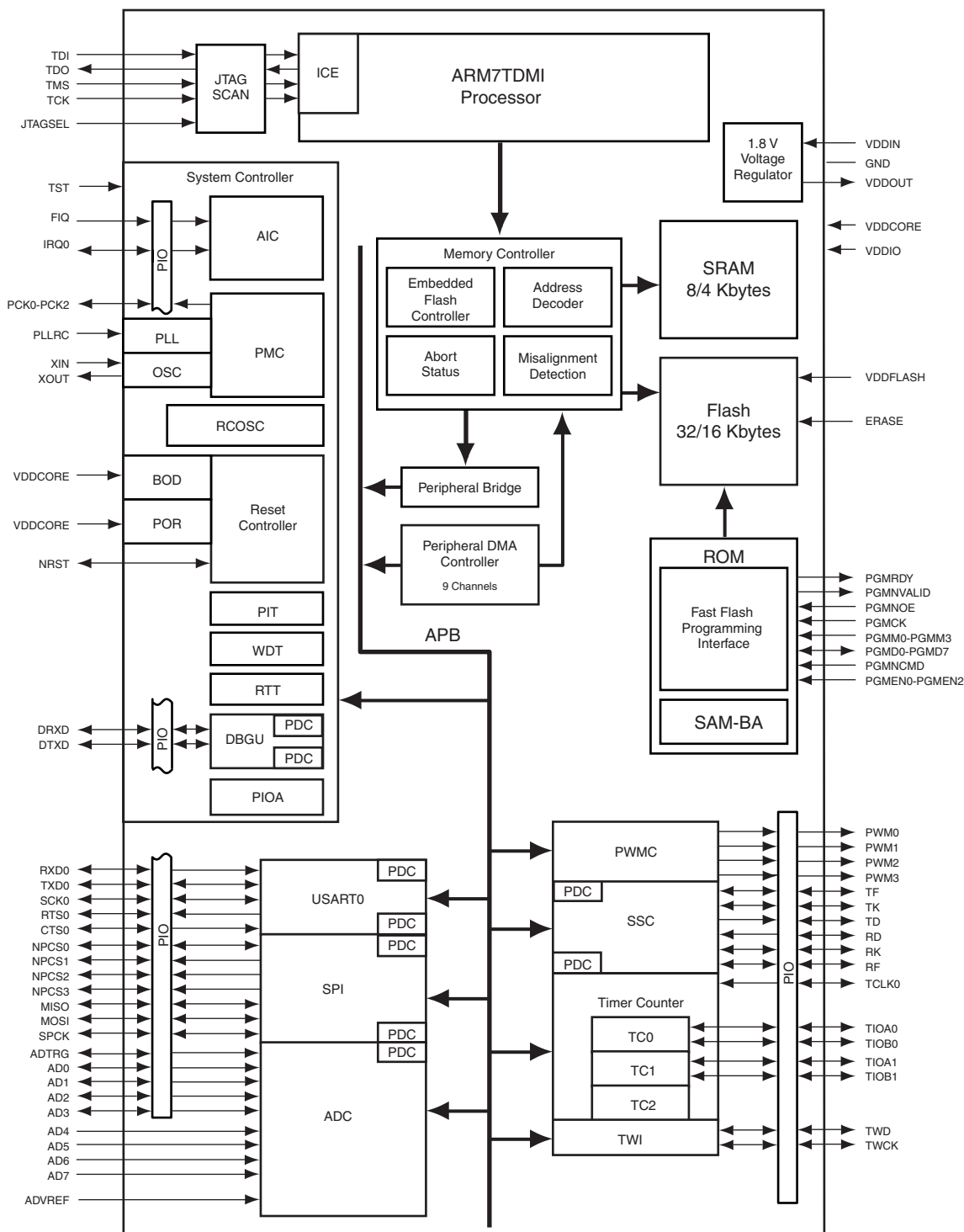
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	I²C, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam7s64-mu-999

Figure 2-2. SAM7S32/16 Block Diagram



3. Signal Description

Table 3-1. Signal Description List

VDDIN	Voltage and ADC Regulator Power Supply Input	Power		3.0 to 3.6V
VDDOUT	Voltage Regulator Output	Power		1.85V nominal
VDDFLASH	Flash Power Supply	Power		3.0V to 3.6V
VDDIO	I/O Lines Power Supply	Power		3.0V to 3.6V or 1.65V to 1.95V
VDDCORE	Core Power Supply	Power		1.65V to 1.95V
VDDPLL	PLL	Power		1.65V to 1.95V
GND	Ground	Ground		
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
PLLRC	PLL Filter	Input		
PCK0 - PCK2	Programmable Clock Output	Output		
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor
JTAGSEL	JTAG Selection	Input		Pull-down resistor ⁽¹⁾
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	Pull-down resistor ⁽¹⁾
NRST	Microcontroller Reset	I/O	Low	Open-drain with pull-Up resistor
TST	Test Mode Select	Input	High	Pull-down resistor ⁽¹⁾
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
IRQ0 - IRQ1	External Interrupt Inputs	Input		IRQ1 not present on SAM7S32/16
FIQ	Fast Interrupt Input	Input		
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset PA0 - PA20 only on SAM7S32/16

4. Package and Pinout

The SAM7S512/256/128/64/321 are available in a 64-lead LQFP or 64-pad QFN package.

The SAM7S161 is available in a 64-Lead LQFP package.

The SAM7S32/16 are available in a 48-lead LQFP or 48-pad QFN package.

4.1 64-lead LQFP and 64-pad QFN Package Outlines

Figure 4-1 and Figure 4-2 show the orientation of the 64-lead LQFP and the 64-pad QFN package. A detailed mechanical description is given in the section Mechanical Characteristics of the full datasheet.

Figure 4-1. 64-lead LQFP Package (Top View)

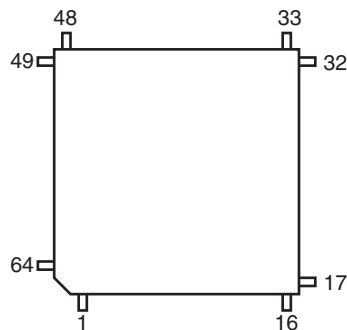
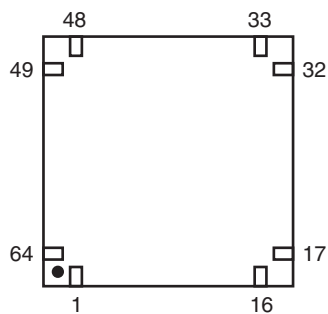


Figure 4-2. 64-pad QFN Package (Top View)



4.3 48-lead LQFP and 48-pad QFN Package Outlines

Figure 4-3 and Figure 4-4 show the orientation of the 48-lead LQFP and the 48-pad QFN package. A detailed mechanical description is given in the section Mechanical Characteristics of the full datasheet.

Figure 4-3. 48-lead LQFP Package (Top View)

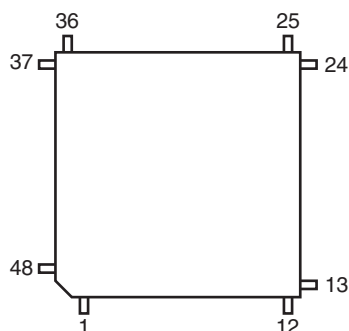
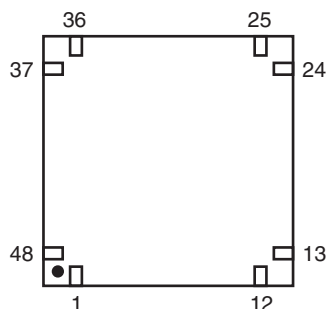


Figure 4-4. 48-pad QFN Package (Top View)



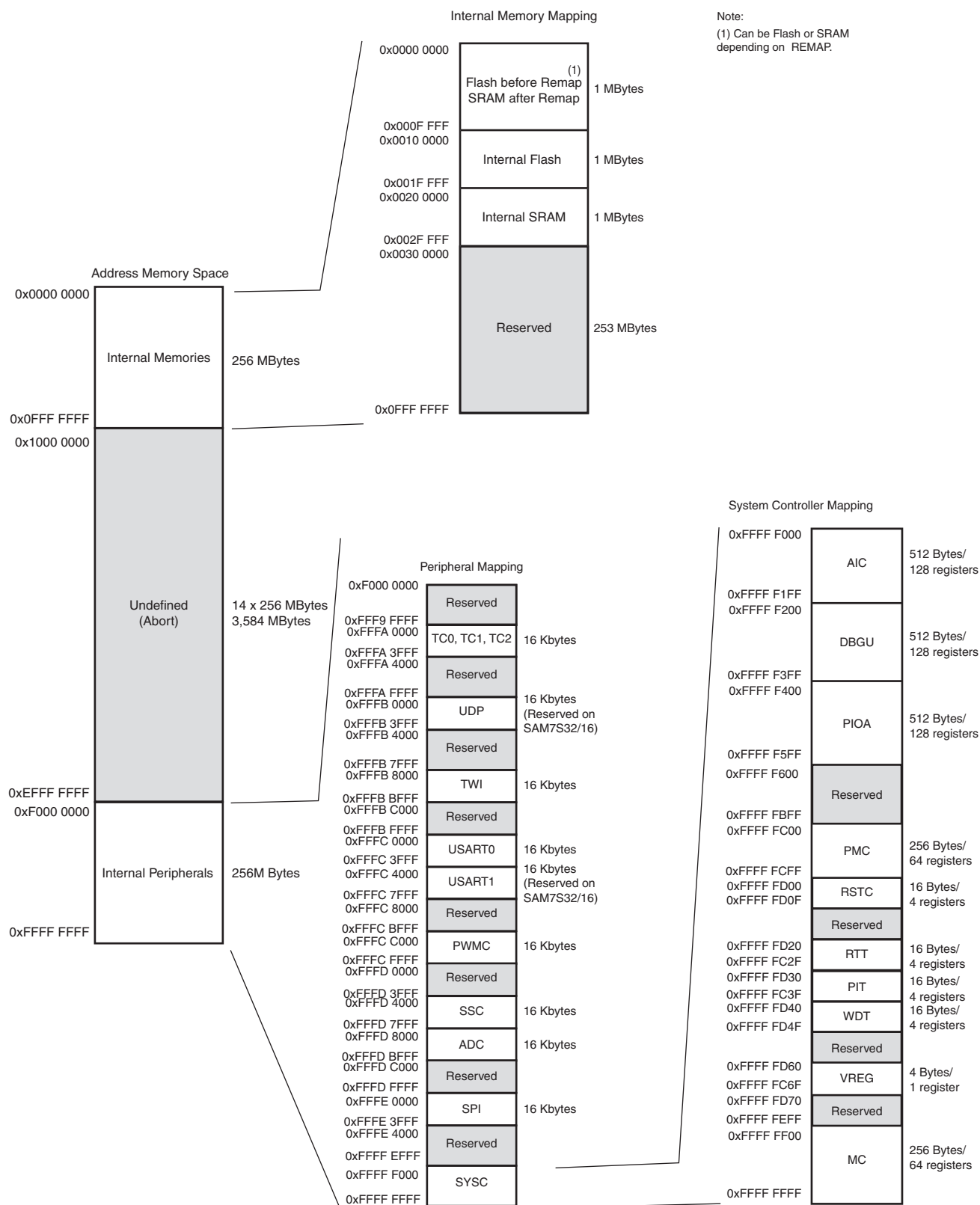
4.4 48-lead LQFP and 48-pad QFN Pinout

Table 4-2. SAM7S32/16 Pinout⁽¹⁾

1	ADVREF	13	VDDIO	25	TDI	37	TDO
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	AD4	15	PA15/PGMD3	27	PA5/PGMRDY	39	TMS
4	AD5	16	PA14/PGMD2	28	PA4/PGMNCMD	40	TCK
5	AD6	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	AD7	18	VDDCORE	30	TST	42	ERASE
7	VDDIN	19	PA12/PGMD0	31	PA3	43	VDDFLASH
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	GND
9	PA17/PGMD5/AD0	21	PA10/PGMM2	33	VDDIO	45	XOUT
10	PA18/PGMD6/AD1	22	PA9/PGMM1	34	GND	46	XIN/PGMCK
11	PA19/PGMD7/AD2	23	PA8/PGMM0	35	PA1/PGMEN1	47	PLLRC
12	PA20/AD3	24	PA7/PGMNVALID	36	PA0/PGMEN0	48	VDDPLL

Note: 1. The bottom pad of the QFN package must be connected to ground.

Figure 8-1. SAM SAM7S512/256/128/64/321/32/161/16 Memory Mapping



8.8.3 Lock Regions

8.8.3.1 SAM7S512

Two Embedded Flash Controllers each manage 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S512 contains 32 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 16 NVM bits (or 32 NVM bits) are software programmable through the corresponding EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.2 SAM7S256

The Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S256 contains 16 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 16 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.3 SAM7S128

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S128 contains 8 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 8 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.4 SAM7S64

The Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S64 contains 16 lock regions and each lock region contains 32 pages of 128 bytes. Each lock region has a size of 4 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 16 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.5 SAM7S321/32

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S321/32 contains 8 lock regions and each lock region contains 32 pages of 128 bytes. Each lock region has a size of 4 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

9.1 Reset Controller

The Reset Controller is based on a power-on reset cell and one brownout detector. It gives the status of the last reset, indicating whether it is a power-up reset, a software reset, a user reset, a watchdog reset or a brownout reset. In addition, it controls the internal resets and the NRST pin open-drain output. It allows to shape a signal on the NRST line, guaranteeing that the length of the pulse meets any requirement.

Note that if NRST is used as a reset output signal for external devices during power-off, the brownout detector must be activated.

9.1.1 Brownout Detector and Power-on Reset

The SAM7S Series embeds a brownout detection circuit and a power-on reset cell. Both are supplied with and monitor VDDCORE. Both signals are provided to the Flash to prevent any code corruption during power-up or power-down sequences or if brownouts occur on the VDDCORE power supply.

The power-on reset cell has a limited-accuracy threshold at around 1.5V. Its output remains low during power-up until VDDCORE goes over this voltage level. This signal goes to the reset controller and allows a full re-initialization of the device.

The brownout detector monitors the VDDCORE level during operation by comparing it to a fixed trigger level. It secures system operations in the most difficult environments and prevents code corruption in case of brownout on the VDDCORE.

Only VDDCORE is monitored.

When the brownout detector is enabled and VDDCORE decreases to a value below the trigger level (V_{bot-} , defined as $V_{bot} - hyst/2$), the brownout output is immediately activated.

When VDDCORE increases above the trigger level (V_{bot+} , defined as $V_{bot} + hyst/2$), the reset is released. The brownout detector only detects a drop if the voltage on VDDCORE stays below the threshold voltage for longer than about 1 μ s.

The threshold voltage has a hysteresis of about 50 mV, to ensure spike free brownout detection. The typical value of the brownout detector threshold is 1.68V with an accuracy of $\pm 2\%$ and is factory calibrated.

The brownout detector is low-power, as it consumes less than 20 μ A static current. However, it can be deactivated to save its static current. In this case, it consumes less than 1 μ A. The deactivation is configured through the GPNVM bit 0 of the Flash.

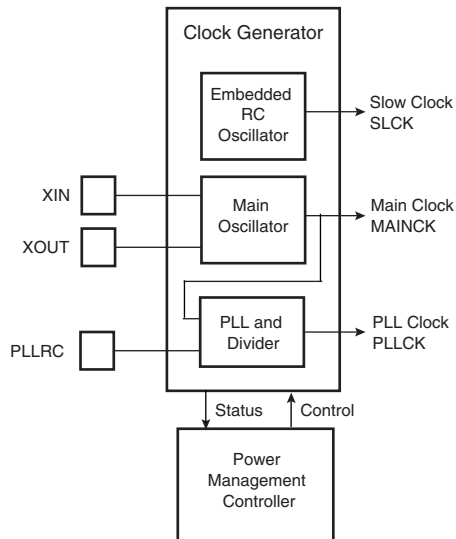
9.2 Clock Generator

The Clock Generator embeds one low-power RC Oscillator, one Main Oscillator and one PLL with the following characteristics:

- RC Oscillator ranges between 22 kHz and 42 kHz
- Main Oscillator frequency ranges between 3 and 20 MHz
- Main Oscillator can be bypassed
- PLL output ranges between 80 and 220 MHz

It provides SLCK, MAINCK and PLLCK.

Figure 9-3. Clock Generator Block Diagram



9.3 Power Management Controller

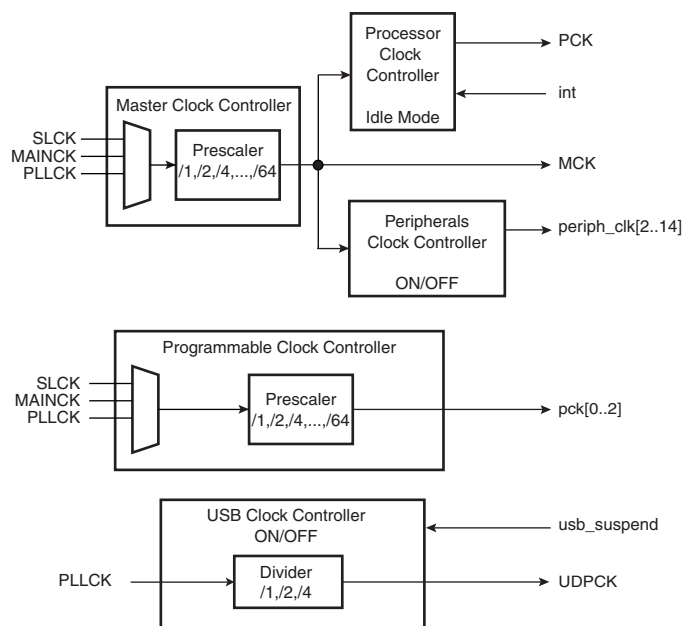
The Power Management Controller uses the Clock Generator outputs to provide:

- the Processor Clock PCK
- the Master Clock MCK
- the USB Clock UDPCK (not present on SAM7S32/16)
- all the peripheral clocks, independently controllable
- three programmable clock outputs

The Master Clock (MCK) is programmable from a few hundred Hz to the maximum operating frequency of the device.

The Processor Clock (PCK) switches off when entering processor idle mode, thus allowing reduced power consumption while waiting for an interrupt.

Figure 9-4. Power Management Controller Block Diagram



9.4 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of an ARM Processor
- Individually maskable and vectored interrupt sources
 - Source 0 is reserved for the Fast Interrupt Input (FIQ)
 - Source 1 is reserved for system peripherals RTT, PIT, EFC, PMC, DBGU, etc.)
 - Other sources control the peripheral interrupts or external interrupts
 - Programmable edge-triggered or level-sensitive internal sources
 - Programmable positive/negative edge-triggered or high/low level-sensitive external sources
- 8-level Priority Controller
 - Drives the normal interrupt of the processor
 - Handles priority of the interrupt sources
 - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
 - Optimizes interrupt service routine branch and execution
 - One 32-bit vector register per interrupt source
 - Interrupt vector register reads the corresponding current interrupt vector
- Protect Mode
 - Easy debugging by preventing automatic operations
- Fast Forcing
 - Permits redirecting any interrupt source on the fast interrupt
- General Interrupt Mask
 - Provides processor synchronization on events without triggering an interrupt

9.5 Debug Unit

- Comprises:
 - One two-pin UART
 - One Interface for the Debug Communication Channel (DCC) support

- One set of Chip ID Registers
- One Interface providing ICE Access Prevention
- Two-pin UART
 - Implemented features are compatible with the USART
 - Programmable Baud Rate Generator
 - Parity, Framing and Overrun Error
 - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
- Debug Communication Channel Support
 - Offers visibility of COMMRX and COMMTX signals from the ARM Processor
- Chip ID Registers
 - Identification of the device revision, sizes of the embedded memories, set of peripherals
 - Chip ID is 0x270B0A40 for AT91SAM7S512 Rev A
 - Chip ID is 0x270B0A4F for AT91SAM7S512 Rev B
 - Chip ID is 0x270D0940 for AT91SAM7S256 Rev A
 - Chip ID is 0x270B0941 for AT91SAM7S256 Rev B
 - Chip ID is 0x270B0942 for AT91SAM7S256 Rev C
 - Chip ID is TBD for AT91SAM7S256 Rev D
 - Chip ID is 0x270C0740 for AT91SAM7S128 Rev A
 - Chip ID is 0x270A0741 for AT91SAM7S128 Rev B
 - Chip ID is 0x270A0742 for AT91SAM7S128 Rev C
 - Chip ID is TBD for AT91SAM7S128 Rev D
 - Chip ID is 0x27090540 for AT91SAM7S64 Rev A
 - Chip ID is 0x27090543 for AT91SAM7S64 Rev B
 - Chip ID is 0x27090544 for AT91SAM7S64 Rev C
 - Chip ID is 0x27080342 for AT91SAM7S321 Rev A
 - Chip ID is 0x27080340 for AT91SAM7S32 Rev A
 - Chip ID is 0x27080341 for AT91SAM7S32 Rev B
 - Chip ID is 0x27050241 for AT91SAM7S161 Rev A
 - Chip ID is 0x27050240 for AT91SAM7S16 Rev A

Note: Refer to the errata section of the datasheet for updates on chip ID.

9.6 Periodic Interval Timer

- 20-bit programmable counter plus 12-bit interval counter

9.7 Watchdog Timer

- 12-bit key-protected Programmable Counter running on prescaled SCLK
- Provides reset or interrupt signals to the system
- Counter may be stopped while the processor is in debug state or in idle mode

9.8 Real-time Timer

- 32-bit free-running counter with alarm running on prescaled SCLK
- Programmable 16-bit prescaler for SCLK accuracy compensation

9.9 PIO Controller

- One PIO Controller, controlling 32 I/O lines (21 for SAM7S32/16)
- Fully programmable through set/clear registers
- Multiplexing of two peripheral functions per I/O line
- For each I/O line (whether assigned to a peripheral or used as general-purpose I/O)
 - Input change interrupt
 - Half a clock period glitch filter
 - Multi-drive option enables driving in open drain
 - Programmable pull-up on each I/O line
 - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

9.10 Voltage Regulator Controller

The aim of this controller is to select the Power Mode of the Voltage Regulator between Normal Mode (bit 0 is cleared) or Standby Mode (bit 0 is set).

Table 10-2. Peripheral Identifiers (SAM7S32/16)

0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC ⁽¹⁾	System	
2	PIOA	Parallel I/O Controller A	
3	Reserved		
4	ADC ⁽¹⁾	Analog-to Digital Converter	
5	SPI	Serial Peripheral Interface	
6	US	USART	
7	Reserved		
8	SSC	Synchronous Serial Controller	
9	TWI	Two-wire Interface	
10	PWMC	PWM Controller	
11	Reserved		
12	TC0	Timer/Counter 0	
13	TC1	Timer/Counter 1	
14	TC2	Timer/Counter 2	
15 - 29	Reserved		
30	AIC	Advanced Interrupt Controller	IRQ0
31	Reserved		

10.3 Peripheral Multiplexing on PIO Lines

The SAM7S Series features one PIO controller, PIOA, that multiplexes the I/O lines of the peripheral set.

PIO Controller A controls 32 lines (21 lines for SAM7S32/16). Each line can be assigned to one of two peripheral functions, A or B. Some of them can also be multiplexed with the analog inputs of the ADC Controller.

Table 10-3, “Multiplexing on PIO Controller A (SAM7S512/256/128/64/321/161),” on page 35 and Table 10-4, “Multiplexing on PIO Controller A (SAM7S32/16),” on page 36 define how the I/O lines of the peripherals A, B or the analog inputs are multiplexed on the PIO Controller A. The two columns “Function” and “Comments” have been inserted for the user’s own comments; they may be used to track how pins are defined in an application.

Note that some peripheral functions that are output only may be duplicated in the table.

All pins reset in their Parallel I/O lines function are configured as input with the programmable pull-up enabled, so that the device is maintained in a static state as soon as a reset is detected.

10.4 PIO Controller A Multiplexing

Table 10-3. Multiplexing on PIO Controller A (SAM7S512/256/128/64/321/161)

PA0	PWM0	TIOA0	High-Drive		
PA1	PWM1	TIOB0	High-Drive		
PA2	PWM2	SCK0	High-Drive		
PA3	TWD	NPCS3	High-Drive		
PA4	TWCK	TCLK0			
PA5	RXD0	NPCS3			
PA6	TXD0	PCK0			
PA7	RTS0	PWM3			
PA8	CTS0	ADTRG			
PA9	DRXD	NPCS1			
PA10	DTXD	NPCS2			
PA11	NPCS0	PWM0			
PA12	MISO	PWM1			
PA13	MOSI	PWM2			
PA14	SPCK	PWM3			
PA15	TF	TIOA1			
PA16	TK	TIOB1			
PA17	TD	PCK1	AD0		
PA18	RD	PCK2	AD1		
PA19	RK	FIQ	AD2		
PA20	RF	IRQ0	AD3		
PA21	RXD1	PCK1			
PA22	TXD1	NPCS3			
PA23	SCK1	PWM0			
PA24	RTS1	PWM1			
PA25	CTS1	PWM2			
PA26	DCD1	TIOA2			
PA27	DTR1	TIOB2			
PA28	DSR1	TCLK1			
PA29	RI1	TCLK2			
PA30	IRQ1	NPCS2			
PA31	NPCS1	PCK2			

10.8 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.9 Timer Counter

- Three 16-bit Timer Counter Channels
 - Two output compare or one input capture per channel (except for SAM7S32/16 which have only two channels connected to the PIO)
- Wide range of functions including:
 - Frequency measurement
 - Event counting
 - Interval measurement
 - Pulse generation
 - Delay timing
 - Pulse Width Modulation
 - Up/down capabilities
- Each channel is user-configurable and contains:
 - Three external clock inputs (The SAM7S32/16 have one)
 - Five internal clock inputs, as defined in [Table 10-5](#)

Table 10-5. Timer Counter Clocks Assignment

TIMER_CLOCK1	MCK/2
TIMER_CLOCK2	MCK/8
TIMER_CLOCK3	MCK/32
TIMER_CLOCK4	MCK/128
TIMER_CLOCK5	MCK/1024

- Two multi-purpose input/output signals
- Two global registers that act on all three TC channels

10.10 PWM Controller

- Four channels, one 16-bit counter per channel
- Common clock generator, providing thirteen different clocks
 - One Modulo n counter providing eleven clocks
 - Two independent linear dividers working on modulo n counter outputs
- Independent channel programming
 - Independent enable/disable commands
 - Independent clock selection
 - Independent period and duty cycle, with double buffering
 - Programmable selection of the output waveform polarity

Table 11-1. 48-lead LQFP Package Dimensions (in mm)

Symbol						
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
R2	0.08	–	0.20	0.003	–	0.008
R1	0.08	–	–	0.003	–	–
q	0°	3.5°	7°	0°	3.5°	7°
θ ₁	0°	–	–	0°	–	–
θ ₂	11°	12°	13°	11°	12°	13°
θ ₃	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	5.50			0.217		
E2	5.50			0.217		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

11.2 QFN Packages

Figure 11-2. 48-pad QFN Package

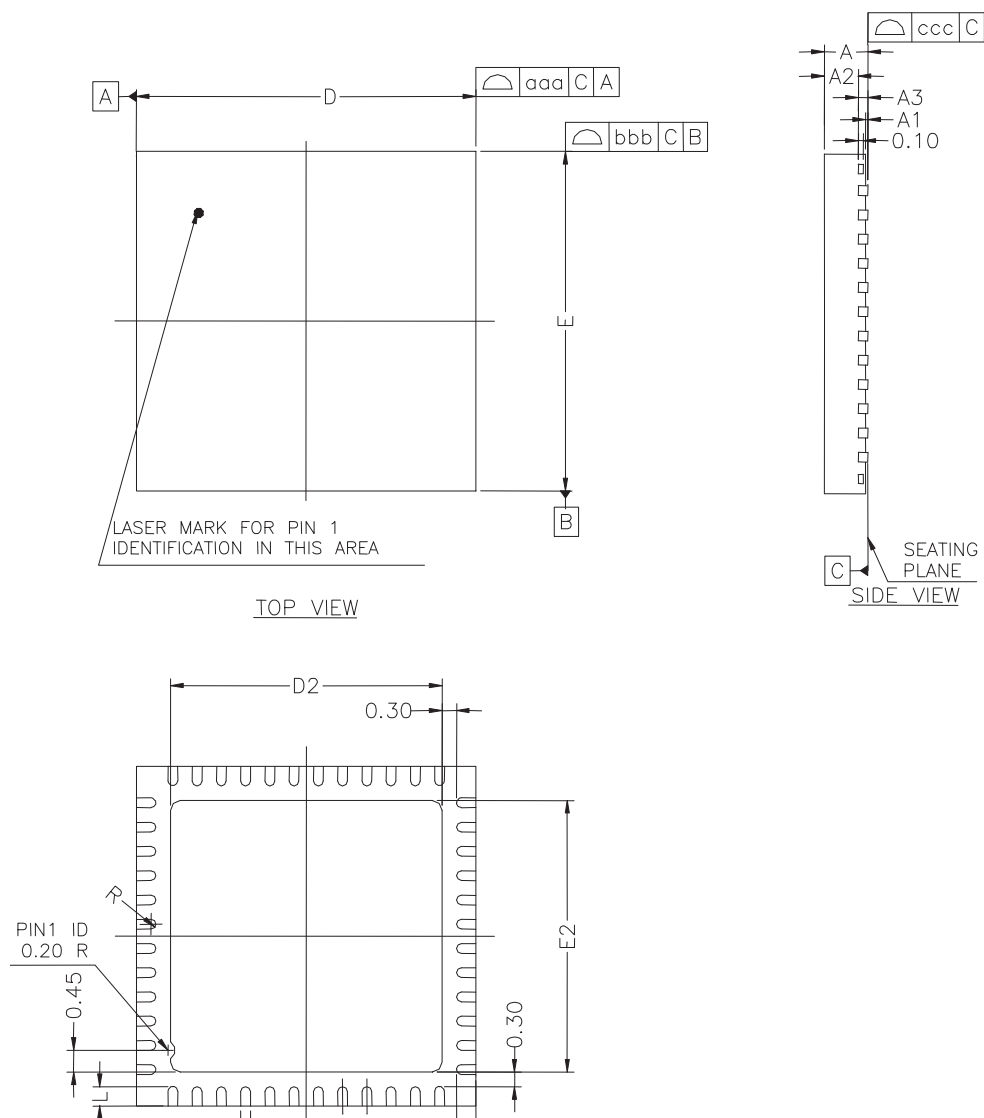


Figure 11-3. 64-pad QFN Package Drawing

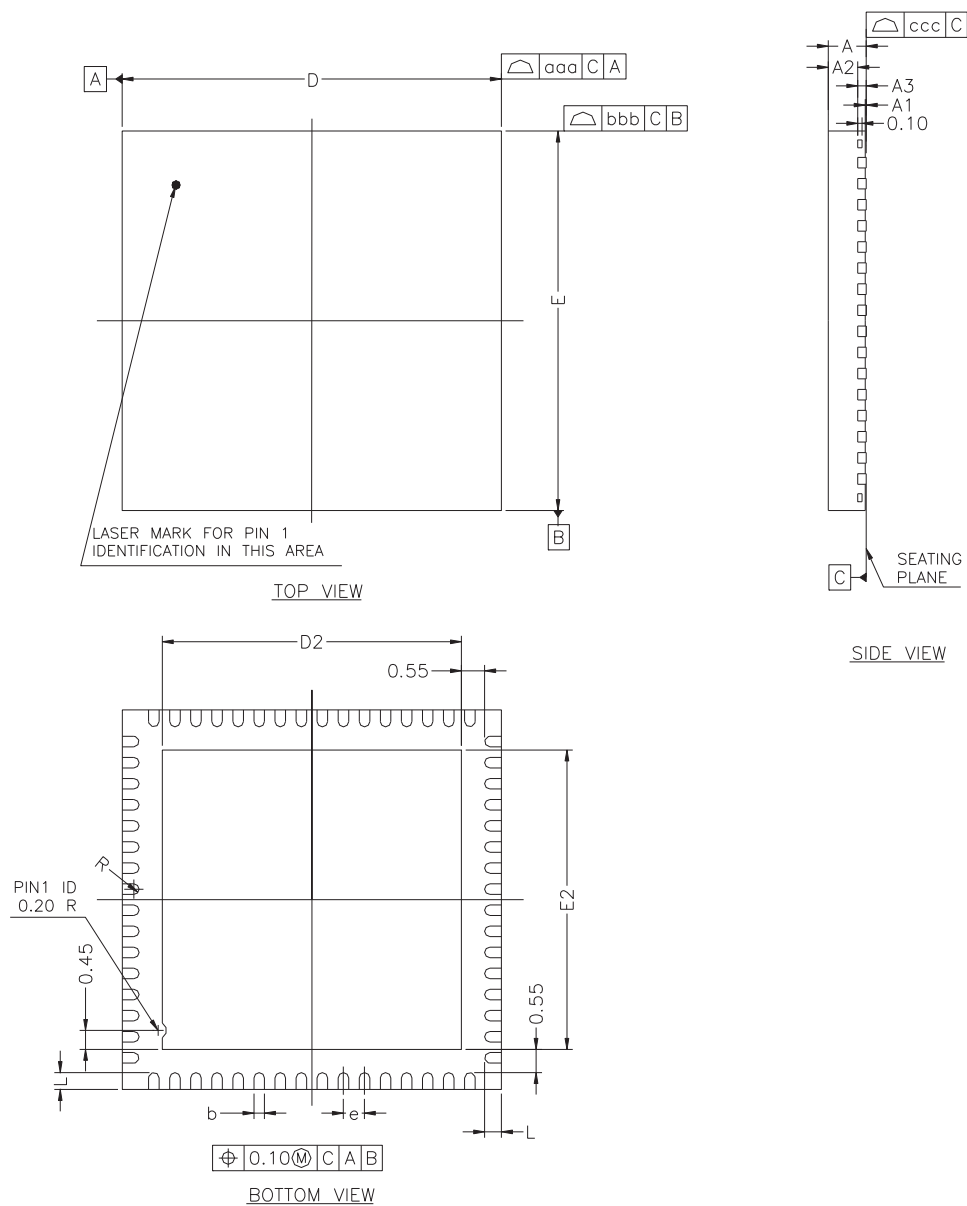


Table 11-4. 64-pad QFN Package Dimensions (in mm)

Symbol						
A	–	–	090	–	–	0.035
A1	–	–	0.05	–	–	0.001
A2	–	0.65	0.70	–	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.23	0.25	0.28	0.009	0.010	0.011
D	9.00 bsc			0.354 bsc		
D2	6.95	7.10	7.25	0.274	0.280	0.285
E	9.00 bsc			0.354 bsc		
E2	6.95	7.10	7.25	0.274	0.280	0.285
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 bsc			0.020 bsc		
R	0.125	–	–	0.0005	–	–
Tolerances of Form and Position						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		



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