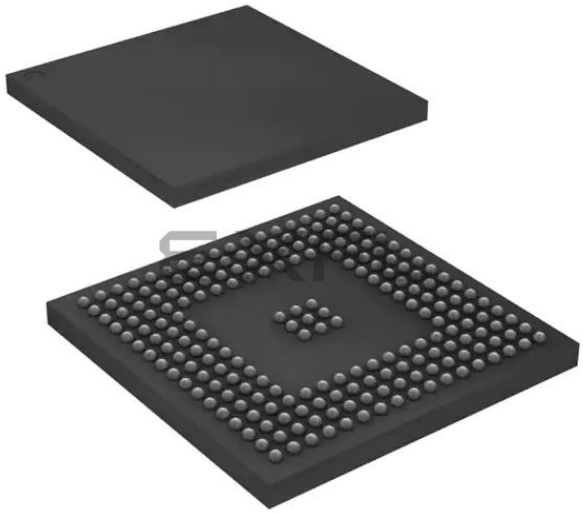


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM, SRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD
Ethernet	-
SATA	-
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	217-LFBGA
Supplier Device Package	217-LFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam9g10-cu

- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Three External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire USART and support for Debug Communication Channel, Programmable ICE Access Prevention
  - Mode for General Purpose Two-wire UART Serial Communication
- Periodic Interval Timer (PIT)
  - 20-bit Interval Timer plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - Key Protected, Programmable Only Once, Windowed 12-bit Counter, Running at Slow Clock
- Real-Time Timer (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock
- Three 32-bit Parallel Input/Output Controllers (PIO) PIOA, PIOB and PIOC
  - 96 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
  - Schmitt Trigger on All Inputs
- Nineteen Peripheral DMA (PDC) Channels
- Multimedia Card Interface (MCI)
  - SDCard/SDIO and MultiMediaCard™ Compliant
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC, MMC and SDCard Compliant
- Three Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Three Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation
  - Support for ISO7816 T0/T1 Smart Card, Hardware and Software Handshaking, RS485 Support
- Two Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- Two-wire Interface (TWI)
  - Master Mode Support, All Two-wire Atmel EEPROMs Supported
  - Compatibility with Standard Two-wire Serial Memories
  - One, Two or Three Bytes for Slave Address
  - Sequential Read/Write Operations
  - Master, Multi-master and Slave Mode Operation
  - Bit rate: up to 400 Kbits
  - GEneral Call Supported in Slave Mode
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies:
  - 1.08V to 1.32V for VDDCORE and VDDBU
  - 3.0V to 3.6V for VDDOSC and for VDDPLL
  - 2.7V to 3.6V for VDDIOP (Peripheral I/Os)
  - 1.65V to 3.6V for VDDIOM (Memory I/Os)
- Available in a 217-ball LFBGA RoHS-compliant Package

1. Description

The AT91SAM9G10 is a complete system-on-chip built around the ARM926EJ-S ARM Thumb processor with an extended DSP instruction set and Jazelle Java accelerator. It achieves 293 MIPS at 266 MHz.

The AT91SAM9G10 is an optimized host processor for applications with an LCD display. Its integrated LCD controller supports BW and up to 16M color, active and passive LCD displays. The External Bus Interface incorporates controllers for synchronous DRAM (SDRAM) and Static memories and features specific interface circuitry for CompactFlash and NAND Flash.

The AT91SAM9G10 integrates a ROM-based Boot Loader supporting code shadowing from, for example, external DataFlash® into external SDRAM. The software controlled Power Management Controller (PMC) keeps system power consumption to a minimum by selectively enabling/disabling the processor and various peripherals and adjustment of the operating frequency.

The AT91SAM9G10 also benefits from the integration of a wide range of debug features including JTAG-ICE, a dedicated UART debug channel (DBGU). This enables the development and debug of all applications, especially those with real-time constraints.

3. Signal Description

Table 3-1. Signal Description by Peripheral

Signal Name	Function	Type	Active Level	Comments
Power				
VDDIOM	EBI I/O Lines Power Supply	Power		1.65 V to 1.95V and 3.0V to 3.6V
VDDIOP	Peripherals I/O Lines Power Supply	Power		3.0V to 3.6V
VDDBU	Backup I/O Lines Power Supply	Power		1.08V to 1.32V
VDDPLL	PLL Power Supply	Power		3.0V to 3.6V
VDDOSC	Oscillator Power Supply	Power		3.0V to 3.6V
VDDCORE	Core Chip Power Supply	Power		1.08V to 1.32V
GND	Ground	Ground		
GNDPLL	PLL Ground	Ground		
GNDOSC	Oscillator Ground	Ground		
GNDBU	Backup Ground	Ground		
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
XIN32	Slow Clock Oscillator Input	Input		
XOUT32	Slow Clock Oscillator Output	Output		
PLLRCA	PLL Filter	Input		
PLLRCB	PLL Filter	Input		
PCK0 - PCK3	Programmable Clock Output	Output		
Shutdown, Wakeup Logic				
SHDN	Shutdown Control	Output		Do not tie over VDDBU.
WKUP	Wake-Up Input	Input		Accepts between 0V and VDDBU.
ICE and JTAG				
TCK	Test Clock	Input		No pull-up resistor.
RTCK	Returned Test Clock	Output		No pull-up resistor.
TDI	Test Data In	Input		No pull-up resistor.
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor.
NTRST	Test Reset Signal	Input	Low	Pull-up resistor.
JTAGSEL	JTAG Selection	Input		Pull-down resistor. Accepts between 0V and VDDBU.
Reset/Test				
NRST	Microcontroller Reset	I/O	Low	Pull-up resistor
TST	Test Mode Select	Input		Pull-down resistor.
BMS	Boot Mode Select	Input		
Debug Unit				
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		

4. Package and Pinout

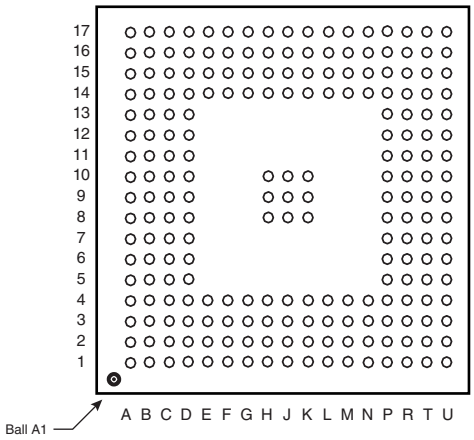
The AT91SAM9G10 is available in a 217-ball LFBGA RoHS-compliant package, 15 x 15 mm, 0.8 mm ball pitch

4.1 217-ball LFBGA Package Outline

Figure 4-1 shows the orientation of the 217-ball LFBGA Package.

A detailed mechanical description is given in the section “AT91SAM9G10 Mechanical Characteristics” of the product datasheet.

Figure 4-1. 217-ball LFBGA Package Outline (Top View)



The NRST pin integrates a permanent pull-up resistor of 100 kΩ minimum to VDDIOP.

The NRST signal is inserted in the Boundary Scan.

6.4 PIO Controller A, B and C Lines

All the I/O lines PA0 to PA31, PB0 to PB31, and PC0 to PC31 integrate a programmable pull-up resistor of 100 kΩ. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers.

After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that require to be enabled as Peripherals at reset. This is explicitly indicated in the column “Reset State” of the PIO Controller multiplexing tables.

6.5 Shutdown Logic Pins

The SHDN pin is an output only, driven by Shutdown Controller.

The pin WKUP is an input only. It can accept voltages only between 0V and VDDBU.

7. Processor and Architecture

7.1 ARM926EJ-S Processor

- RISC Processor Based on ARM v5TEJ Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets
  - ARM High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-Stage Pipeline Architecture:
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 16 Kbyte Data Cache, 16 Kbyte Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete AHB system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)

7.2 Debug and Test Features

- Integrated Embedded In-circuit Emulator Real-Time
  - Two real-time Watchpoint Units
  - Two Independent Registers: Debug Control Register and Debug Status Register
  - Test Access Port Accessible through JTAG Protocol
  - Debug Communications Channel
- Debug Unit
  - Two-pin UART
  - Debug Communication Channel Interrupt Handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins

7.3 Bus Matrix

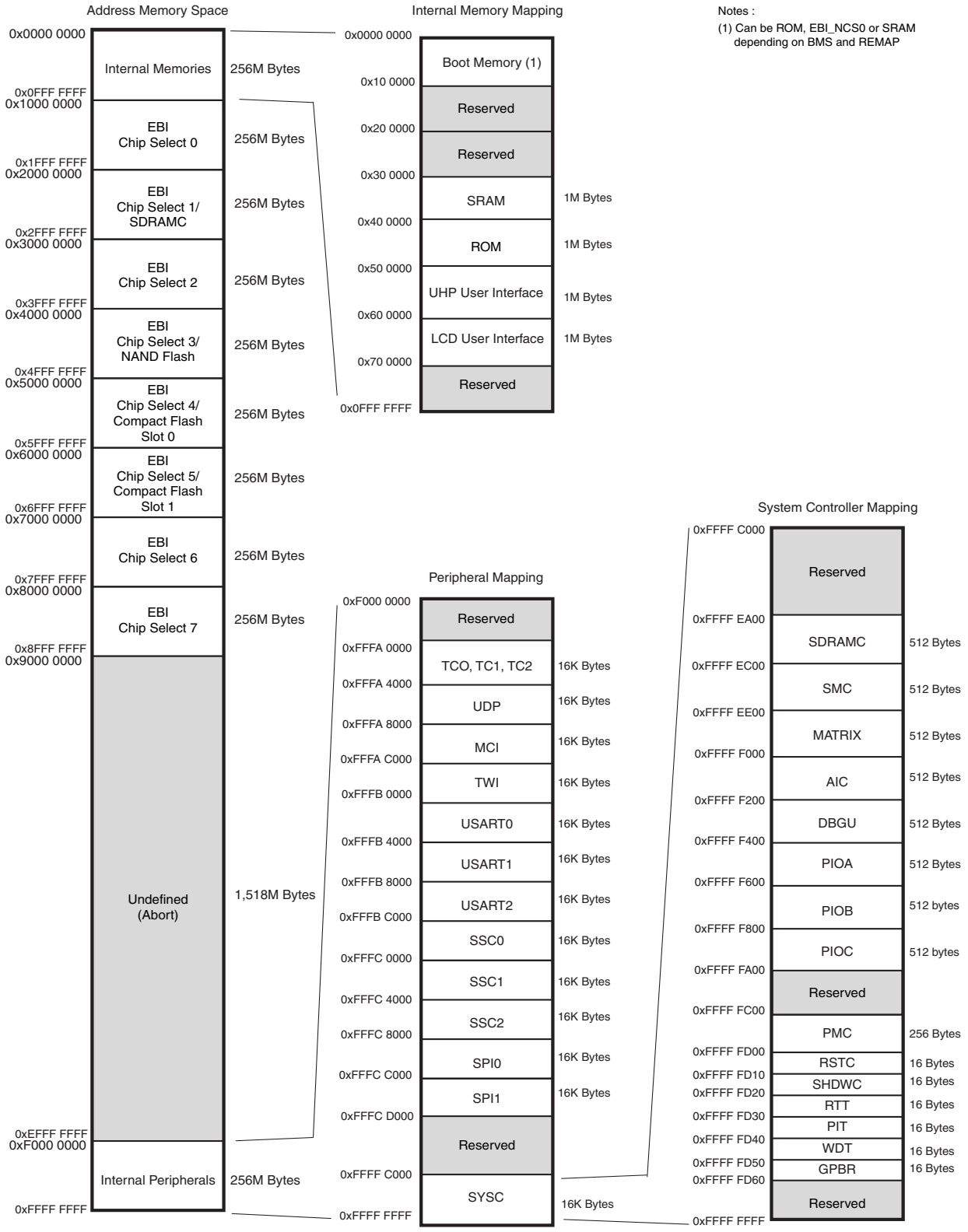
- Five Masters and Five Slaves handled
  - Handles Requests from the ARM926EJ-S, USB Host Port, LCD Controller and the Peripheral DMA Controller to internal ROM, internal SRAM, EBI, APB, LCD Controller and USB Host Port.
  - Round-Robin Arbitration (three modes supported: no default master, last accessed default master, fixed default master)
  - Burst Breaking with Slot Cycle Limit
- One Address Decoder Provided per Master
  - Three different slaves may be assigned to each decoded memory area: one for internal boot, one for external boot, one after remap.
- Boot Mode Select Option
  - Non-volatile Boot Memory can be Internal or External.
  - Selection is made by BMS pin sampled at reset.
- Remap Command
  - Allows Remapping of an Internal SRAM in Place of the Boot Non-Volatile Memory
  - Allows Handling of Dynamic Exception Vectors

7.4 Peripheral DMA Controller

- Transfers from/to peripheral to/from any memory space without intervention of the processor.
- Next Pointer Support, forbids strong real-time constraints on buffer management.
- Nineteen channels
  - Two for each USART
  - Two for the Debug Unit
  - Two for each Serial Synchronous Controller
  - Two for each Serial Peripheral Interface
  - One for the Multimedia Card Interface

8. Memories

Figure 8-1. AT91SAM9G10 Memory Mapping



A first level of address decoding is performed by the Bus Matrix, i.e., the implementation of the Advanced High performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4 Gbytes of address space into 16 areas of 256 Mbytes. The areas 1 to 8 are directed to the EBI that associates these areas to the external chip selects NCS0 to NCS7. The area 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1 Mbyte of internal memory area. The area 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

The Bus Matrix manages five Masters and five Slaves.

Each Master has its own bus and its own decoder, thus allowing a different memory mapping per Master.

Regarding Master 0 and Master 1 (ARM926™ Instruction and Data), three different Slaves are assigned to the memory space decoded at address 0x0: one for internal boot, one for external boot, one after remap. Refer to Table 8-3 for details.

Table 8-1. List of Bus Matrix Masters

Master 0	ARM926 Instruction
Master 1	ARM926 Data
Master 2	PDC
Master 3	LCD Controller
Master 4	USB Host

Each Slave has its own arbiter, thus allowing a different arbitration per Slave.

Table 8-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM
Slave 1	Internal ROM
Slave 2	LCD Controller and USB Host Port Interfaces
Slave 3	External Bus Interface
Slave 4	Internal Peripherals

8.1 Embedded Memories

- 32 KB ROM
  - Single Cycle Access at full bus speed
- 16 KB Fast SRAM
  - Single Cycle Access at full bus speed

8.1.2.1 *BMS = 1, Boot on Embedded ROM*

The system boots using the Boot Program.

- Enable the 32,768 Hz oscillator
- Auto baudrate detection
- Downloads and runs an application from external storage media into internal SRAM
- Automatic detection of valid application
- Bootloader on a non-volatile memory
  - SPI Serial Flash or DataFlash® connected on NPCS0 of the SPI0
  - NAND Flash
  - SDCard (boot ROM does not support high-capacity SDCards)
- SAM-BA Boot in case no valid program is detected in external NVM, supporting
  - Serial communication on a DBGU
  - USB Device HS Port

8.1.2.2 *BMS = 0, Boot on External Memory*

- Boot on slow clock (32,768 Hz)
- Boot with the default configuration for the Static Memory Controller, byte select mode, 16-bit data bus, Read/Write controlled by Chip Select, allows boot on 16-bit non-volatile memory.

The customer-programmed software must perform a complete configuration.

To speed up the boot sequence when booting at 32 kHz EBI CS0 (BMS=0), the user must take the following steps:

1. Program the PMC (main oscillator enable or bypass mode).
2. Program and start the PLL.
3. Reprogram the SMC setup, cycle, hold, mode timings registers for CS0 to adapt them to the new clock
4. Switch the main clock to the new value.

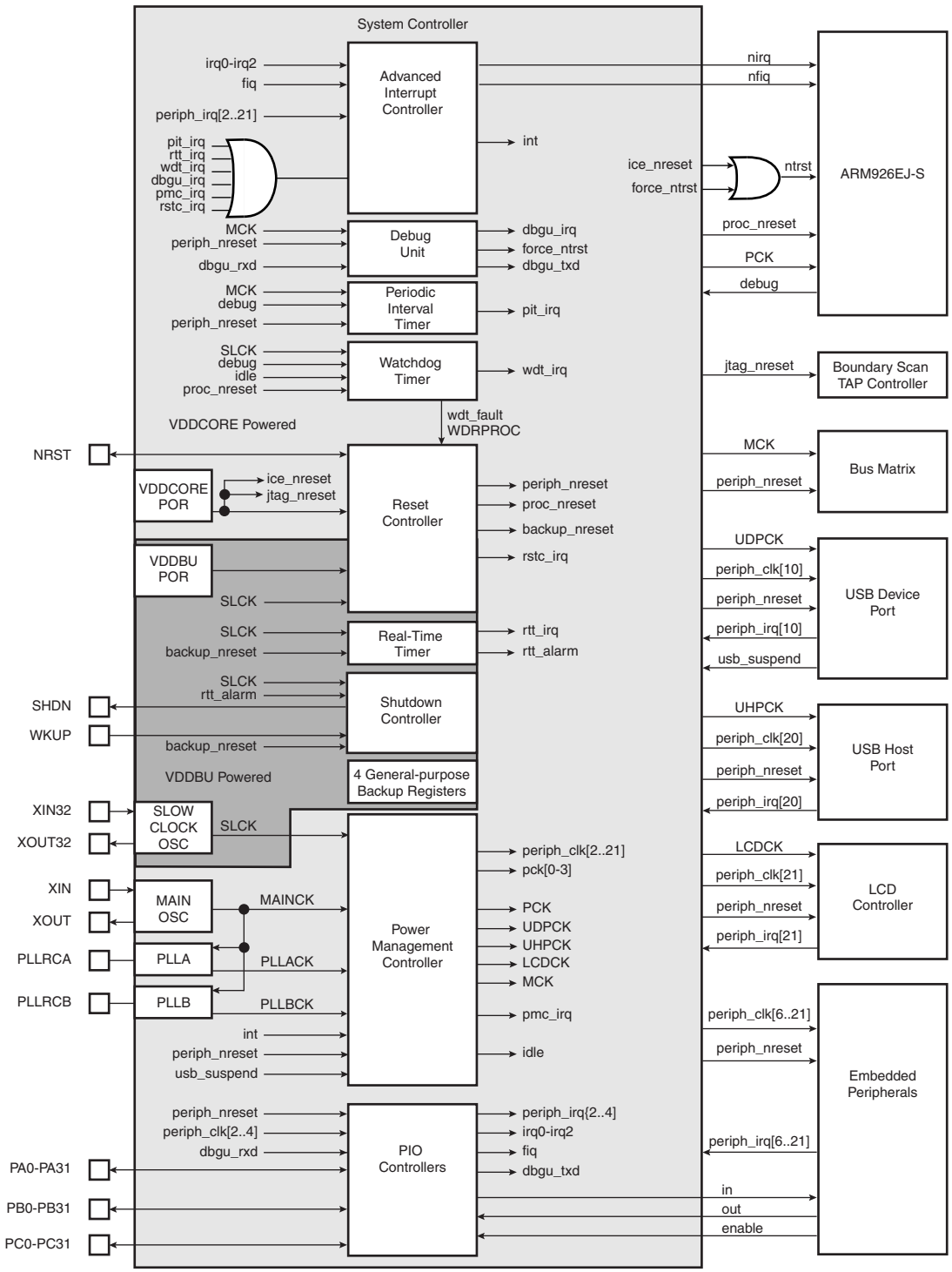
8.2 External Memories

The external memories are accessed through the External Bus Interface (Bus Matrix Slave 3).

Refer to the memory map in Figure 8-1 on page 15.

9.1 Block Diagram

Figure 9-1. System Controller Block Diagram



9.2 Reset Controller

- Based on two Power-on-Reset cells
- Status of the last reset
  - Either cold reset, first reset, soft reset, user reset, watchdog reset, wake-up reset
- Controls the internal resets and the NRST pin output

9.3 Shutdown Controller

- Shutdown and Wake-up logic:
  - Software programmable assertion of the SHDN pin
  - Deassertion Programmable on a WKUP pin level change or on alarm

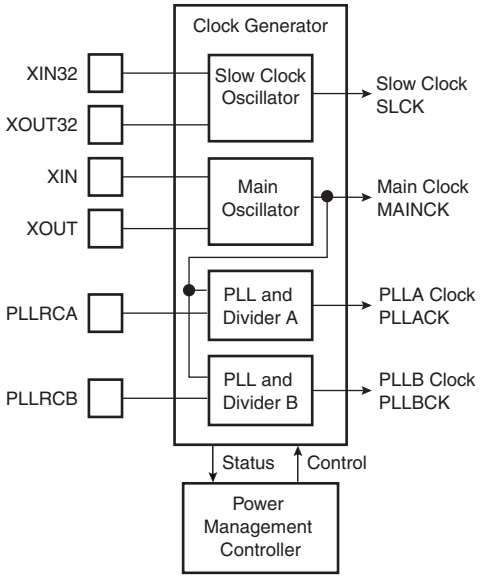
9.4 General-purpose Backup Registers

- Four 32-bit general-purpose backup registers

9.5 Clock Generator

- Embeds the Low-power 32,768 Hz Slow Clock Oscillator
  - Provides the permanent Slow Clock to the system
- Embeds the Main Oscillator
  - Oscillator bypass feature
  - Supports 3 to 20 MHz crystals
- Embeds Two PLLs
  - Outputs 80 to 300 MHz clocks
  - Integrates an input divider to increase output accuracy
  - 1 MHz minimum input frequency
- Provides SLCK, MAINCK, PLLACK and PLLBCK.

Figure 9-2. Clock Generator Block Diagram



9.10 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of an ARM Processor
- Thirty-two individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals (PIT, RTT, PMC, DBGU, etc.)
  - Source 2 to Source 31 control up to thirty embedded peripheral interrupts or external interrupts
  - Programmable edge-triggered or level-sensitive internal sources
  - Programmable positive/negative edge-triggered or high/low level-sensitive
- Four External Sources
- 8-level Priority Controller
  - Drives the normal interrupt of the processor
  - Handles priority of the interrupt sources 1 to 31
  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes Interrupt Service Routine Branch and Execution
  - One 32-bit Vector Register per interrupt source
  - Interrupt Vector Register reads the corresponding current Interrupt Vector
- Protect Mode
  - Easy debugging by preventing automatic operations when protect mode is enabled
- Fast Forcing
  - Permits redirecting any normal interrupt source on the Fast Interrupt of the processor
- General Interrupt Mask
  - Provides processor synchronization on events without triggering an interrupt

9.11 Debug Unit

- Composed of four functions
  - Two-pin UART
  - Debug Communication Channel (DCC) support
  - Chip ID Registers
  - ICE Access Prevention
- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter
- Debug Communication Channel Support

10.3 Peripheral Multiplexing on PIO Lines

The AT91SAM9G10 features three PIO controllers, PIOA, PIOB and PIOC, that multiplex the I/O lines of the peripheral set.

Each PIO Controller controls up to thirty-two lines. Each line can be assigned to one of two peripheral functions, A or B. Table 10-2 on page 28, Table 10-3 on page 29 and Table 10-4 on page 30 define how the I/O lines of the peripherals A and B are multiplexed on the PIO Controllers. The two columns “Function” and “Comments” have been inserted for the user’s own comments; they may be used to track how pins are defined in an application.

Note that some output only peripheral functions might be duplicated within the tables.

The column “Reset State” indicates whether the PIO line resets in I/O mode or in peripheral mode. If I/O is mentioned, the PIO line resets in input with the pull-up enabled, so that the device is maintained in a static state as soon as the reset is released. As a result, the bit corresponding to the PIO line in the register PIO_PSR (Peripheral Status Register) resets low.

If a signal name is mentioned in the “Reset State” column, the PIO line is assigned to this function and the corresponding bit in PIO_PSR resets high. This is the case of pins controlling memories, in particular the address lines, which require the pin to be driven as soon as the reset is released. Note that the pull-up resistor is also enabled in this case.

10.3.1 Resource Multiplexing

10.3.1.1 LCD Controller

The LCD Controller can interface with several LCD panels. It supports 4, 8 or 16 bit-per-pixel without any limitation. Interfacing 24 bit-per-pixel TFTs panel prevents using the SSC0 and the chip select line 0 of the SPI1.

16 bit-per-pixel TFT panels are interfaced through peripheral B functions, as color data is output on LCDD3 to LCDD7, LCDD11 to LCDD15 and LCDD19 to LCDD23. Intensity bit is output on LCDD2, LCDD10 and LCDD18. Using the peripheral B does not prevent using the SSC0 and the SPI1 lines.

10.3.1.2 EBI

If not required, the NWAIT function (external wait request) can be deactivated by software, allowing this pin to be used as a PIO.

10.3.1.3 32-bit Data Bus

Using a 32-bit Data Bus prevents:

- using the three Timer Counter channels’ outputs and trigger inputs
- using the SSC2

10.3.1.4 NAND Flash Interface

Using the NAND Flash interface prevents:

- using NCS3, NCS6 and NCS7 to access other parallel devices

10.3.1.5 Compact Flash Interface

Using the CompactFlash interface prevents:

- using NCS4 and/or NCS5 to access other parallel devices

10.3.2 PIO Controller A Multiplexing

Table 10-2. Multiplexing on PIO Controller A

PIO Controller A					Application Usage		
I/O Line	Peripheral A	Peripheral B	Comments	Reset State	Power Supply	Function	Comments
PA0	SPI0_MISO	MCDA0		I/O	VDDIOP		
PA1	SPI0_MOSI	MCCDA		I/O	VDDIOP		
PA2	SPI0_SPCK	MCCK		I/O	VDDIOP		
PA3	SPI0_NPCS0			I/O	VDDIOP		
PA4	SPI0_NPCS1	MCDA1		I/O	VDDIOP		
PA5	SPI0_NPCS2	MCDA2		I/O	VDDIOP		
PA6	SPI0_NPCS3	MCDA3		I/O	VDDIOP		
PA7	TWD	PCK0		I/O	VDDIOP		
PA8	TWCK	PCK1		I/O	VDDIOP		
PA9	DRXD	PCK2		I/O	VDDIOP		
PA10	DTXD	PCK3		I/O	VDDIOP		
PA11	TSYNC	SCK1		I/O	VDDIOP		
PA12	TCLK	RTS1		I/O	VDDIOP		
PA13	TPS0	CTS1		I/O	VDDIOP		
PA14	TPS1	SCK2		I/O	VDDIOP		
PA15	TPS2	RTS2		I/O	VDDIOP		
PA16	TPK0	CTS2		I/O	VDDIOP		
PA17	TPK1	TF1		I/O	VDDIOP		
PA18	TPK2	TK1		I/O	VDDIOP		
PA19	TPK3	TD1		I/O	VDDIOP		
PA20	TPK4	RD1		I/O	VDDIOP		
PA21	TPK5	RK1		I/O	VDDIOP		
PA22	TPK6	RF1		I/O	VDDIOP		
PA23	TPK7	RTS0		I/O	VDDIOP		
PA24	TPK8	SPI1_NPCS1		I/O	VDDIOP		
PA25	TPK9	SPI1_NPCS2		I/O	VDDIOP		
PA26	TPK10	SPI1_NPCS3		I/O	VDDIOP		
PA27	TPK11	SPI0_NPCS1		I/O	VDDIOP		
PA28	TPK12	SPI0_NPCS2		I/O	VDDIOP		
PA29	TPK13	SPI0_NPCS3		I/O	VDDIOP		
PA30	TPK14	A23		A23	VDDIOM		
PA31	TPK15	A24		A24	VDDIOM		

10.3.3 PIO Controller B Multiplexing

Table 10-3. Multiplexing on PIO Controller B

PIO Controller B					Application Usage		
I/O Line	Peripheral A	Peripheral B	Comments	Reset State	Power Supply	Function	Comments
PB0	LCDVSYNC			I/O	VDDIOP		
PB1	LCDHSYNC			I/O	VDDIOP		
PB2	LCDDOTCK	PCK0		I/O	VDDIOP		
PB3[1]	LCDDEN		See footnote[1]	I/O	VDDIOP		
PB4	LCDCC	LCDD2		I/O	VDDIOP		
PB5	LCDD0	LCDD3		I/O	VDDIOP		
PB6	LCDD1	LCDD4		I/O	VDDIOP		
PB7	LCDD2	LCDD5		I/O	VDDIOP		
PB8	LCDD3	LCDD6		I/O	VDDIOP		
PB9	LCDD4	LCDD7		I/O	VDDIOP		
PB10	LCDD5	LCDD10		I/O	VDDIOP		
PB11	LCDD6	LCDD11		I/O	VDDIOP		
PB12	LCDD7	LCDD12		I/O	VDDIOP		
PB13	LCDD8	LCDD13		I/O	VDDIOP		
PB14	LCDD9	LCDD14		I/O	VDDIOP		
PB15	LCDD10	LCDD15		I/O	VDDIOP		
PB16	LCDD11	LCDD19		I/O	VDDIOP		
PB17	LCDD12	LCDD20		I/O	VDDIOP		
PB18	LCDD13	LCDD21		I/O	VDDIOP		
PB19	LCDD14	LCDD22		I/O	VDDIOP		
PB20	LCDD15	LCDD23		I/O	VDDIOP		
PB21	TF0	LCDD16		I/O	VDDIOP		
PB22	TK0	LCDD17		I/O	VDDIOP		
PB23	TD0	LCDD18		I/O	VDDIOP		
PB24	RD0	LCDD19		I/O	VDDIOP		
PB25	RK0	LCDD20		I/O	VDDIOP		
PB26	RF0	LCDD21		I/O	VDDIOP		
PB27	SPI1_NPCS1	LCDD22		I/O	VDDIOP		
PB28	SPI1_NPCS0	LCDD23		I/O	VDDIOP		
PB29	SPI1_SPCK	IRQ2		I/O	VDDIOP		
PB30	SPI1_MISO	IRQ1		I/O	VDDIOP		
PB31	SPI1_MOSI	PCK2		I/O	VDDIOP		

Note: 1. PB3 is multiplexed with BMS signal. Care should be taken during reset time.

10.3.4 PIO Controller C Multiplexing

Table 10-4. Multiplexing on PIO Controller C

PIO Controller C					Application Usage		
I/O Line	Peripheral A	Peripheral B	Comments	Reset State	Power Supply	Function	Comments
PC0	NANDOE	NCS6		I/O	VDDIOM		
PC1	NANDWE	NCS7		I/O	VDDIOP		
PC2	NWAIT	IRQ0		I/O	VDDIOP		
PC3	A25/CFRNW			A25	VDDIOP		
PC4	NCS4/CFCS0			I/O	VDDIOP		
PC5	NCS5/CFCS1			I/O	VDDIOP		
PC6	CFCE1			I/O	VDDIOP		
PC7	CFCE2			I/O	VDDIOM		
PC8	TXD0	PCK2		I/O	VDDIOP		
PC9	RXD0	PCK3		I/O	VDDIOP		
PC10	RTS0	SCK0		I/O	VDDIOP		
PC11	CTS0	FIQ		I/O	VDDIOP		
PC12	TXD1	NCS6		I/O	VDDIOP		
PC13	RXD1	NCS7		I/O	VDDIOP		
PC14	TXD2	SPI1_NPCS2		I/O	VDDIOP		
PC15	RXD2	SPI1_NPCS3		I/O	VDDIOP		
PC16	D16	TCLK0		I/O	VDDIOM		
PC17	D17	TCLK1		I/O	VDDIOM		
PC18	D18	TCLK2		I/O	VDDIOM		
PC19	D19	TIOA0		I/O	VDDIOM		
PC20	D20	TIOB0		I/O	VDDIOM		
PC21	D21	TIOA1		I/O	VDDIOM		
PC22	D22	TIOB1		I/O	VDDIOM		
PC23	D23	TIOA2		I/O	VDDIOM		
PC24	D24	TIOB2		I/O	VDDIOM		
PC25	D25	TF2		I/O	VDDIOM		
PC26	D26	TK2		I/O	VDDIOM		
PC27	D27	TD2		I/O	VDDIOM		
PC28	D28	RD2		I/O	VDDIOM		
PC29	D29	RK2		I/O	VDDIOM		
PC30	D30	RF2		I/O	VDDIOM		
PC31	D31	PCK1		I/O	VDDIOM		

10.5 Static Memory Controller

- External memory mapping, 256 Mbyte address space per Chip Select Line
- Up to Eight Chip Select Lines
- 8-, 16- or 32-bit Data Bus
- Multiple Access Modes supported
  - Byte Write or Byte Select Lines
  - Asynchronous read in Page Mode supported (4- up to 32-byte page size)
- Multiple device adaptability
  - Compliant with LCD Module
  - Control signal programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time
- Slow Clock Mode Supported

10.6 SDRAM Controller

- Supported Devices
  - Standard and Low Power SDRAM (Mobile SDRAM)
- Numerous configurations supported
  - 2K, 4K, 8K Row Address Memory Parts
  - SDRAM with two or four Internal Banks
  - SDRAM with 16- or 32-bit Data Path
- Programming Facilities
  - Word, half-word, byte access
  - Automatic page break when Memory Boundary has been reached
  - Multibank Ping-pong Access
  - Timing parameters specified by software
  - Automatic refresh operation, refresh rate is programmable
- Energy-saving Capabilities
  - Self-refresh, power down and deep power down modes supported
- Error detection
  - Refresh Error Interrupt
- SDRAM Power-up Initialization by software
- CAS Latency of 1, 2 and 3 supported
- Auto Precharge Command not used

10.7 Serial Peripheral Interface

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to fifteen peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

10.8 Two-wire Interface

- Compatibility with standard two-wire serial memories
- One, two or three bytes for slave address
- Sequential read/write operations
- Supports either master or slave modes
- Master, multi-master and slave mode operation
- Bit rate: up to 400 Kbits
- General call supported in slave mode

10.9 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - By-8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
  - Optional Manchester Encoding

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com
www.atmel.com/AT91SAM

Technical Support
AT91SAM Support
Atmel techincal support

Sales Contacts
www.atmel.com/contacts/

Literature Requests
www.atmel.com/literature