Infineon Technologies - SAK-XC167CI-16F20F BB Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	C166SV2
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, EBI/EMI, I²C, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	103
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	PG-TQFP-144-7
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-xc167ci-16f20f-bb

1 Summary of Features

- High Performance 16-bit CPU with 5-Stage Pipeline
  - 25 ns Instruction Cycle Time at 40 MHz CPU Clock (Single-Cycle Execution)
  - 1-Cycle Multiplication (16 ×16 bit), Background Division (32 / 16 bit) in 21 Cycles
  - 1-Cycle Multiply-and-Accumulate (MAC) Instructions
  - Enhanced Boolean Bit Manipulation Facilities
  - Zero-Cycle Jump Execution
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Fast Context Switching Support with Two Additional Local Register Banks
  - 16 Mbytes Total Linear Address Space for Code and Data
  - 1024 Bytes On-Chip Special Function Register Area (C166 Family Compatible)
- 16-Priority-Level Interrupt System with 77 Sources, Sample-Rate down to 50 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC), 24-Bit Pointers Cover Total Address Space
- Clock Generation via on-chip PLL (factors 1:0.15 … 1:10), or via Prescaler (factors 1:1 … 60:1)
- On-Chip Memory Modules
  - 2 Kbytes On-Chip Dual-Port RAM (DPRAM)
  - 4 Kbytes On-Chip Data SRAM (DSRAM)
  - 2 Kbytes On-Chip Program/Data SRAM (PSRAM)
  - 128 Kbytes On-Chip Program Memory (Flash Memory)
- On-Chip Peripheral Modules
  - 16-Channel A/D Converter with Programmable Resolution (10-bit or 8-bit) and Conversion Time (down to 2.55 µs or 2.15 µs)
  - Two 16-Channel General Purpose Capture/Compare Units (32 Input/Output Pins)
  - Capture/Compare Unit for flexible PWM Signal Generation (CAPCOM6) (3/6 Capture/Compare Channels and 1 Compare Channel)
  - Multi-Functional General Purpose Timer Unit with 5 Timers
  - Two Synchronous/Asynchronous Serial Channels (USARTs)
  - Two High-Speed-Synchronous Serial Channels
  - On-Chip TwinCAN Interface (Rev. 2.0B active) with 32 Message Objects (Full CAN/Basic CAN) on Two CAN Nodes, and Gateway Functionality
  - IIC Bus Interface (10-bit addressing, 400 kbit/s) with 3 Channels (multiplexed)
  - On-Chip Real Time Clock, Driven by Dedicated Oscillator
- Idle, Sleep, and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog

- Up to 12 Mbytes External Address Space for Code and Data
  - Programmable External Bus Characteristics for Different Address Ranges
  - Multiplexed or Demultiplexed External Address/Data Buses
  - Selectable Address Bus Width
  - 16-Bit or 8-Bit Data Bus Width
  - Five Programmable Chip-Select Signals
  - Hold- and Hold-Acknowledge Bus Arbitration Support
- Up to 103 General Purpose I/O Lines,
  partly with Selectable Input Thresholds and Hysteresis
- On-Chip Bootstrap Loader
- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Debug Support via JTAG Interface
- 144-Pin Green TQFP Package, 0.5 mm (19.7 mil) pitch (RoHS compliant)

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the XC167 please refer to the **“Product Catalog Microcontrollers”**, which summarizes all available microcontroller variants.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

This document describes several derivatives of the XC167 group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity all versions are referred to by the term **XC167** throughout this document.

Table 2 Pin Definitions and Functions

Sym-bol	Pin Num.	Input Outp.	Function
P20.12	3	IO	For details, please refer to the description of **P20**.
NMI	4	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the NMI pin must be low in order to force the XC167 into power down mode. If NMI is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin NMI should be pulled high externally.
P6		IO	Port 6 is an 8-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 6 is selectable (standard or special). The Port 6 pins also serve for alternate functions:
P6.0	7	O	CS0 Chip Select 0 Output,
		IO	CC0IO CAPCOM1: CC0 Capture Inp./Compare Output
P6.1	8	O	CS1 Chip Select 1 Output,
		IO	CC1IO CAPCOM1: CC1 Capture Inp./Compare Output
P6.2	9	O	CS2 Chip Select 2 Output,
		IO	CC2IO CAPCOM1: CC2 Capture Inp./Compare Output
P6.3	10	O	CS3 Chip Select 3 Output,
		IO	CC3IO CAPCOM1: CC3 Capture Inp./Compare Output
P6.4	11	O	CS4 Chip Select 4 Output,
		IO	CC4IO CAPCOM1: CC4 Capture Inp./Compare Output
P6.5	12	I	HOLD External Master Hold Request Input,
		IO	CC5IO CAPCOM1: CC5 Capture Inp./Compare Output
P6.6	13	I/O	HLDA Hold Acknowledge Output (master mode) or Input (slave mode),
		IO	CC6IO CAPCOM1: CC6 Capture Inp./Compare Output
P6.7	14	O	BREQ Bus Request Output,
		IO	CC7IO CAPCOM1: CC7 Capture Inp./Compare Output

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
XTAL2 XTAL1	137 138	O I	XTAL2: Output of the main oscillator amplifier circuit XTAL1: Input to the main oscillator amplifier and input to the internal clock generator To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed. *Note: Input pin XTAL1 belongs to the core voltage domain. Therefore, input voltages must be within the range defined for V_{DDI}.*
XTAL3 XTAL4	140 141	I O	XTAL3: Input to the auxiliary (32-kHz) oscillator amplifier XTAL4: Output of the auxiliary (32-kHz) oscillator amplifier circuit To clock the device from an external source, drive XTAL3, while leaving XTAL4 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed. *Note: Input pin XTAL3 belongs to the core voltage domain. Therefore, input voltages must be within the range defined for V_{DDI}.*
$\overline{\text{RSTIN}}$	142	I	Reset Input with Schmitt-Trigger characteristics. A low-level at this pin while the oscillator is running resets the XC167. A spike filter suppresses input pulses < 10 ns. Input pulses > 100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. *Note: The reset duration must be sufficient to let the hardware configuration signals settle.* *External circuitry must guarantee low-level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating range.*
$\overline{\text{BRK OUT}}$	143	O	Debug System: Break Out
$\overline{\text{BRKIN}}$	144	I	Debug System: Break In
NC	1, 2, 107 - 110	–	No connection. It is recommended not to connect these pins to the PCB.

3.2 External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes[1)], which are as follows:

- 16 … 24-bit Addresses, 16-bit Data, Demultiplexed
- 16 … 24-bit Addresses, 16-bit Data, Multiplexed
- 16 … 24-bit Addresses, 8-bit Data, Multiplexed
- 16 … 24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output. The high order address (segment) lines use Port 4. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines are assigned to Port 4.

Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. External modules can directly be connected to the common address/data bus and their individual select lines.

Access to very slow memories or modules with varying access times is supported via a particular ‘Ready’ function. The active level of the control input signal is selectable.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration and allows the sharing of external resources with other bus masters. The bus arbitration is enabled by software. After enabling, pins P6.7 … P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{HLDA}$ pin is an output. In Slave Mode pin $\overline{HLDA}$ is switched to input. This allows the direct connection of the slave controller to another master controller without glue logic.

Important timing characteristics of the external bus interface have been made programmable (via registers TCONCSx/FCONCSx) to allow the user the adaption of a wide range of different types of memories and external peripherals.

In addition, up to 4 independent address windows may be defined (via registers ADDRSELx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these 4 address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is related to the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

Table 4 XC167 Interrupt Nodes

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
CAPCOM Register 0	CC1_CC0IC	xx'0040$_H$	10$_H$ / 16$_D$
CAPCOM Register 1	CC1_CC1IC	xx'0044$_H$	11$_H$ / 17$_D$
CAPCOM Register 2	CC1_CC2IC	xx'0048$_H$	12$_H$ / 18$_D$
CAPCOM Register 3	CC1_CC3IC	xx'004C$_H$	13$_H$ / 19$_D$
CAPCOM Register 4	CC1_CC4IC	xx'0050$_H$	14$_H$ / 20$_D$
CAPCOM Register 5	CC1_CC5IC	xx'0054$_H$	15$_H$ / 21$_D$
CAPCOM Register 6	CC1_CC6IC	xx'0058$_H$	16$_H$ / 22$_D$
CAPCOM Register 7	CC1_CC7IC	xx'005C$_H$	17$_H$ / 23$_D$
CAPCOM Register 8	CC1_CC8IC	xx'0060$_H$	18$_H$ / 24$_D$
CAPCOM Register 9	CC1_CC9IC	xx'0064$_H$	19$_H$ / 25$_D$
CAPCOM Register 10	CC1_CC10IC	xx'0068$_H$	1A$_H$ / 26$_D$
CAPCOM Register 11	CC1_CC11IC	xx'006C$_H$	1B$_H$ / 27$_D$
CAPCOM Register 12	CC1_CC12IC	xx'0070$_H$	1C$_H$ / 28$_D$
CAPCOM Register 13	CC1_CC13IC	xx'0074$_H$	1D$_H$ / 29$_D$
CAPCOM Register 14	CC1_CC14IC	xx'0078$_H$	1E$_H$ / 30$_D$
CAPCOM Register 15	CC1_CC15IC	xx'007C$_H$	1F$_H$ / 31$_D$
CAPCOM Register 16	CC2_CC16IC	xx'00C0$_H$	30$_H$ / 48$_D$
CAPCOM Register 17	CC2_CC17IC	xx'00C4$_H$	31$_H$ / 49$_D$
CAPCOM Register 18	CC2_CC18IC	xx'00C8$_H$	32$_H$ / 50$_D$
CAPCOM Register 19	CC2_CC19IC	xx'00CC$_H$	33$_H$ / 51$_D$
CAPCOM Register 20	CC2_CC20IC	xx'00D0$_H$	34$_H$ / 52$_D$
CAPCOM Register 21	CC2_CC21IC	xx'00D4$_H$	35$_H$ / 53$_D$
CAPCOM Register 22	CC2_CC22IC	xx'00D8$_H$	36$_H$ / 54$_D$
CAPCOM Register 23	CC2_CC23IC	xx'00DC$_H$	37$_H$ / 55$_D$
CAPCOM Register 24	CC2_CC24IC	xx'00E0$_H$	38$_H$ / 56$_D$
CAPCOM Register 25	CC2_CC25IC	xx'00E4$_H$	39$_H$ / 57$_D$
CAPCOM Register 26	CC2_CC26IC	xx'00E8$_H$	3A$_H$ / 58$_D$
CAPCOM Register 27	CC2_CC27IC	xx'00EC$_H$	3B$_H$ / 59$_D$
CAPCOM Register 28	CC2_CC28IC	xx'00F0$_H$	3C$_H$ / 60$_D$

3.6 Capture/Compare Units (CAPCOM1/2)

The CAPCOM units support generation and control of timing sequences on up to 32 channels with a maximum resolution of 1 system clock cycle (8 cycles in staggered mode). The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for each capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture/compare registers relative to external events.

Both of the two capture/compare register arrays contain 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or compare function.
All registers of each module have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

Table 6 Compare Modes (CAPCOM1/2)

Compare Modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare timer overflow; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; can be used with any compare mode

count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM1/2 timers, and to cause a reload from the CAPREL register.

The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows the XC167 to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

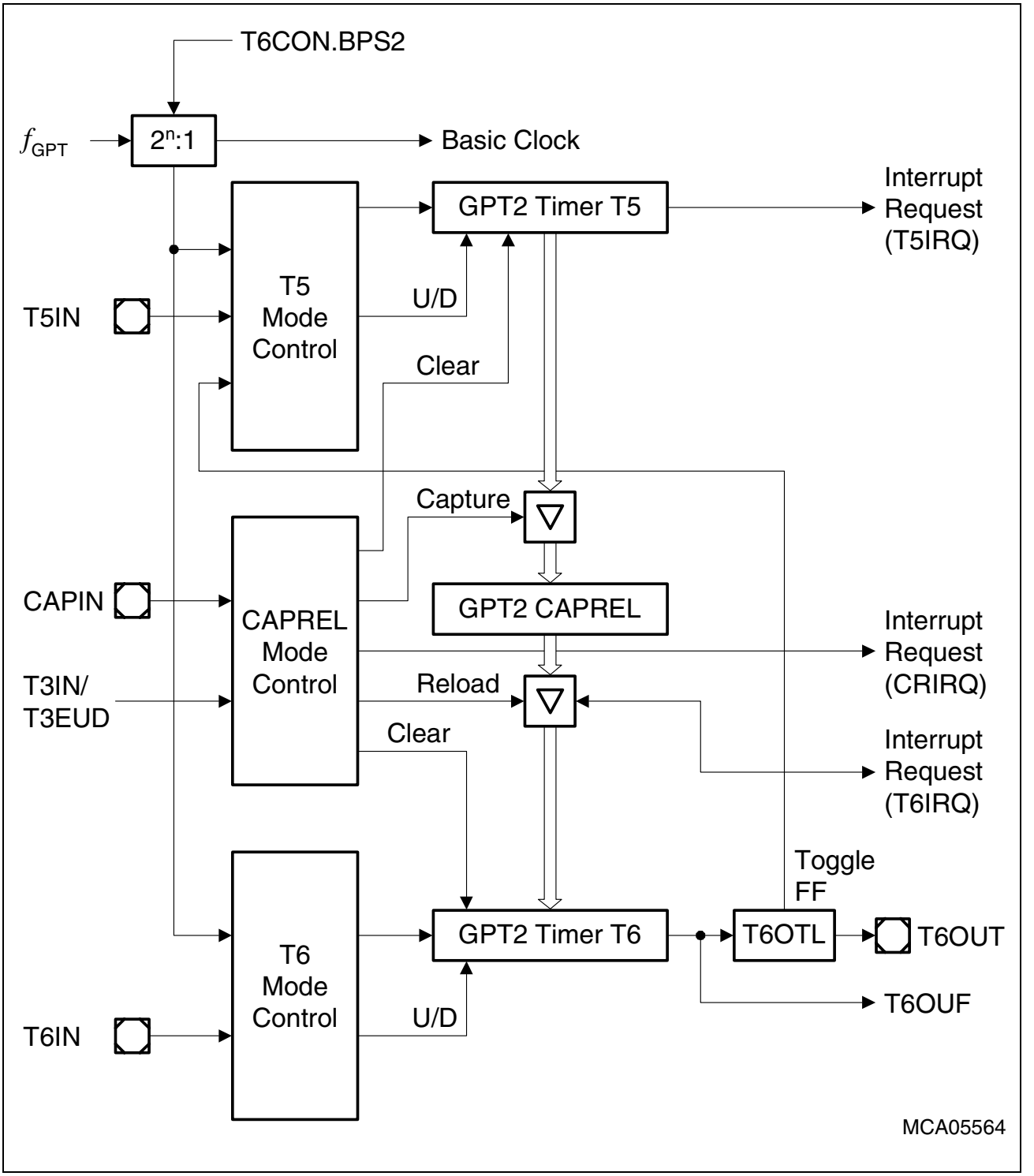

Figure 8 Block Diagram of GPT2

3.9 Real Time Clock

The Real Time Clock (RTC) module of the XC167 is directly clocked via a separate clock driver either with the on-chip auxiliary oscillator frequency (f_{RTC} = f_{OSCa}) or with the prescaled on-chip main oscillator frequency (f_{RTC} = f_{OSCm}/32). It is therefore independent from the selected clock generation mode of the XC167.

The RTC basically consists of a chain of divider blocks:

- a selectable 8:1 divider (on - off)
- the reloadable 16-bit timer T14
- the 32-bit RTC timer block (accessible via registers RTCH and RTCL), made of:
  - a reloadable 10-bit timer
  - a reloadable 6-bit timer
  - a reloadable 6-bit timer
  - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

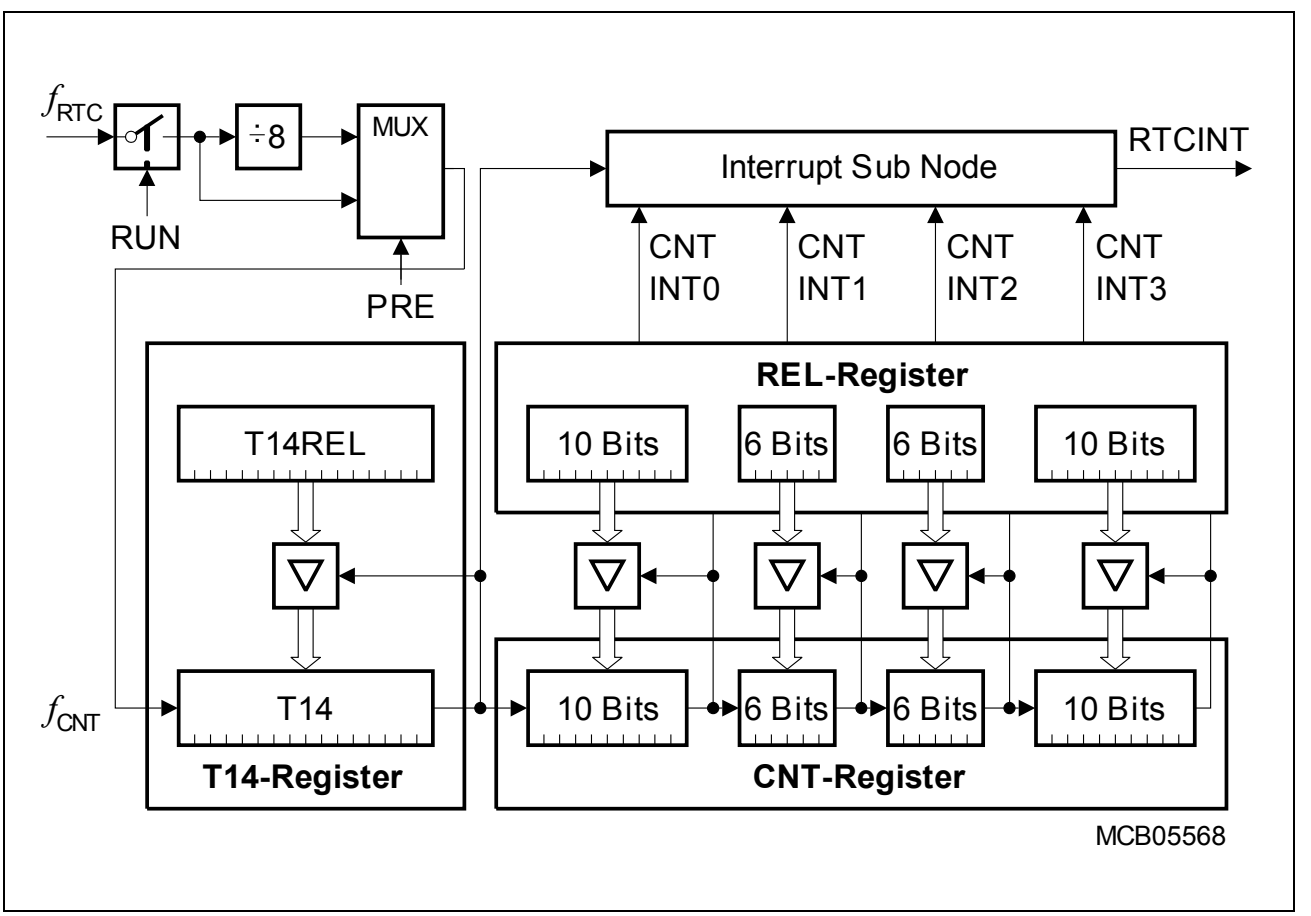

Figure 9 RTC Block Diagram

Note: The registers associated with the RTC are not affected by a reset in order to maintain the correct system time even when intermediate resets are executed.

3.18 Power Management

The XC167 provides several means to control the power it consumes either at a given time or averaged over a certain timespan. Three mechanisms can be used (partly in parallel):

- **Power Saving Modes** switch the XC167 into a special operating mode (control via instructions).
  Idle Mode stops the CPU while the peripherals can continue to operate.
  Sleep Mode and Power Down Mode stop all clock signals and all operation (RTC may optionally continue running). Sleep Mode can be terminated by external interrupt signals.
- **Clock Generation Management** controls the distribution and the frequency of internal and external clock signals. While the clock signals for currently inactive parts of logic are disabled automatically, the user can reduce the XC167's CPU clock frequency which drastically reduces the consumed power.
  External circuitry can be controlled via the programmable frequency output FOUT.
- **Peripheral Management** permits temporary disabling of peripheral modules (control via register SYSCON3). Each peripheral can separately be disabled/enabled.

The on-chip RTC supports intermittent operation of the XC167 by generating cyclic wake-up signals. This offers full performance to quickly react on action requests while the intermittent sleep phases greatly reduce the average power consumption of the system.

Table 8 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XC167. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 10 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Digital supply voltage for the core	V_{DDI}	2.35	2.7	V	Active mode, $f_{CPU} = f_{CPUmax}$ 1)2)
Digital supply voltage for IO pads	V_{DDP}	4.4	5.5	V	Active mode 2)
Supply Voltage Difference	ΔV_{DD}	-0.5	–	V	V_{DDP} - V_{DDI} 3)
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	-5	5	mA	Per IO pin 4)5)
		-2	5	mA	Per analog input pin 4)5)
Overload current coupling factor for analog inputs 6)	K_{OVA}	–	1.0×10^{-4}	–	$I_{OV} > 0$
		–	1.5×10^{-3}	–	$I_{OV} < 0$
Overload current coupling factor for digital I/O pins 6)	K_{OVD}	–	5.0×10^{-3}	–	$I_{OV} > 0$
		–	1.0×10^{-2}	–	$I_{OV} < 0$
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	–	50	mA	5)
External Load Capacitance	C_L	–	50	pF	Pin drivers in **default** mode 7)
Ambient temperature	T_A	–	–	°C	see **Table 1**

1) f_{CPUmax} = 40 MHz for devices marked … 40F, f_{CPUmax} = 20 MHz for devices marked … 20F.

2) External circuitry must guarantee low level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached their operating range.

3) This limitation must be fulfilled under all operating conditions including power-ramp-up, power-ramp-down, and power-save modes.

4) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{DDP} + 0.5$ V ($I_{OV} > 0$) or $V_{OV} < V_{SS} - 0.5$ V ($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltages must remain within the specified limits.
Proper operation is not guaranteed if overload conditions occur on functional pins such as XTAL1, $\overline{\text{RD}}$, $\overline{\text{WR}}$, etc.

5) Not subject to production test - verified by design/characterization.

4.3 Analog/Digital Converter Parameters

Table 14 A/D Converter Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Analog reference supply	V_{AREF}	SR	4.5	V_{DDP} + 0.1	V	1)
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.1	V_{SS} + 0.1	V	–
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	2)
Basic clock frequency	f_{BC}		0.5	20	MHz	3)
Conversion time for 10-bit result[4]	t_{C10P}	CC	$52 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. on
	t_{C10}	CC	$40 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. off
Conversion time for 8-bit result[4]	t_{C8P}	CC	$44 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. on
	t_{C8}	CC	$32 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. off
Calibration time after reset	t_{CAL}	CC	484	11,696	t_{BC}	5)
Total unadjusted error	TUE	CC	–	±2	LSB	1)
Total capacitance of an analog input	C_{AINT}	CC	–	15	pF	6)
Switched capacitance of an analog input	C_{AINS}	CC	–	10	pF	6)
Resistance of the analog input path	R_{AIN}	CC	–	2	kΩ	6)
Total capacitance of the reference input	C_{AREFT}	CC	–	20	pF	6)
Switched capacitance of the reference input	C_{AREFS}	CC	–	15	pF	6)
Resistance of the reference input path	R_{AREF}	CC	–	1	kΩ	6)

1) TUE is tested at $V_{AREF} = V_{DDP} + 0.1$ V, $V_{AGND} = 0$ V. It is verified by design for all other voltages within the defined voltage range.
If the analog reference supply voltage drops below 4.5 V (i.e. $V_{AREF} \geq 4.0$ V) or exceeds the power supply voltage by up to 0.2 V (i.e. $V_{AREF} = V_{DDP} + 0.2$ V) the maximum TUE is increased to ±3 LSB. This range is not subject to production test.
The specified TUE is guaranteed only, if the absolute sum of input overload currents on Port 5 pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the respective period of time. During the reset calibration sequence the maximum TUE may be ±4 LSB.

2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

4.4 AC Parameters

4.4.1 Definition of Internal Timing

The internal operation of the XC167 is controlled by the internal master clock f_{MC}.

The master clock signal f_{MC} can be generated from the oscillator clock signal f_{OSC} via different mechanisms. The duration of master clock periods (TCMs) and their variation (and also the derived external timing) depend on the used mechanism to generate f_{MC}. This influence must be regarded when calculating the timings for the XC167.

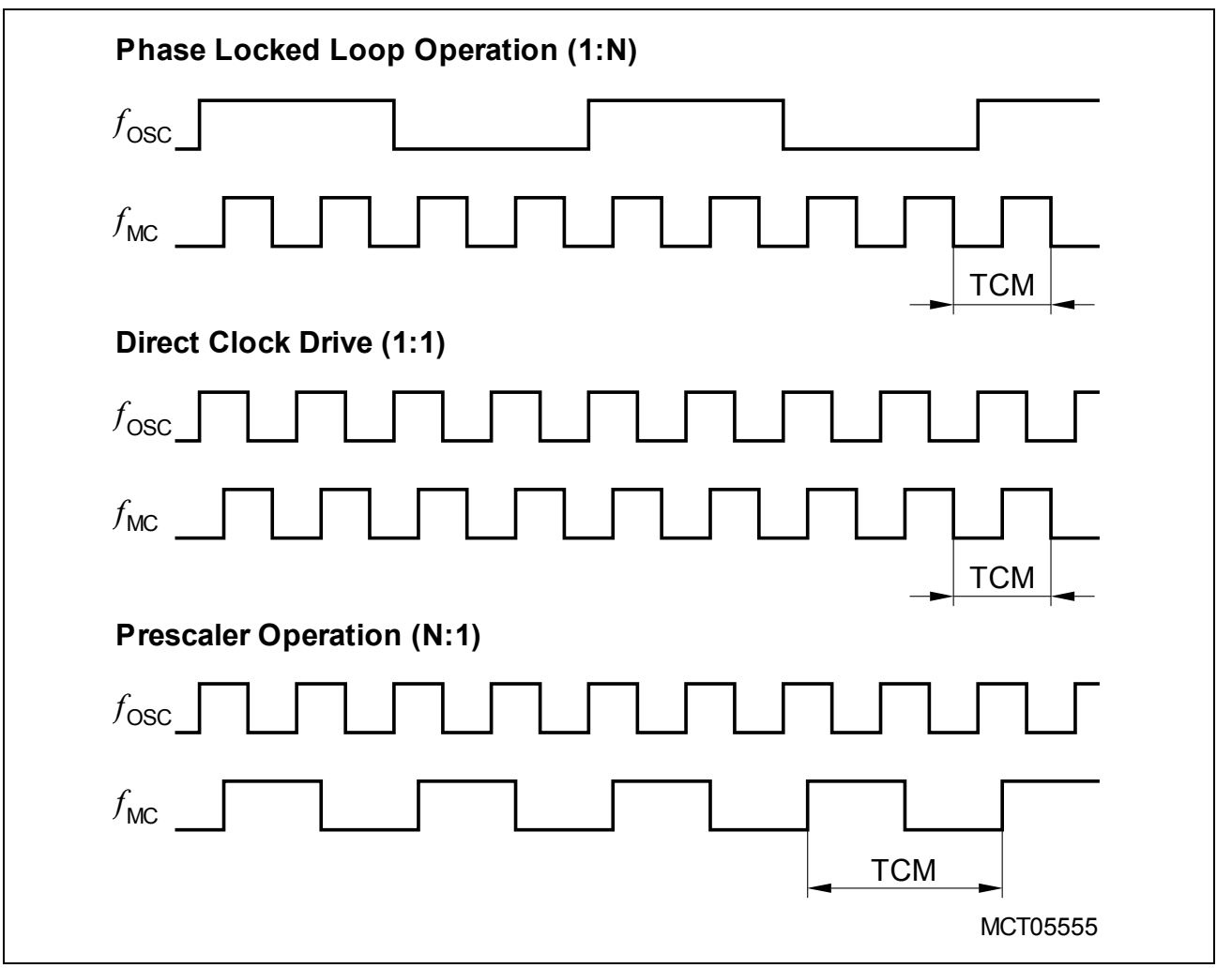

Figure 15 Generation Mechanisms for the Master Clock

*Note: The example for PLL operation shown in **Figure 15** refers to a PLL factor of 1:4, the example for prescaler operation refers to a divider factor of 2:1.*

The used mechanism to generate the master clock is selected by register PLLCON.

CPU and EBC are clocked with the CPU clock signal f_{CPU}. The CPU clock can have the same frequency as the master clock ($f_{CPU} = f_{MC}$) or can be the master clock divided by two: $f_{CPU} = f_{MC} / 2$. This factor is selected by bit CPSYS in register SYSCON1.

4.4.5 External Bus Timing

Table 20 CLKOUT Reference Signal

Parameter	Symbol		Limits		Unit
			Min.	Max.	
CLKOUT cycle time	tc_5	CC	40/30/25[1]		ns
CLKOUT high time	tc_6	CC	8	–	ns
CLKOUT low time	tc_7	CC	6	–	ns
CLKOUT rise time	tc_8	CC	–	4	ns
CLKOUT fall time	tc_9	CC	–	4	ns

1) The CLKOUT cycle time is influenced by the PLL jitter (given values apply to f_{CPU} = 25/33/40 MHz). For longer periods the relative deviation decreases (see PLL deviation formula).

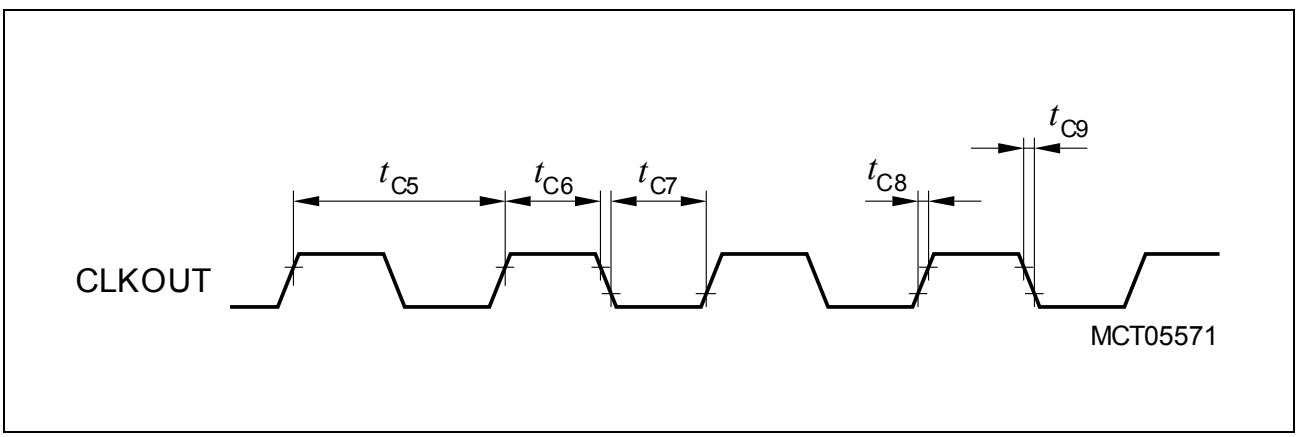

Figure 20 CLKOUT Signal Timing

Bus Cycle Control via READY Input

The duration of an external bus cycle can be controlled by the external circuitry via the READY input signal. The polarity of this input signal can be selected.

Synchronous READY permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

Asynchronous READY puts no timing constraints on the input signal but incurs one waitstate minimum due to the additional synchronization stage. The minimum duration of an asynchronous READY signal to be safely synchronized must be one CLKOUT period plus the input setup time.

An active READY signal can be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{RD}$ or $\overline{WR}$).

If the next following bus cycle is READY-controlled, an active READY signal must be disabled before the first valid sample point for the next bus cycle. This sample point depends on the programmed phases of the next following cycle.

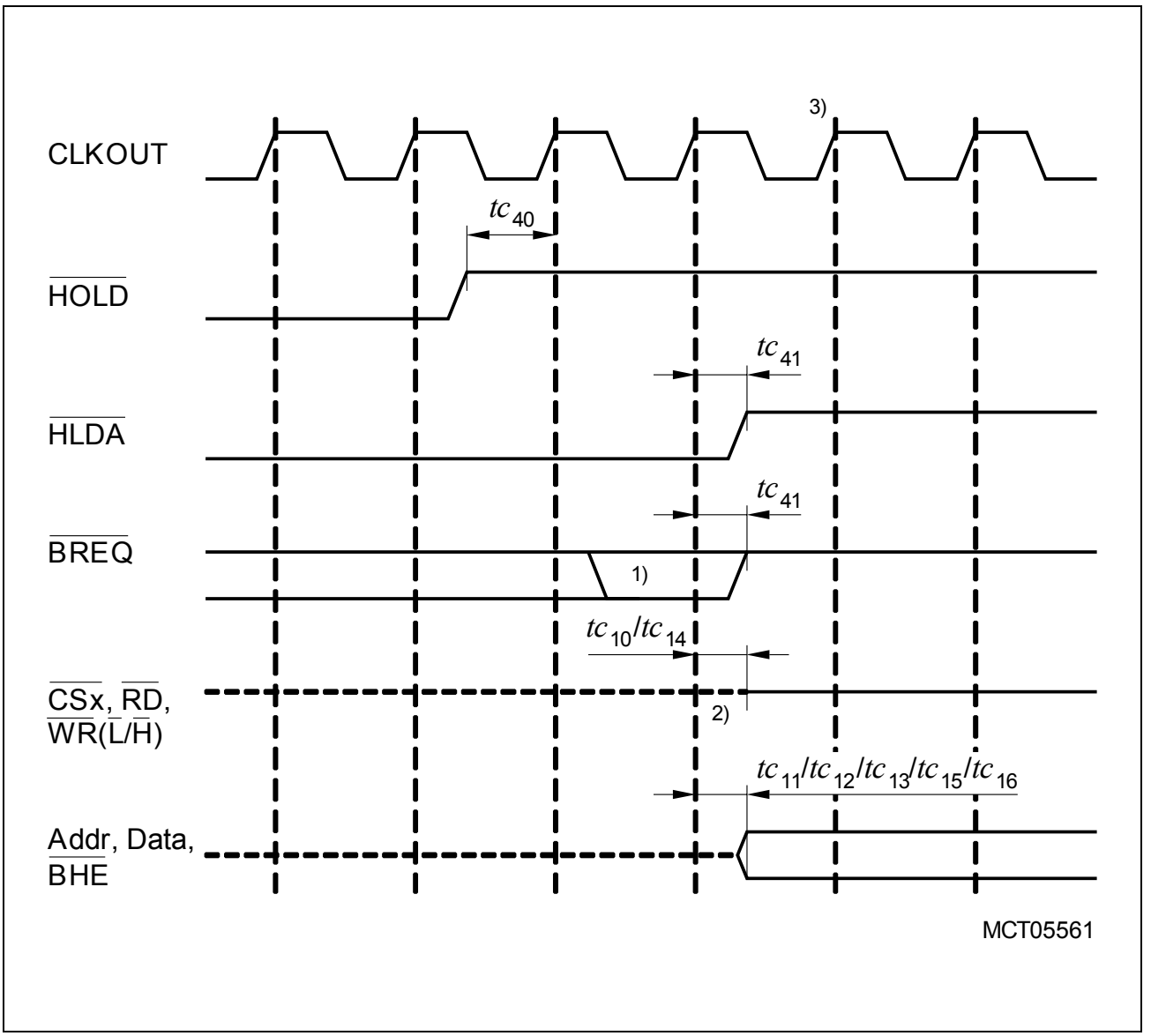

Figure 25 External Bus Arbitration, Regaining the Bus

Notes

1. *This is the last chance for $\overline{BREQ}$ to trigger the indicated regain-sequence. Even if $\overline{BREQ}$ is activated earlier, the regain-sequence is initiated by $\overline{HOLD}$ going high. Please note that $\overline{HOLD}$ may also be deactivated without the XC167 requesting the bus.*
2. *The control outputs will be resistive high (pull-up) before being driven inactive (ALE will be low).*
3. *The next XC167 driven bus cycle may start here.*

5.2 Flash Memory Parameters

The data retention time of the XC167's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Table 25 Flash Parameters (XC167, 128 Kbytes)

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Data retention time	t_{RET}	15	–	years	10^3 erase/program cycles
Flash Erase Endurance	N_{ER}	20×10^3	–	cycles	Data retention time 5 years

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