Infineon Technologies - SAK-XC167CI-16F40F BB Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	103
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	PG-TQFP-144-7
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-xc167ci-16f40f-bb

Edition 2006-08

Published by
Infineon Technologies AG
81726 München, Germany

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1 Summary of Features

- High Performance 16-bit CPU with 5-Stage Pipeline
  - 25 ns Instruction Cycle Time at 40 MHz CPU Clock (Single-Cycle Execution)
  - 1-Cycle Multiplication (16 ×16 bit), Background Division (32 / 16 bit) in 21 Cycles
  - 1-Cycle Multiply-and-Accumulate (MAC) Instructions
  - Enhanced Boolean Bit Manipulation Facilities
  - Zero-Cycle Jump Execution
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Fast Context Switching Support with Two Additional Local Register Banks
  - 16 Mbytes Total Linear Address Space for Code and Data
  - 1024 Bytes On-Chip Special Function Register Area (C166 Family Compatible)
- 16-Priority-Level Interrupt System with 77 Sources, Sample-Rate down to 50 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC), 24-Bit Pointers Cover Total Address Space
- Clock Generation via on-chip PLL (factors 1:0.15 … 1:10), or via Prescaler (factors 1:1 … 60:1)
- On-Chip Memory Modules
  - 2 Kbytes On-Chip Dual-Port RAM (DPRAM)
  - 4 Kbytes On-Chip Data SRAM (DSRAM)
  - 2 Kbytes On-Chip Program/Data SRAM (PSRAM)
  - 128 Kbytes On-Chip Program Memory (Flash Memory)
- On-Chip Peripheral Modules
  - 16-Channel A/D Converter with Programmable Resolution (10-bit or 8-bit) and Conversion Time (down to 2.55 µs or 2.15 µs)
  - Two 16-Channel General Purpose Capture/Compare Units (32 Input/Output Pins)
  - Capture/Compare Unit for flexible PWM Signal Generation (CAPCOM6) (3/6 Capture/Compare Channels and 1 Compare Channel)
  - Multi-Functional General Purpose Timer Unit with 5 Timers
  - Two Synchronous/Asynchronous Serial Channels (USARTs)
  - Two High-Speed-Synchronous Serial Channels
  - On-Chip TwinCAN Interface (Rev. 2.0B active) with 32 Message Objects (Full CAN/Basic CAN) on Two CAN Nodes, and Gateway Functionality
  - IIC Bus Interface (10-bit addressing, 400 kbit/s) with 3 Channels (multiplexed)
  - On-Chip Real Time Clock, Driven by Dedicated Oscillator
- Idle, Sleep, and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog

2.2 Pin Configuration and Definition

The pins of the XC167 are described in detail in **Table 2**, including all their alternate functions. **Figure 2** summarizes all pins in a condensed way, showing their location on the 4 sides of the package. E*) and C*) mark pins to be used as alternate external interrupt inputs, C*) marks pins that can have CAN interface lines assigned to them.

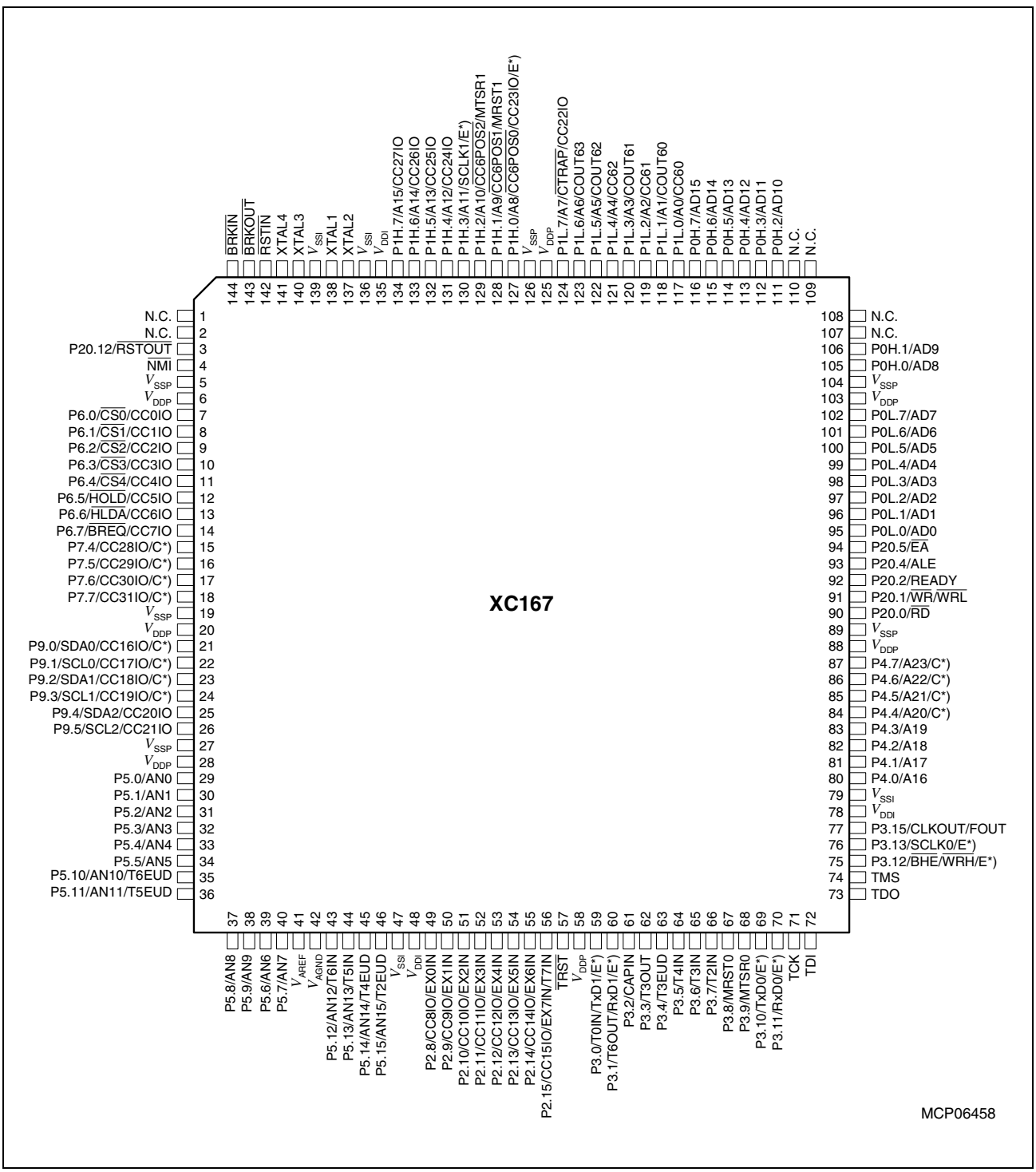


Figure 2 Pin Configuration (top view)

Table 2 Pin Definitions and Functions

Sym-bol	Pin Num.	Input Outp.	Function
P20.12	3	IO	For details, please refer to the description of **P20**.
NMI	4	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the NMI pin must be low in order to force the XC167 into power down mode. If NMI is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin NMI should be pulled high externally.
P6		IO	Port 6 is an 8-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 6 is selectable (standard or special). The Port 6 pins also serve for alternate functions:
P6.0	7	O	CS0 Chip Select 0 Output,
		IO	CC0IO CAPCOM1: CC0 Capture Inp./Compare Output
P6.1	8	O	CS1 Chip Select 1 Output,
		IO	CC1IO CAPCOM1: CC1 Capture Inp./Compare Output
P6.2	9	O	CS2 Chip Select 2 Output,
		IO	CC2IO CAPCOM1: CC2 Capture Inp./Compare Output
P6.3	10	O	CS3 Chip Select 3 Output,
		IO	CC3IO CAPCOM1: CC3 Capture Inp./Compare Output
P6.4	11	O	CS4 Chip Select 4 Output,
		IO	CC4IO CAPCOM1: CC4 Capture Inp./Compare Output
P6.5	12	I	HOLD External Master Hold Request Input,
		IO	CC5IO CAPCOM1: CC5 Capture Inp./Compare Output
P6.6	13	I/O	HLDA Hold Acknowledge Output (master mode) or Input (slave mode),
		IO	CC6IO CAPCOM1: CC6 Capture Inp./Compare Output
P6.7	14	O	BREQ Bus Request Output,
		IO	CC7IO CAPCOM1: CC7 Capture Inp./Compare Output

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
P7		IO	Port 7 is a 4-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 7 is selectable (standard or special). Port 7 pins provide inputs/outputs for CAPCOM2 and serial interface lines.[1)]
P7.4	15	I/O I I	CC28IO CAPCOM2: CC28 Capture Inp./Compare Outp., CAN2_RxD CAN Node 2 Receive Data Input, EX7IN Fast External Interrupt 7 Input (alternate pin B)
P7.5	16	I/O O I	CC29IO CAPCOM2: CC29 Capture Inp./Compare Outp., CAN2_TxD CAN Node 2 Transmit Data Output, EX6IN Fast External Interrupt 6 Input (alternate pin B)
P7.6	17	I/O I I	CC30IO CAPCOM2: CC30 Capture Inp./Compare Outp., CAN1_RxD CAN Node 1 Receive Data Input, EX7IN Fast External Interrupt 7 Input (alternate pin A)
P7.7	18	I/O O I	CC31IO CAPCOM2: CC31 Capture Inp./Compare Outp., CAN1_TxD CAN Node 1 Transmit Data Output, EX6IN Fast External Interrupt 6 Input (alternate pin A)

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
P4		IO	Port 4 is an 8-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 4 is selectable (standard or special). Port 4 can be used to output the segment address lines, the optional chip select lines, and for serial interface lines:[1)]
P4.0	80	O	A16 Least Significant Segment Address Line
P4.1	81	O	A17 Segment Address Line
P4.2	82	O	A18 Segment Address Line
P4.3	83	O	A19 Segment Address Line
P4.4	84	O	A20 Segment Address Line,
		I	CAN2_RxD CAN Node 2 Receive Data Input,
		I	EX5IN Fast External Interrupt 5 Input (alternate pin B)
P4.5	85	O	A21 Segment Address Line,
		I	CAN1_RxD CAN Node 1 Receive Data Input,
		I	EX4IN Fast External Interrupt 4 Input (alternate pin B)
P4.6	86	O	A22 Segment Address Line,
		O	CAN1_TxD CAN Node 1 Transmit Data Output,
		I	EX5IN Fast External Interrupt 5 Input (alternate pin A)
P4.7	87	O	A23 Most Significant Segment Address Line,
		I	CAN1_RxD CAN Node 1 Receive Data Input,
		O	CAN2_TxD CAN Node 2 Transmit Data Output,
		I	EX4IN Fast External Interrupt 4 Input (alternate pin A)

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function	
PORT1		IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. Each pin can be programmed for input (output driver in high-impedance state) or output. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes (also after switching from a demultiplexed to a multiplexed bus mode). The following PORT1 pins also serve for alt. functions:	
P1L.0	117	I/O	CC60	CAPCOM6: Input / Output of Channel 0
P1L.1	118	O	COUT60	CAPCOM6: Output of Channel 0
P1L.2	119	I/O	CC61	CAPCOM6: Input / Output of Channel 1
P1L.3	120	O	COUT61	CAPCOM6: Output of Channel 1
P1L.4	121	I/O	CC62	CAPCOM6: Input / Output of Channel 2
P1L.5	122	O	COUT62	CAPCOM6: Output of Channel 2
P1L.6	123	O	$\overline{\text{COUT63}}$	Output of 10-bit Compare Channel
P1L.7	124	I	$\overline{\text{CTRAP}}$	$\overline{\text{CAPCOM2}}$: CC22 Capture Inp./Compare Outp. $\overline{\text{CTRAP}}$ is an input pin with an internal pull-up resistor. A low level on this pin switches the CAPCOM6 compare outputs to the logic level defined by software (if enabled).
		I/O	$\overline{\text{CC22IO}}$	CAPCOM2: CC22 Capture Inp./Compare Outp.
P1H.0	127	I	$\overline{\text{CC6POS0}}$	CAPCOM6: Position 0 Input,
		I	EX0IN	Fast External Interrupt 0 Input (alternate pin B),
		I/O	$\overline{\text{CC23IO}}$	CAPCOM2: CC23 Capture Inp./Compare Outp.
P1H.1	128	I	$\overline{\text{CC6POS1}}$	CAPCOM6: Position 1 Input,
		I/O	$\overline{\text{MRST1}}$	SSC1 Master-Receive/Slave-Transmit In/Out.
P1H.2	129	I	$\overline{\text{CC6POS2}}$	CAPCOM6: Position 2 Input,
		I/O	MTSR1	SSC1 Master-Transmit/Slave-Receive Out/Inp.
P1H.3	130	I/O	SCLK1	SSC1 Master Clock Output / Slave Clock Input,
		I	EX0IN	Fast External Interrupt 0 Input (alternate pin A)
P1H.4	131	I/O	CC24IO	CAPCOM2: CC24 Capture Inp./Compare Outp.
P1H.5	132	I/O	CC25IO	CAPCOM2: CC25 Capture Inp./Compare Outp.
P1H.6	133	I/O	CC26IO	CAPCOM2: CC26 Capture Inp./Compare Outp.
P1H.7	134	I/O	CC27IO	CAPCOM2: CC27 Capture Inp./Compare Outp.

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
XTAL2 XTAL1	137 138	O I	XTAL2: Output of the main oscillator amplifier circuit XTAL1: Input to the main oscillator amplifier and input to the internal clock generator To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed. *Note: Input pin XTAL1 belongs to the core voltage domain. Therefore, input voltages must be within the range defined for V_{DDI}.*
XTAL3 XTAL4	140 141	I O	XTAL3: Input to the auxiliary (32-kHz) oscillator amplifier XTAL4: Output of the auxiliary (32-kHz) oscillator amplifier circuit To clock the device from an external source, drive XTAL3, while leaving XTAL4 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed. *Note: Input pin XTAL3 belongs to the core voltage domain. Therefore, input voltages must be within the range defined for V_{DDI}.*
$\overline{\text{RSTIN}}$	142	I	Reset Input with Schmitt-Trigger characteristics. A low-level at this pin while the oscillator is running resets the XC167. A spike filter suppresses input pulses < 10 ns. Input pulses > 100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. *Note: The reset duration must be sufficient to let the hardware configuration signals settle.* *External circuitry must guarantee low-level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating range.*
$\overline{\text{BRK OUT}}$	143	O	Debug System: Break Out
$\overline{\text{BRKIN}}$	144	I	Debug System: Break In
NC	1, 2, 107 - 110	–	No connection. It is recommended not to connect these pins to the PCB.

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
V_{AREF}	41	–	Reference voltage for the A/D converter.
V_{AGND}	42	–	Reference ground for the A/D converter.
V_{DDI}	48, 78, 135	–	Digital Core Supply Voltage (On-Chip Modules): +2.5 V during normal operation and idle mode. Please refer to the **Operating Conditions**.
V_{DDP}	6, 20, 28, 58, 88, 103, 125	–	Digital Pad Supply Voltage (Pin Output Drivers): +5 V during normal operation and idle mode. Please refer to the **Operating Conditions**.
V_{SSI}	47, 79, 136, 139	–	**Digital Ground** Connect decoupling capacitors to adjacent V_{DD}/V_{SS} pin pairs as close as possible to the pins. All V_{SS} pins must be connected to the ground-line or ground-plane.
V_{SSP}	5, 19, 27, 89, 104, 126	–	

1) The CAN interface lines are assigned to ports P4, P7, and P9 under software control.

3.8 General Purpose Timer (GPT12E) Unit

The GPT12E unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.
Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

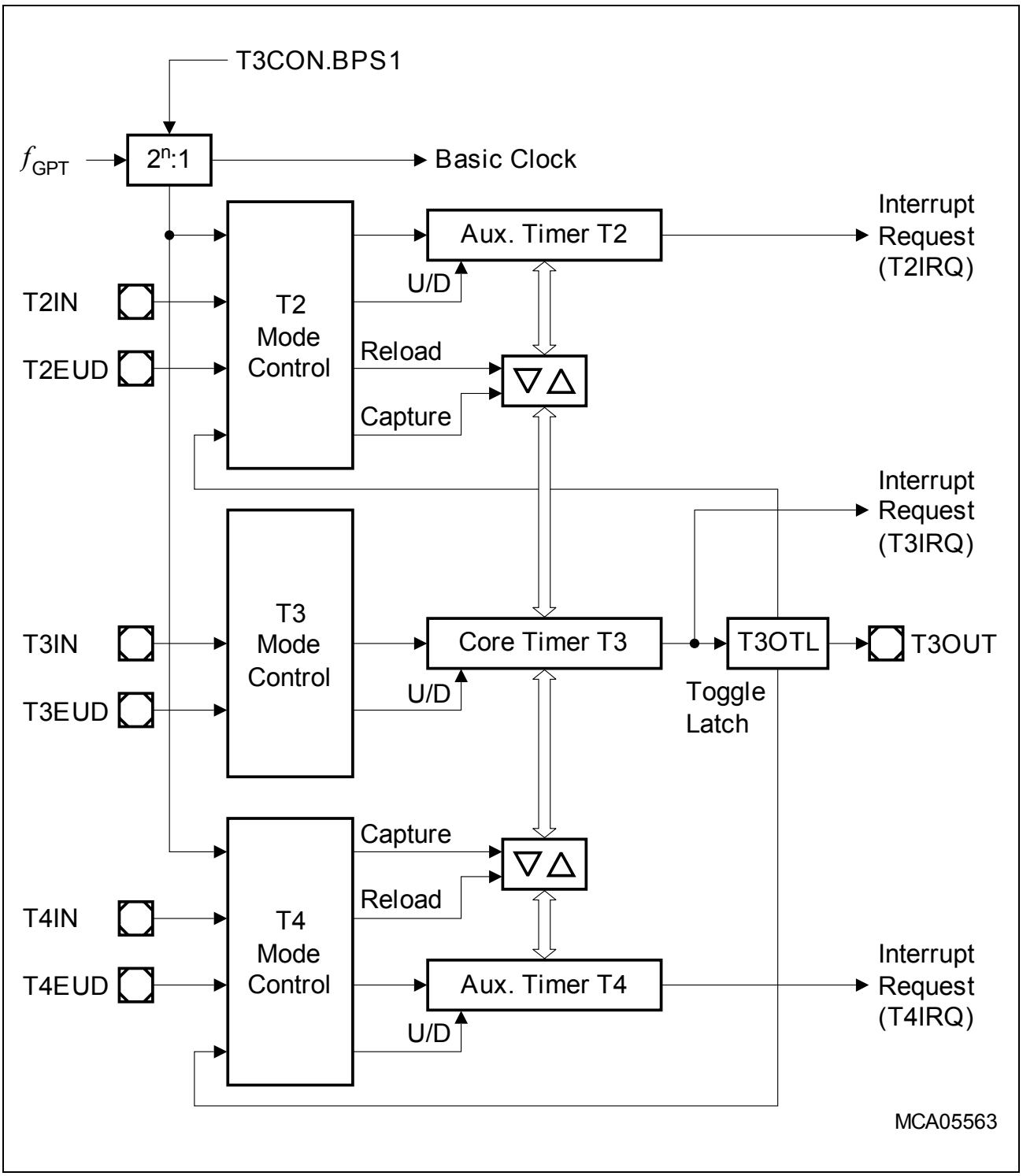


Figure 7 Block Diagram of GPT1

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The

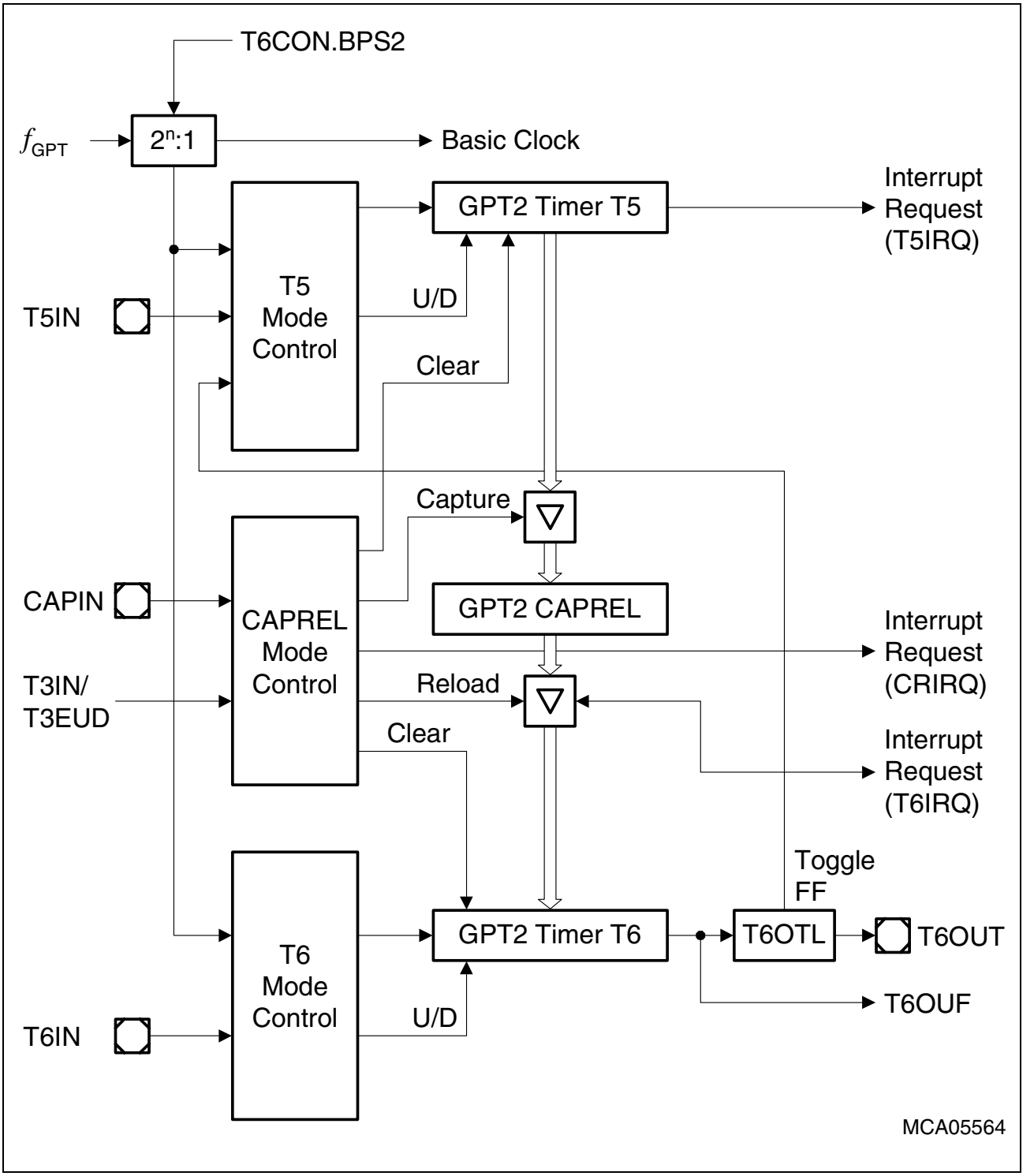


Figure 8 Block Diagram of GPT2

3.10 A/D Converter

For analog signal measurement, a 10-bit A/D converter with 16 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable (in two modes) and can thus be adjusted to the external circuitry. The A/D converter can also operate in 8-bit conversion mode, where the conversion time is further reduced.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the XC167 supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels are sequentially sampled and converted. In the Auto Scan Continuous mode, the prespecified channels are repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (e.g. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital IO or input stages under software control. This can be selected for each pin separately via register P5DIDIS (Port 5 Digital Input Disable).

The Auto-Power-Down feature of the A/D converter minimizes the power consumption when no conversion is in progress.

Table 12 Current Limits for Port Output Drivers

Port Output Driver Mode	Maximum Output Current (I_{OLmax}, $-I_{OHmax}$)[1]	Nominal Output Current (I_{OLnom}, $-I_{OHnom}$)
Strong driver	10 mA	2.5 mA
Medium driver	4.0 mA	1.0 mA
Weak driver	0.5 mA	0.1 mA

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring port output pins the total output current in each direction (ΣI_{OL} and $\Sigma -I_{OH}$) must remain below 50 mA.

Table 13 Power Consumption XC167 (Operating Conditions apply)

Parameter	Sym-bol	Limit Values		Unit	Test Condition
		Min.	Max.		
Power supply current (active) with all peripherals active	I_{DDI}	–	15 + 2.6 × f_{CPU}	mA	f_{CPU} in [MHz][1)2)]
Pad supply current	I_{DDP}	–	5	mA	[3)]
Idle mode supply current with all peripherals active	I_{IDX}	–	15 + 1.2 × f_{CPU}	mA	f_{CPU} in [MHz][2)]
Sleep and Power down mode supply current caused by leakage[4)]	I_{PDL}[5)]	–	128,000 × $e^{-\alpha}$	mA	V_{DDI} = V_{DDImax}[6)] T_J in [°C] α = 4670 / (273 + T_J)
Sleep and Power down mode supply current caused by leakage and the RTC running, clocked by the main oscillator[4)]	I_{PDM}[7)]	–	0.6 + 0.02 × f_{OSC} + I_{PDL}	mA	V_{DDI} = V_{DDImax} f_{OSC} in [MHz]
Sleep and Power down mode supply current caused by leakage and the RTC running, clocked by the auxiliary oscillator at 32 kHz[4)]	I_{PDA}	–	0.1 + I_{PDL}	mA	V_{DDI} = V_{DDImax}

1) During Flash programming or erase operations the supply current is increased by max. 5 mA.

2) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 11**. These parameters are tested at V_{DDImax} and maximum CPU clock frequency with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

3) The pad supply voltage pins (V_{DDP}) mainly provides the current consumed by the pin output drivers. A small amount of current is consumed even though no outputs are driven, because the drivers' input stages are switched and also the Flash module draws some power from the V_{DDP} supply.

Table 16 VCO Bands for PLL Operation[1)]

PLLCON.PLLVB	VCO Frequency Range	Base Frequency Range
00	100 … 150 MHz	20 … 80 MHz
01	150 … 200 MHz	40 … 130 MHz
10	200 … 250 MHz	60 … 180 MHz
11	Reserved	

1) Not subject to production test - verified by design/characterization.

4.4.3 External Clock Drive XTAL1

Table 19 External Clock Drive Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
Oscillator period	t_{OSC}	SR	25	250[1)]	ns
High time[2)]	t_1	SR	6	–	ns
Low time[2)]	t_2	SR	6	–	ns
Rise time[2)]	t_3	SR	–	8	ns
Fall time[2)]	t_4	SR	–	8	ns

1) The maximum limit is only relevant for PLL operation to ensure the minimum input frequency for the PLL.

2) The clock input signal must reach the defined levels V_{ILC} and V_{IHC}.

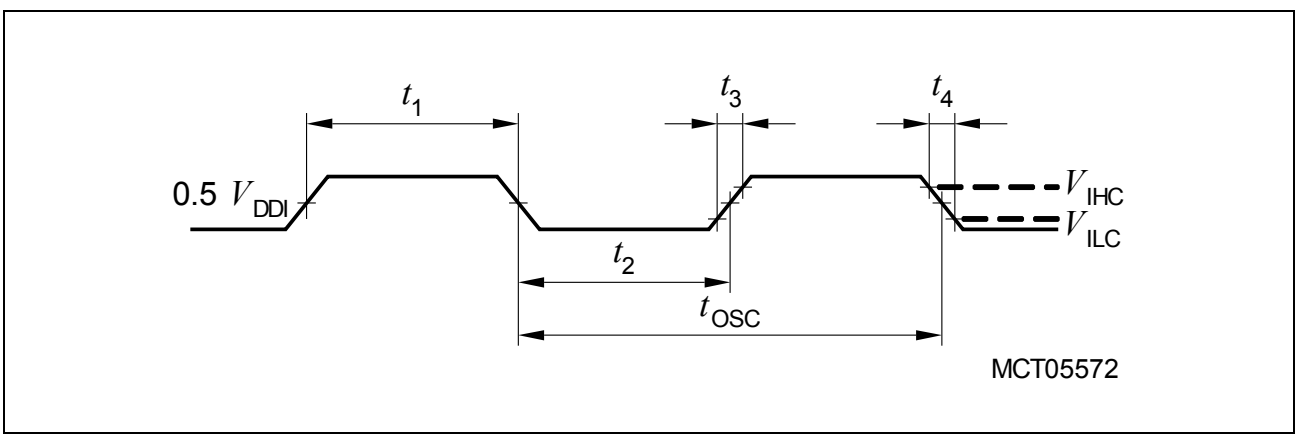


Figure 17 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal or a ceramic resonator, the oscillator frequency is limited to a range of 4 MHz to 16 MHz.
It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.
When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is verified by design only (not subject to production test).

Variable Memory Cycles

External bus cycles of the XC167 are executed in five subsequent cycle phases (AB, C, D, E, F). The duration of each cycle phase is programmable (via the TCONCSx registers) to adapt the external bus cycles to the respective external module (memory, peripheral, etc.).

The duration of the access phase can optionally be controlled by the external module via the READY handshake input.

This table provides a summary of the phases and the respective choices for their duration.

Table 21 Programmable Bus Cycle Phases (see timing diagrams)

Bus Cycle Phase	Parameter	Valid Values	Unit
Address setup phase, the standard duration of this phase (1 … 2 TCP) can be extended by 0 … 3 TCP if the address window is changed	tp_{AB}	1 … 2 (5)	TCP
Command delay phase	tp_{C}	0 … 3	TCP
Write Data setup/MUX Tristate phase	tp_{D}	0 … 1	TCP
Access phase	tp_{E}	1 … 32	TCP
Address/Write Data hold phase	tp_{F}	0 … 3	TCP

Note: The bandwidth of a parameter (minimum and maximum value) covers the whole operating range (temperature, voltage) as well as process variations. Within a given device, however, this bandwidth is smaller than the specified range. This is also due to interdependencies between certain parameters. Some of these interdependencies are described in additional notes (see standard timing).

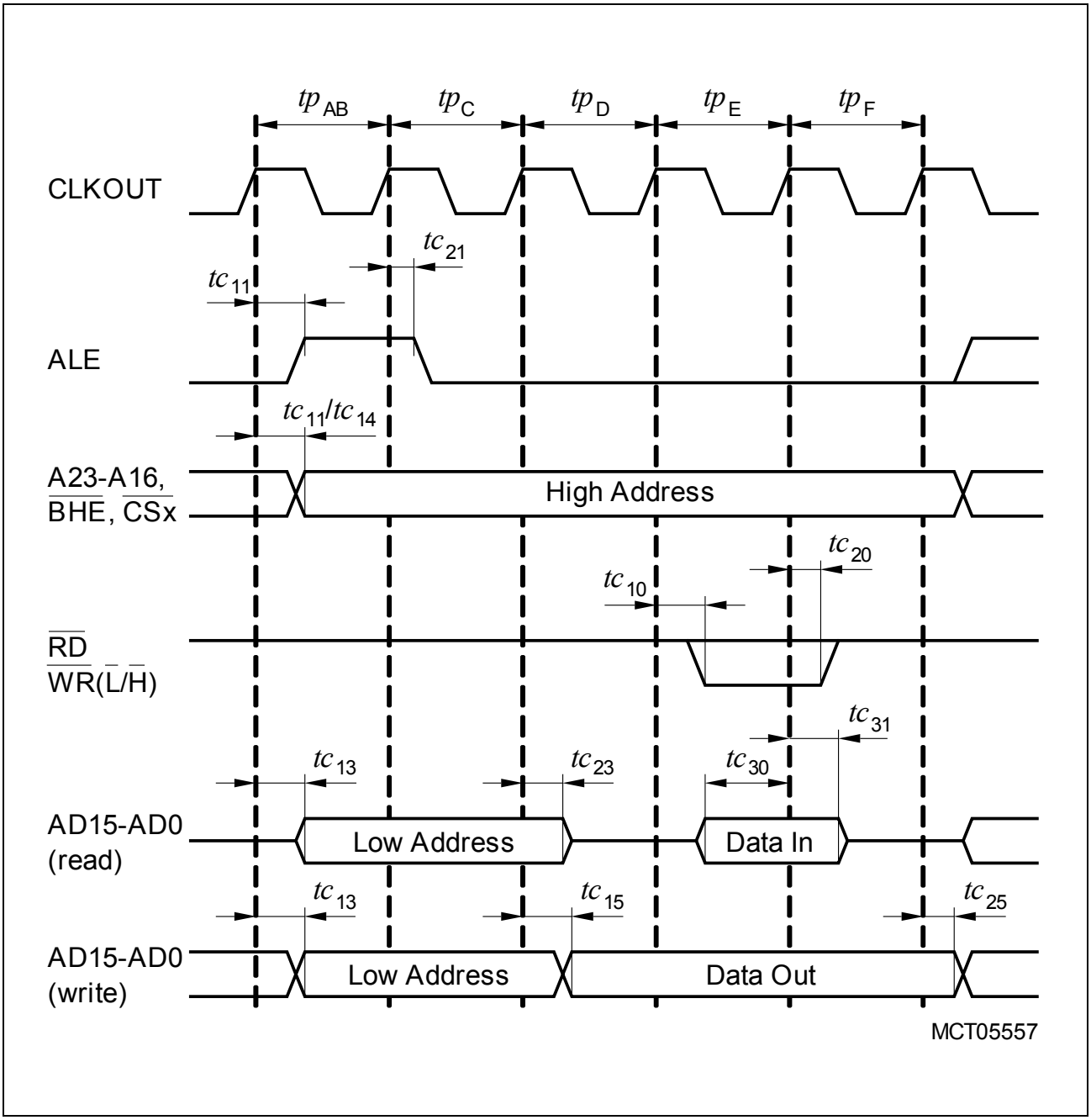
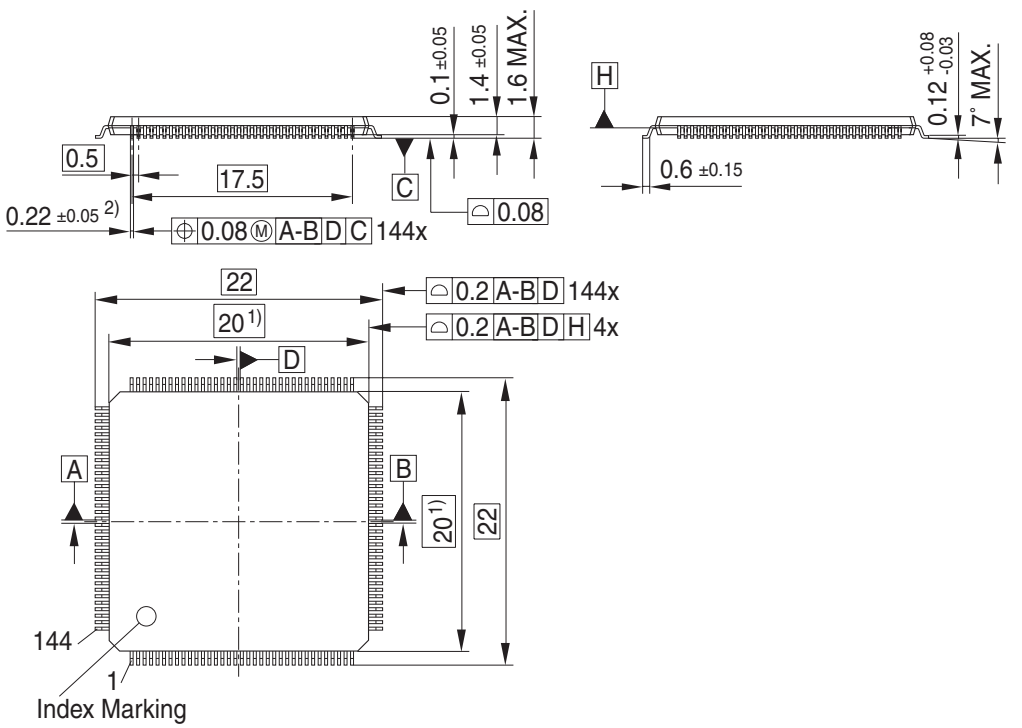


Figure 21 Multiplexed Bus Cycle



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

GPP09243

Figure 27 **P-TQFP-144-19** (Plastic Thin Quad Flat Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**. Dimensions in mm

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