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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

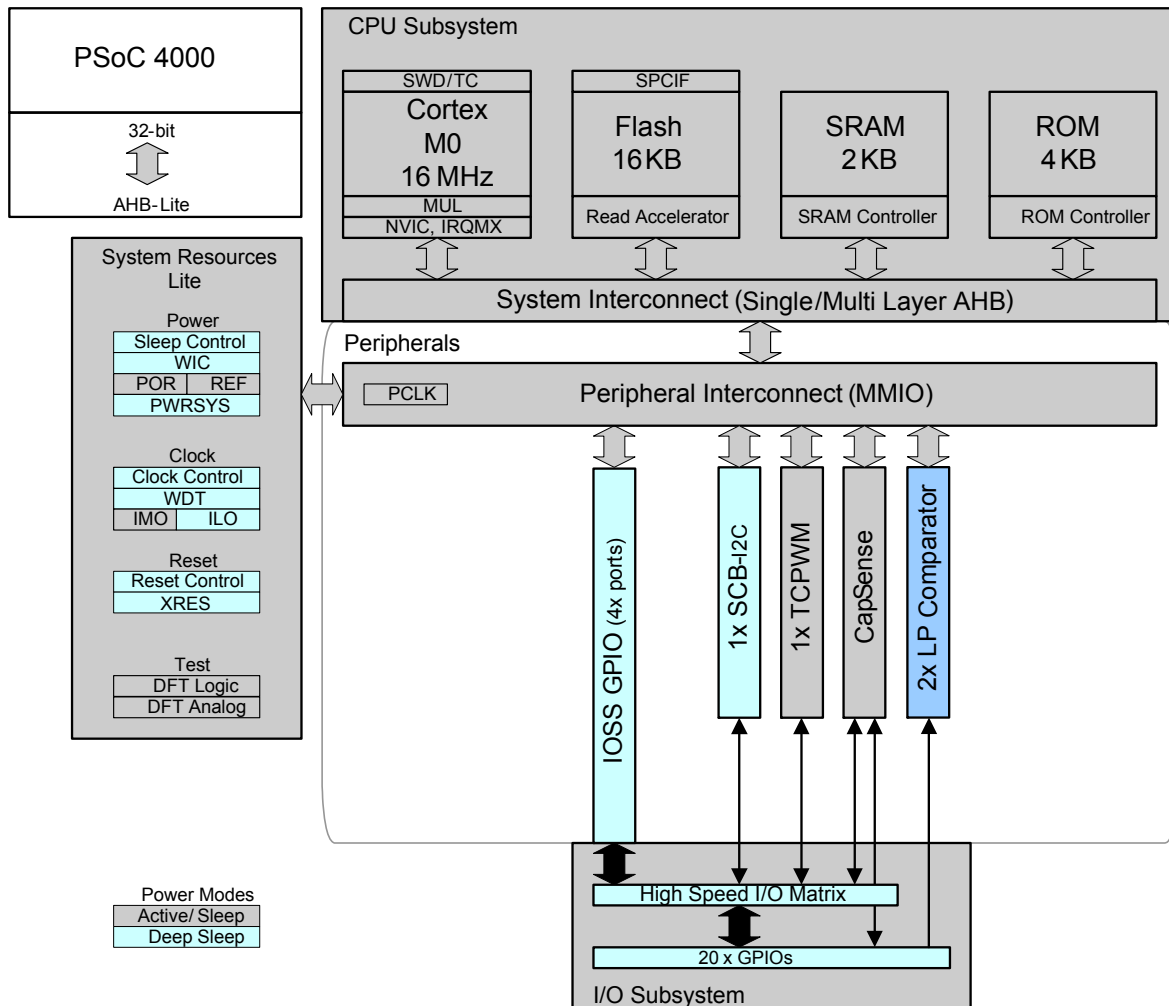
Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	16MHz
Connectivity	I ² C
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	D/A 1x7b, 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4014sxa-421t

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Block Diagram



Functional Description

PSoC 4000 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4000 devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4000 family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features

- Robust flash protection

- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can only be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4000, with device security enabled, will have only limited capability for failure analysis. This is a trade-off the PSoC 4000 allows the customer to make.

Functional Overview

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in the PSoC 4000 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. This enables fully compatible, binary, upward migration of the code to higher performance processors, such as the Cortex-M3 and M4. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode.

The CPU also includes a debug interface, the SWD interface, which is a 2-wire form of JTAG. The debug configuration used for PSoC 4000 has four breakpoint (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4000 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver zero wait-state (WS) access time at 16 MHz. The flash accelerator delivers 85% of the single-cycle SRAM access performance on average.

SRAM

Two KB of SRAM are provided with zero wait-state access at 16 MHz.

SRAM

A supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section on [Power on page 8](#). It provides an assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4000 operates with a single external supply over the range of either 1.8 V \pm 5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4000 provides Active, Sleep, and Deep Sleep low-power modes.

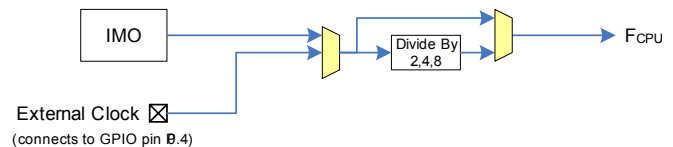
All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 μ S.

Clock System

The PSoC 4000 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4000 consists of the internal main oscillator (IMO) and the internal low-frequency oscillator (ILO) and provision for an external clock.

Figure 1. PSoC 4000 MCU Clocking Architecture



The F_{CPU} signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are four clock dividers for the PSoC 4000, each with 16-bit divide capability. The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC Creator.

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4000. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is \pm 2% (24 and 32 MHz).

ILO Clock Source

The ILO is a very low power, 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

Reset

The PSoC 4000 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset on the 24-pin package. An internal POR is provided on the 16-pin package. The XRES pin has an internal pull-up resistor that is always enabled.

Voltage Reference

The PSoC 4000 reference system generates all internally required references. A 1.2-V voltage reference is provided for the comparator. The IDACs are based on a \pm 5% reference.

Descriptions of the Pin functions are as follows:

VDD: Power supply for both analog and digital sections.

VSS: Ground pin.

VCCD: Regulated digital supply (1.8 V \pm 5%).

Pins belonging to Ports 0, 1, and 2 can all be used as CSD sense and shield pins can be connected to AMUXBUS A or B or can all be used as GPIO pins that can be driven by the firmware.

Pins on Port 3 can be used as GPIO, in addition to their alternate functions listed above.

The following packages are provided: 24-pin QFN and 16-pin SOIC.

Figure 2. 24-pin QFN Pinout

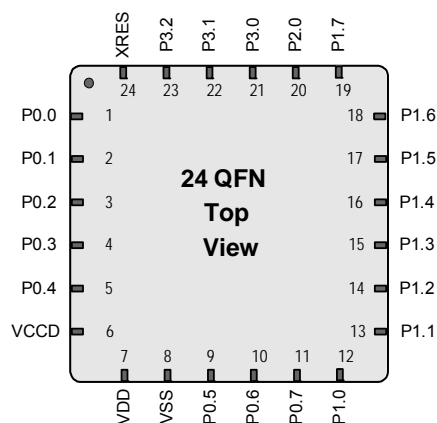
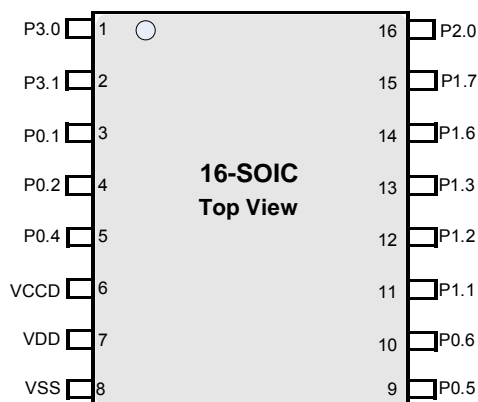


Figure 3. 16-pin SOIC Pinout



Power

The following power system diagrams (Figure 4 and Figure 5) show the set of power supply pins as implemented for the PSoC 4000. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DD} input. There is a separate regulator for the Deep Sleep mode. The supply voltage range is either 1.8 V \pm 5% (externally regulated) or 1.8 V to 5.5 V (unregulated externally; regulated internally) with all functions and circuits operating over that range.

The PSoC 4000 family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply.

Unregulated External Supply

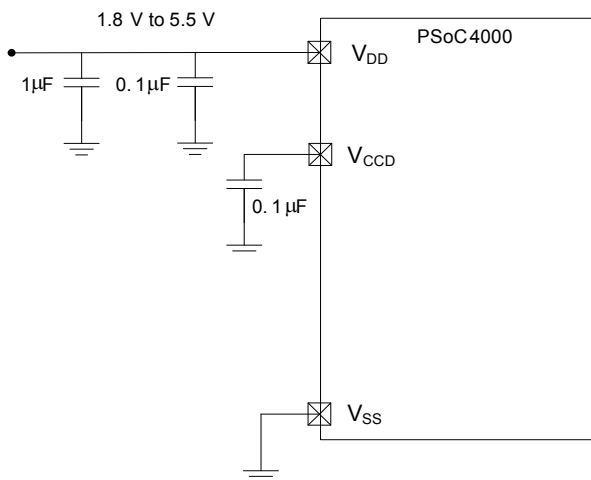
In this mode, the PSoC 4000 is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4000 supplies the internal logic and the V_{CCD} output of the PSoC 4000 must be bypassed to ground via an external capacitor (0.1 μ F; X5R ceramic or better).

Bypass capacitors must be used from V_{DD} to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1- μ F range, in parallel with a smaller capacitor (0.1 μ F, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme follows (V_{DDIO} is available on the 16-QFN package).

Figure 4. 24-pin QFN Bypass Scheme Example - Unregulated External Supply

Power supply connections when $1.8 \leq V_{DD} \leq 5.5$ V

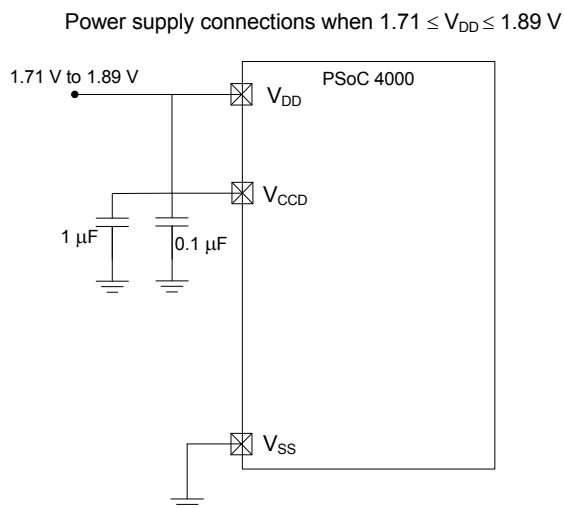


Regulated External Supply

In this mode, the PSoC 4000 is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the V_{DD} and V_{CCD} pins are shorted together and bypassed. The internal regulator is disabled in the firmware.

An example of a bypass scheme follows.

Figure 5. 24-pin QFN Bypass Scheme Example - Regulated External Supply



Development Support

The PSoC 4000 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC 4000 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often

include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4000 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Electrical Specifications

Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings^[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V _{DDD_ABS}	Digital supply relative to V _{SS}	–0.5	–	6	V	
SID2	V _{CCD_ABS}	Direct digital core voltage input relative to V _{SS}	–0.5	–	1.95	V	
SID3	V _{GPIO_ABS}	GPIO voltage	–0.5	–	V _{DD} +0.5	V	
SID4	I _{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
SID5	I _{GPIO_injection}	GPIO injection current, Max for V _{IH} > V _{DDD} , and Min for V _{IL} < V _{SS}	–0.5	–	0.5	mA	Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	
BID46	LU	Pin current for latch-up	–140	–	140	mA	

Note

- Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

Device Level Specifications

All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ for A grade devices and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$ for S grade devices, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 3. DC Specifications

Typical values measured at $V_{DD} = 3.3\text{ V}$ and $25\text{ }^{\circ}\text{C}$.

Spec ID#	Parameter	Description	Min	Typ	Max ^[2]	Units	Details/ Conditions
SID53	V_{DD}	Power supply input voltage	1.8	–	5.5	V	With regulator enabled
SID255	V_{DD}	Power supply input voltage ($V_{CCD} = V_{DD}$)	1.71	–	1.89	V	Internally unregulated supply
SID54	V_{DDIO}	V_{DDIO} domain supply	1.71	–	V_{DD}	V	
SID55	C_{EFC}	External regulator voltage bypass	–	0.1	–	μF	X5R ceramic or better
SID56	C_{EXC}	Power supply bypass capacitor	–	1	–	μF	X5R ceramic or better
Active Mode, $V_{DD} = 1.8$ to 5.5 V							
SID9	I_{DD5}	Execute from flash; CPU at 6 MHz	–	2.0	2.85	mA	
SID12	I_{DD8}	Execute from flash; CPU at 12 MHz	–	3.2	3.75	mA	
SID16	I_{DD11}	Execute from flash; CPU at 16 MHz	–	4.0	4.5	mA	
Sleep Mode, $V_{DD} = 1.71$ to 5.5 V							
SID25	I_{DD20}	$I^2\text{C}$ wakeup, WDT on. 6 MHz	–	1.1	–	mA	
SID25A	I_{DD20A}	$I^2\text{C}$ wakeup, WDT on. 12 MHz	–	1.4	–	mA	
Deep Sleep Mode, $V_{DD} = 1.8$ to 3.6 V (Regulator on)							
SID31	I_{DD26}	$I^2\text{C}$ wakeup and WDT on	–	2.5	8.2	μA	
Deep Sleep Mode, $V_{DD} = 3.6$ to 5.5 V (Regulator on)							
SID34	I_{DD29}	$I^2\text{C}$ wakeup and WDT on	–	2.5	12	μA	
Deep Sleep Mode, $V_{DD} = V_{CCD} = 1.71$ to 1.89 V (Regulator bypassed)							
SID37	I_{DD32}	$I^2\text{C}$ wakeup and WDT on	–	2.5	9.2	μA	
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2	5	mA	

Note

2. Maximum values corresponds to values at higher temperature ($105\text{ }^{\circ}\text{C}$).

Table 4. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F _{CPU}	CPU frequency	DC	–	16	MHz	1.71 ≤ V _{DD} ≤ 5.5
SID49 ^[3]	T _{SLEEP}	Wakeup from Sleep mode	–	0	–	μs	
SID50 ^[3]	T _{DEEPSLEEP}	Wakeup from Deep Sleep mode	–	35	–	μs	

GPIO

Table 5. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	V _{IH} ^[4]	Input voltage high threshold	0.7 × V _{DD}	–	–	V	CMOS Input
SID58	V _{IL}	Input voltage low threshold	–	–	0.3 × V _{DD}	V	CMOS Input
SID241	V _{IH} ^[4]	LVTTL input, V _{DD} < 2.7 V	0.7 × V _{DD}	–	–	V	
SID242	V _{IL}	LVTTL input, V _{DD} < 2.7 V	–	–	0.3 × V _{DD}	V	
SID243	V _{IH} ^[4]	LVTTL input, V _{DD} ≥ 2.7 V	2.0	–	–	V	
SID244	V _{IL}	LVTTL input, V _{DD} ≥ 2.7 V	–	–	0.8	V	
SID59	V _{OH}	Output voltage high level	V _{DD} – 0.6	–	–	V	I _{OH} = 4 mA at 3 V V _{DD}
SID60	V _{OH}	Output voltage high level	V _{DD} – 0.5	–	–	V	I _{OH} = 1 mA at 1.8 V V _{DD}
SID61	V _{OL}	Output voltage low level	–	–	0.6	V	I _{OL} = 4 mA at 1.8 V V _{DD}
SID62	V _{OL}	Output voltage low level	–	–	0.6	V	I _{OL} = 10 mA at 3 V V _{DD}
SID62A	V _{OL}	Output voltage low level	–	–	0.4	V	I _{OL} = 3 mA at 3 V V _{DD}
SID63	R _{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	R _{PULLDOWN}	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID65	I _{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V _{DD} = 3.0 V
SID66	C _{IN}	Input capacitance	–	3	7	pF	
SID67 ^[5]	V _{HYSTTL}	Input hysteresis LVTTL	15	40	–	mV	V _{DD} ≥ 2.7 V
SID68 ^[5]	V _{HYSCMOS}	Input hysteresis CMOS	0.05 × V _{DD}	–	–	mV	V _{DD} < 4.5 V
SID68A ^[5]	V _{HYSCMOS5V5}	Input hysteresis CMOS	200	–	–	mV	V _{DD} > 4.5 V
SID69 ^[5]	I _{DIODE}	Current through protection diode to V _{DD} /V _{SS}	–	–	100	μA	
SID69A ^[5]	I _{TOT_GPIO}	Maximum total source or sink chip current	–	–	85	mA	

Notes

3. Guaranteed by characterization.
4. V_{IH} must not exceed V_{DD} + 0.2 V.
5. Guaranteed by characterization.

Table 6. GPIO AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DD} , Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12	ns	3.3 V V_{DD} , Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	–	3.3 V V_{DD} , Cload = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	–	3.3 V V_{DD} , Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO F_{OUT} ; 3.3 V $\leq V_{DD} \leq 5.5$ V. Fast strong mode.	–	–	16	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO F_{OUT} ; 1.71 V $\leq V_{DD} \leq 3.3$ V. Fast strong mode.	–	–	16	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO F_{OUT} ; 3.3 V $\leq V_{DD} \leq 5.5$ V. Slow strong mode.	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO F_{OUT} ; 1.71 V $\leq V_{DD} \leq 3.3$ V. Slow strong mode.	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V $\leq V_{DD} \leq 5.5$ V	–	–	16	MHz	90/10% V_{IO}

XRES
Table 7. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	$0.7 \times V_{DD}$	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	$0.3 \times V_{DD}$	V	CMOS Input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	k Ω	
SID80	C_{IN}	Input capacitance	–	3	7	pF	
SID81 ^[6]	$V_{HYSXRES}$	Input voltage hysteresis	–	05* V_{DD}	–	mV	Typical hysteresis is 200 mV for V_{DD} > 4.5V

Table 8. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83 ^[6]	$T_{RESETWIDTH}$	Reset pulse width	5	–	–	μ s	
BID#194 ^[6]	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	3	ms	

Note

6. Guaranteed by characterization.

Analog Peripherals

Comparator

Table 9. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID330 ^[6]	I _{CMP1}	Block current, High Bandwidth mode	–	–	110	μA	
SID331 ^[6]	I _{CMP2}	Block current, Low Power mode	–	–	85	μA	
SID332 ^[6]	V _{OFFSET1}	Offset voltage, High Bandwidth mode	–	10	30	mV	
SID333 ^[6]	V _{OFFSET2}	Offset voltage, Low Power mode	–	10	30	V	
SID334 ^[6]	Z _{CMP}	DC input impedance of comparator	35	–	–	MΩ	
SID338 ^[6]	VINP_COMP	Comparator input range	0	–	3.6	V	Max input voltage is lower of 3.6 V or V _{DD}

Table 10. Comparator AC Specifications (Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID336 ^[6]	T _{COMP1}	Response Time High Bandwidth mode, 50-mV overdrive	–	–	90	ns	
SID337 ^[6]	T _{COMP2}	Response Time Low Power mode, 50-mV overdrive	–	–	110	ns	

Memory

Table 15. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V _{PE}	Erase and program voltage	1.71	–	5.5	V	

Table 16. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	T _{ROWWRITE} ^[9]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	T _{ROWERASE} ^[9]	Row erase time	–	–	13	ms	
SID176	T _{ROWPROGRAM} ^[9]	Row program time after erase	–	–	7	ms	
SID178	T _{BULKERASE} ^[9]	Bulk erase time (16 KB)	–	–	15	ms	
SID180 ^[10]	T _{DEVPROG} ^[9]	Total device program time	–	–	7.5	seconds	
SID181 ^[10]	F _{END}	Flash endurance	100 K	–	–	cycles	
SID182 ^[10]	F _{RET}	Flash retention. T _A ≤ 55 °C, 100 K P/E cycles	20 ^[11]	–	–	years	
SID182A ^[10]		Flash retention. T _A ≤ 85 °C, 10 K P/E cycles	10 ^[12]	–	–	years	

System Resources

Power-on Reset (POR)

Table 17. Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185 ^[10]	V _{RISEIPOR}	Rising trip voltage	0.80	–	1.5	V	
SID186 ^[10]	V _{FALLIPOR}	Falling trip voltage	0.70	–	1.4	V	

Table 18. Brown-out Detect (BOD) for V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190 ^[10]	V _{FALLPPOR}	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	
SID192 ^[10]	V _{FALLDPSLP}	BOD trip voltage in Deep Sleep	1.11	–	1.5	V	

Notes

9. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
10. Guaranteed by characterization.
11. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the –40 °C to +105 °C ambient temperature range. Contact customer care@cypress.com.
12. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the –40 °C to +105 °C ambient temperature range. Contact customer care@cypress.com.

SWD Interface

Table 19. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCLK1	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCLK \leq 1/3 CPU clock frequency
SID214	F_SWDCLK2	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7	MHz	SWDCLK \leq 1/3 CPU clock frequency
SID215 ^[13]	T_SWDI_SETUP	$T = 1/f_{\text{SWDCLK}}$	$0.25 \cdot T$	–	–	ns	
SID216 ^[13]	T_SWDI_HOLD	$T = 1/f_{\text{SWDCLK}}$	$0.25 \cdot T$	–	–	ns	
SID217 ^[13]	T_SWDO_VALID	$T = 1/f_{\text{SWDCLK}}$	–	–	$0.5 \cdot T$	ns	
SID217A ^[13]	T_SWDO_HOLD	$T = 1/f_{\text{SWDCLK}}$	1	–	–	ns	

Internal Main Oscillator

Table 20. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I _{IMO1}	IMO operating current at 48 MHz	–	–	250	μA	
SID219	I _{IMO2}	IMO operating current at 24 MHz	–	–	180	μA	

Table 21. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	F _{IMOTOL1}	Frequency variation at 24 and 32 MHz (trimmed)	–	–	±2	%	$2\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, and $-25\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ for A grade devices and $-25\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$ for S grade devices
SID223A	F _{IMOTOLVCCD}	Frequency variation (trimmed)	–	–	±4	%	All
SID226	T _{STARTIMO}	IMO startup time	–	–	7	μs	
SID228	T _{JITRMSIMO2}	RMS jitter at 24 MHz	–	145	–	ps	

Internal Low-Speed Oscillator

Table 22. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231 ^[13]	I _{ILO1}	ILO operating current	–	0.3	1.05	μA	
SID233 ^[13]	I _{ILOLEAK}	ILO leakage current	–	2	15	nA	

Table 23. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234 ^[13]	T _{STARTILO1}	ILO startup time	–	–	2	ms	
SID236 ^[13]	T _{ILODUTY}	ILO duty cycle	40	50	60	%	
SID237	F _{ILOTRIM1}	ILO frequency range	20	40	80	kHz	

Note

13. Guaranteed by characterization.

Table 24. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305 ^[14]	ExtClkFreq	External clock input frequency	0	–	16	MHz	
SID306 ^[14]	ExtClkDuty	Duty cycle; measured at $V_{DD/2}$	45	–	55	%	

Table 25. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262 ^[14]	T _{CLKSWITCH}	System clock source switching time	3	–	4	Periods	

Note

14. Guaranteed by characterization.



The PSoC 4000 part numbers and features are listed in the following table.

Part Numbering Conventions

The part numbers are of the form CY8C4ABCDEF-XYZ where the fields are defined as follows.

Examples

Field	Example 1	Example 2	Example 3
Cypress Prefix	CY8C	4	A
Architecture	4	A	B
Family Group within Architecture	A	B	C
Speed Grade	B	C	D
Flash Capacity	C	D	E
Package Code	D	E	F
Temperature Range	E	F	-
Peripheral Set	F	-	x

4 : PSoC 4

0 : 4000 Family

1 : 16 MHz

4 : 16 KB

LQ: QFN
SX: SOIC

A: AEC-Q100, -40 °C to +85 °C
S: AEC-Q100, -40 °C to +105 °C

The Field Values are listed in the following table:

Field	Description	Values	Meaning
CY8C	Cypress prefix		
4	Architecture	4	PSoC 4
A	Family	0	4000 Family
B	CPU speed	1	16 MHz
		4	48 MHz
C	Flash capacity	3	8 KB
		4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package code	SX	SOIC
		LQ	QFN
F	Temperature range	A/S	Automotive
XYZ	Attributes code	000-999	Code of feature set in specific family

Packaging

Table 26. Package List

Spec ID#	Package	Description
BID#26	24-pin QFN	24-pin 4 x 4 x 0.6 mm QFN with 0.5-mm pitch
BID#40	16-pin SOIC	16-pin (150 Mil) SOIC

Table 27. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T _A	Operating ambient temperature	For A grade devices	–40	25.00	85	°C
T _A	Operating ambient temperature	For S grade devices	–40	25.00	105	°C
T _J	Operating junction temperature	For A grade devices	–40	–	100	°C
T _J	Operating junction temperature	For S grade devices	–40	–	120	°C
T _{JA}	Package θ_{JA} (24-pin QFN)		–	38.01	–	°C/W
T _{JA}	Package θ_{JA} (16-pin SOIC)		–	142.14	–	°C/W

Table 28. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All	260 °C	30 seconds

Table 29. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020

Package	MSL
All	MSL 3

Acronyms

Table 30. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 30. Acronyms Used in this Document (continued)

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I ² C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board

Document Conventions

Units of Measure

Table 31. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt
W	watt

Document History Page

Description Title: Automotive PSoC® 4: PSoC 4000 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-92145				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4388517	SNPR	05/23/2014	New datasheet for new device family.
*A	4425292	SNPR	07/23/2014	Changed status from Advance to Preliminary. Updated Electrical Specifications : Updated Device Level Specifications : Updated description above Table 3 . Updated Memory : Updated Table 16 : Added Note 11 and referred the same note in minimum value of SID182 spec. Added Note 12 and referred the same note in minimum value of SID182A spec.
*B	4594824	JICG	12/12/2014	Updated Electrical Specifications : Updated Device Level Specifications : Updated Table 3 : Updated entire table. Updated Analog Peripherals : Updated Comparator : Updated Table 9 : Added maximum value of I_{CMP1} parameter as 110 μA . Added maximum value of I_{CMP2} parameter as 85 μA . Updated Table 10 : Changed maximum value of T_{COMP1} parameter from 50 ns to 90 ns. Changed maximum value of T_{COMP2} parameter from 100 ns to 110 ns. Updated Digital Peripherals : Removed Timer. Added Timer Counter Pulse-Width Modulator (TCPWM) . Removed Counter. Removed Pulse Width Modulation (PWM). Updated I²C : Updated Table 13 : Changed maximum value of I_{I2C1} parameter from 10.5 μA to 25 μA . Added maximum value of I_{I2C4} parameter as 2.5 μA . Updated Power-on Reset (POR) : Updated Table 17 : Updated entire table. Updated Memory : Updated Table 16 : Added maximum value of $T_{BULKERASE}$ parameter as 15 ms. Added maximum value of $T_{DEVPROG}$ parameter as 7.5 seconds. Updated System Resources : Updated Power-on Reset (POR) : Updated Table 18 : Added maximum value of $V_{FALLPPOR}$ parameter as 1.62 V. Changed minimum value of $V_{FALLDPSLP}$ parameter from 1.14 V to 1.11 V. Updated Internal Main Oscillator : Updated Table 20 : Changed maximum value of I_{IMO1} parameter from 1000 μA to 250 μA . Changed maximum value of I_{IMO2} parameter from 325 μA to 180 μA . Updated Table 21 : Added maximum value of $T_{STARTIMO}$ parameter as 7 μs .