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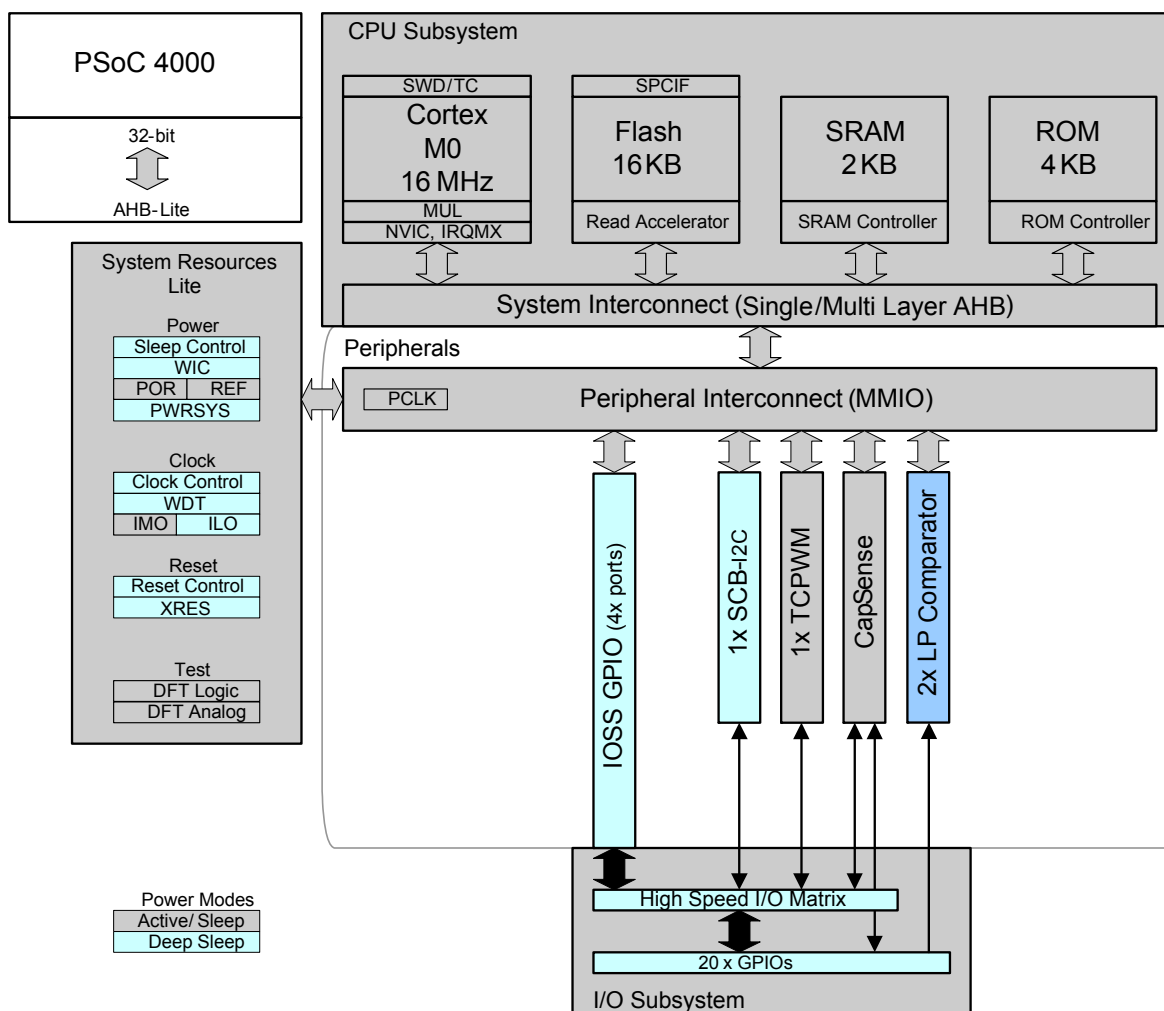
Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	16MHz
Connectivity	I²C
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	D/A 1x7b, 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4014sxs-421t

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Block Diagram



Functional Description

PSoC 4000 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4000 devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4000 family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features

- Robust flash protection

- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can only be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4000, with device security enabled, will have only limited capability for failure analysis. This is a trade-off the PSoC 4000 allows the customer to make.

Analog Blocks

Low-power Comparators

The PSoC 4000 has a low-power comparator, which uses the built-in voltage reference. Any one of up to 16 pins can be used as a comparator input and the output of the comparator can be brought out to a pin. The selected comparator input is connected to the minus input of the comparator with the plus input always connected to the 1.2-V voltage reference

Current DACs

The PSoC 4000 has two IDACs, which can drive any of up to 16 pins on the chip. These IDACs have programmable current ranges.

Analog Multiplexed Buses

The PSoC 4000 has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on Ports 0, 1, and 2.

Fixed Function Digital

Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention.

Serial Communication Block (SCB)

The PSoC 4000 has a serial communication block, which implements a multi-master I²C interface.

I²C Mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI²C that creates a mailbox address range in the memory of the PSoC 4000 and effectively reduces I²C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I²C peripheral is compatible with the I²C Standard-mode and Fast-mode devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

The PSoC 4000 is not completely compliant with the I²C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I²C system.

GPIO

The PSoC 4000 has up to 20 GPIOs. The GPIO block implements the following:

- Eight drive modes:
 - Analog input mode (input and output buffers disabled)
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 2 and 3). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (4 for PSoC 4000).

Special Function Peripherals

CapSense

CapSense is supported in the PSoC 4000 through a CSD block that can be connected to up to 16 pins through an analog mux bus via an analog switch (pins on Port 3 are not available for CapSense purposes). CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another mux bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

Pinouts

The following is the pin list for PSoC 4000. All Port pins support GPIO. Ports 0, 1, and 2 support CSD CapSense and analog mux bus connections.

Table 1. PSoC 4000 Pin Descriptions

24-QFN		16-SOIC		TCPWM Signals	Alternate Functions
Pin	Name	Pin	Name		
1	P0.0/TRIN0			TRIN0: Trigger Input 0	
2	P0.1/TRIN1/ CMPO_0	3	P0.1/TRIN1/CMPO_0	TRIN1: Trigger Input 1	CMPO_0: Sense Comp Out
3	P0.2/TRIN2	4	P0.2/TRIN2	TRIN2: Trigger Input 2	
4	P0.3/TRIN3			TRIN3: Trigger Input 3	
5	P0.4/TRIN4/ CMPO_0/EXT_CLK	5	P0.4/TRIN4/CMPO_0 /EXT_CLK	TRIN4: Trigger Input 4	CMPO_0: Sense Comp Out, External Clock, CMOD Cap
6	VCCD	6	VCCD		
7	VDD	7	VDD		
8	VSS	8	VSS		
9	P0.5	9	P0.5		
10	P0.6	10	P0.6		
11	P0.7				
12	P1.0				
13	P1.1/OUT0	11	P1.1/OUT0	OUT0: PWM OUT 0	
14	P1.2/SCL	12	P1.2/SCL		I2C Clock
15	P1.3/SDA	13	P1.3/SDA		I2C Data
16	P1.4/UND0			UND0: Underflow Out	
17	P1.5/OVF0			OVF0: Overflow Out	
18	P1.6/OVF0/UND0 /nOUT0/CMPO_0	14	P1.6/OVF0/UND0 /nOUT0/CMPO_0	nOUT0: Complement of OUT0 (not OUT)	CMPO_0: Sense Comp Out, Internal Reset function during POR (must not have load to ground during POR).
19	P1.7/MATCH/EXT_C LK	15	P1.7/MATCH/EXT_C LK	MATCH: Match Out	External Clock
20	P2.0	16	P2.0		
21	P3.0/SDA/ SWD_IO	1	P3.0/SDA/ SWD_IO		I2C Data, SWD IO
22	P3.1/SCL/ SWD_CLK	2	P3.1/SCL/ SWD_CLK		I2C Clock, SWD Clock
23	P3.2			OUT0: PWM OUT 0	
24	XRES				XRES: External Reset

Descriptions of the Pin functions are as follows:

VDD: Power supply for both analog and digital sections.

VSS: Ground pin.

VCCD: Regulated digital supply (1.8 V \pm 5%).

Pins belonging to Ports 0, 1, and 2 can all be used as CSD sense and shield pins can be connected to AMUXBUS A or B or can all be used as GPIO pins that can be driven by the firmware.

Pins on Port 3 can be used as GPIO, in addition to their alternate functions listed above.

The following packages are provided: 24-pin QFN and 16-pin SOIC.

Figure 2. 24-pin QFN Pinout

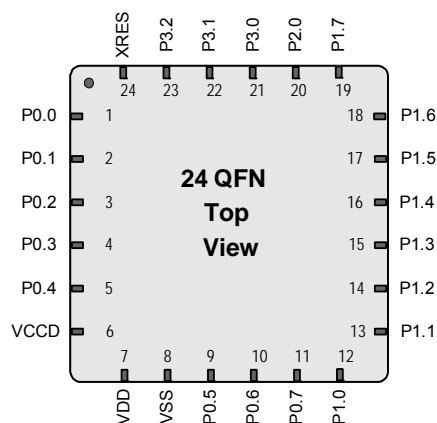
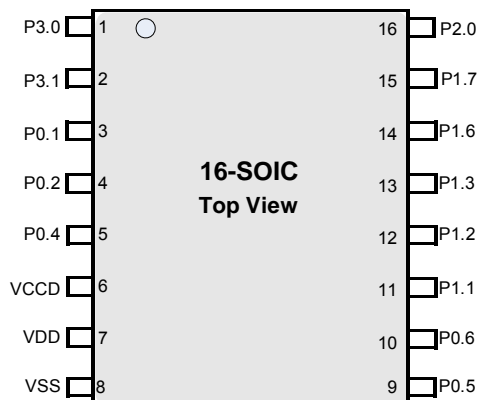


Figure 3. 16-pin SOIC Pinout



Electrical Specifications

Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings^[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V _{DDD_ABS}	Digital supply relative to V _{SS}	–0.5	–	6	V	
SID2	V _{CCD_ABS}	Direct digital core voltage input relative to V _{SS}	–0.5	–	1.95	V	
SID3	V _{GPIO_ABS}	GPIO voltage	–0.5	–	V _{DD} +0.5	V	
SID4	I _{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
SID5	I _{GPIO_injection}	GPIO injection current, Max for V _{IH} > V _{DDD} , and Min for V _{IL} < V _{SS}	–0.5	–	0.5	mA	Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	
BID46	LU	Pin current for latch-up	–140	–	140	mA	

Note

- Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

Device Level Specifications

All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ for A grade devices and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$ for S grade devices, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 3. DC Specifications

Typical values measured at $V_{DD} = 3.3\text{ V}$ and $25\text{ }^{\circ}\text{C}$.

Spec ID#	Parameter	Description	Min	Typ	Max ^[2]	Units	Details/ Conditions
SID53	V_{DD}	Power supply input voltage	1.8	–	5.5	V	With regulator enabled
SID255	V_{DD}	Power supply input voltage ($V_{CCD} = V_{DD}$)	1.71	–	1.89	V	Internally unregulated supply
SID54	V_{DDIO}	V_{DDIO} domain supply	1.71	–	V_{DD}	V	
SID55	C_{EFC}	External regulator voltage bypass	–	0.1	–	μF	X5R ceramic or better
SID56	C_{EXC}	Power supply bypass capacitor	–	1	–	μF	X5R ceramic or better
Active Mode, $V_{DD} = 1.8$ to 5.5 V							
SID9	I_{DD5}	Execute from flash; CPU at 6 MHz	–	2.0	2.85	mA	
SID12	I_{DD8}	Execute from flash; CPU at 12 MHz	–	3.2	3.75	mA	
SID16	I_{DD11}	Execute from flash; CPU at 16 MHz	–	4.0	4.5	mA	
Sleep Mode, $V_{DD} = 1.71$ to 5.5 V							
SID25	I_{DD20}	$I^2\text{C}$ wakeup, WDT on. 6 MHz	–	1.1	–	mA	
SID25A	I_{DD20A}	$I^2\text{C}$ wakeup, WDT on. 12 MHz	–	1.4	–	mA	
Deep Sleep Mode, $V_{DD} = 1.8$ to 3.6 V (Regulator on)							
SID31	I_{DD26}	$I^2\text{C}$ wakeup and WDT on	–	2.5	8.2	μA	
Deep Sleep Mode, $V_{DD} = 3.6$ to 5.5 V (Regulator on)							
SID34	I_{DD29}	$I^2\text{C}$ wakeup and WDT on	–	2.5	12	μA	
Deep Sleep Mode, $V_{DD} = V_{CCD} = 1.71$ to 1.89 V (Regulator bypassed)							
SID37	I_{DD32}	$I^2\text{C}$ wakeup and WDT on	–	2.5	9.2	μA	
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2	5	mA	

Note

2. Maximum values corresponds to values at higher temperature ($105\text{ }^{\circ}\text{C}$).

Analog Peripherals

Comparator

Table 9. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID330 ^[6]	I _{CMP1}	Block current, High Bandwidth mode	–	–	110	μA	
SID331 ^[6]	I _{CMP2}	Block current, Low Power mode	–	–	85	μA	
SID332 ^[6]	V _{OFFSET1}	Offset voltage, High Bandwidth mode	–	10	30	mV	
SID333 ^[6]	V _{OFFSET2}	Offset voltage, Low Power mode	–	10	30	V	
SID334 ^[6]	Z _{CMP}	DC input impedance of comparator	35	–	–	MΩ	
SID338 ^[6]	VINP_COMP	Comparator input range	0	–	3.6	V	Max input voltage is lower of 3.6 V or V _{DD}

Table 10. Comparator AC Specifications (Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID336 ^[6]	T _{COMP1}	Response Time High Bandwidth mode, 50-mV overdrive	–	–	90	ns	
SID337 ^[6]	T _{COMP2}	Response Time Low Power mode, 50-mV overdrive	–	–	110	ns	

CSD
Table 11. CSD and IDAC Block Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
CSD and IDAC Specifications							
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	VDD > 2V (with ripple), 25 °C T _A , Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	VDD > 1.75V (with ripple), 25 °C T _A , Parasitic Capacitance (C _P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD#15	VREF	Voltage reference for CSD and Comparator	1.1	1.2	1.3	V	
SID.CSD#16	IDAC1IDD	IDAC1 (8-bits) block current	–	–	1125	µA	
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1125	µA	
SID308	V _{CSD}	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.8	–	V _{DD} – 0.8	V	
SID309	IDAC1 _{DNL}	DNL for 8-bit resolution	–1	–	1	LSB	
SID310	IDAC1 _{INL}	INL for 8-bit resolution	–3	–	3	LSB	
SID311	IDAC2 _{DNL}	DNL for 7-bit resolution	–1	–	1	LSB	
SID312	IDAC2 _{INL}	INL for 7-bit resolution	–3	–	3	LSB	
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1 pF sensitivity
SID314	IDAC1 _{CRT1}	Output current of IDAC1 (8 bits) in high range	–	612	–	µA	
SID314A	IDAC1 _{CRT2}	Output current of IDAC1(8 bits) in low range	–	306	–	µA	
SID315	IDAC2 _{CRT1}	Output current of IDAC2 (7 bits) in high range	–	304.8	–	µA	
SID315A	IDAC2 _{CRT2}	Output current of IDAC2 (7 bits) in low range	–	152.4	–	µA	
SID320	IDAC _{OFFSET}	All zeroes input	–	–	±1	LSB	
SID321	IDAC _{GAIN}	Full-scale error less offset	–	–	±10	%	
SID322	IDAC _{MISMATCH}	Mismatch between IDACs	–	–	7	LSB	
SID323	IDAC _{SET8}	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	IDAC _{SET7}	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Digital Peripherals

Timer Counter Pulse-Width Modulator (TCPWM)

Table 12. TCPWM Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	μA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 8 MHz	–	–	145	μA	All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 16 MHz	–	–	160	μA	All modes (TCPWM)
SID.TCPWM.3	TCPWM _{FREQ}	Operating frequency	–	–	F _c	MHz	F _c max = CLK_SYS. Maximum = 16 MHz
SID.TCPWM.4	TPWM _{ENEXT}	Input trigger pulse width	2/F _c	–	–	ns	For all trigger events ^[7]
SID.TCPWM.5	TPWM _{EXT}	Output trigger pulse widths	2/F _c	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TC _{RES}	Resolution of counter	1/F _c	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM _{RES}	PWM resolution	1/F _c	–	–	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	Q _{RES}	Quadrature inputs resolution	1/F _c	–	–	ns	Minimum pulse width between Quadrature phase inputs.

Note

7. Guaranteed by characterization.

I^2C

Table 13. Fixed I^2C DC Specifications^[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	25	μA	
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135	μA	
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	2.5	μA	

Table 14. Fixed I^2C AC Specifications^[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	400	Kbps	

Note

8. Guaranteed by characterization.

SWD Interface

Table 19. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCLK1	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCLK \leq 1/3 CPU clock frequency
SID214	F_SWDCLK2	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7	MHz	SWDCLK \leq 1/3 CPU clock frequency
SID215 ^[13]	T_SWDI_SETUP	$T = 1/f_{\text{SWDCLK}}$	$0.25 \cdot T$	–	–	ns	
SID216 ^[13]	T_SWDI_HOLD	$T = 1/f_{\text{SWDCLK}}$	$0.25 \cdot T$	–	–	ns	
SID217 ^[13]	T_SWDO_VALID	$T = 1/f_{\text{SWDCLK}}$	–	–	$0.5 \cdot T$	ns	
SID217A ^[13]	T_SWDO_HOLD	$T = 1/f_{\text{SWDCLK}}$	1	–	–	ns	

Internal Main Oscillator

Table 20. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I _{IMO1}	IMO operating current at 48 MHz	–	–	250	μA	
SID219	I _{IMO2}	IMO operating current at 24 MHz	–	–	180	μA	

Table 21. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	F _{IMOTOL1}	Frequency variation at 24 and 32 MHz (trimmed)	–	–	±2	%	$2\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, and $-25\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ for A grade devices and $-25\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$ for S grade devices
SID223A	F _{IMOTOLVCCD}	Frequency variation (trimmed)	–	–	±4	%	All
SID226	T _{STARTIMO}	IMO startup time	–	–	7	μs	
SID228	T _{JITRMSIMO2}	RMS jitter at 24 MHz	–	145	–	ps	

Internal Low-Speed Oscillator

Table 22. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231 ^[13]	I _{ILO1}	ILO operating current	–	0.3	1.05	μA	
SID233 ^[13]	I _{ILOLEAK}	ILO leakage current	–	2	15	nA	

Table 23. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234 ^[13]	T _{STARTILO1}	ILO startup time	–	–	2	ms	
SID236 ^[13]	T _{ILODUTY}	ILO duty cycle	40	50	60	%	
SID237	F _{ILOTRIM1}	ILO frequency range	20	40	80	kHz	

Note

13. Guaranteed by characterization.

Table 24. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305 ^[14]	ExtClkFreq	External clock input frequency	0	–	16	MHz	
SID306 ^[14]	ExtClkDuty	Duty cycle; measured at $V_{DD/2}$	45	–	55	%	

Table 25. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262 ^[14]	T _{CLKSWITCH}	System clock source switching time	3	–	4	Periods	

Note

14. Guaranteed by characterization.

Ordering Information

The PSoC 4000 part numbers and features are listed in the following table.

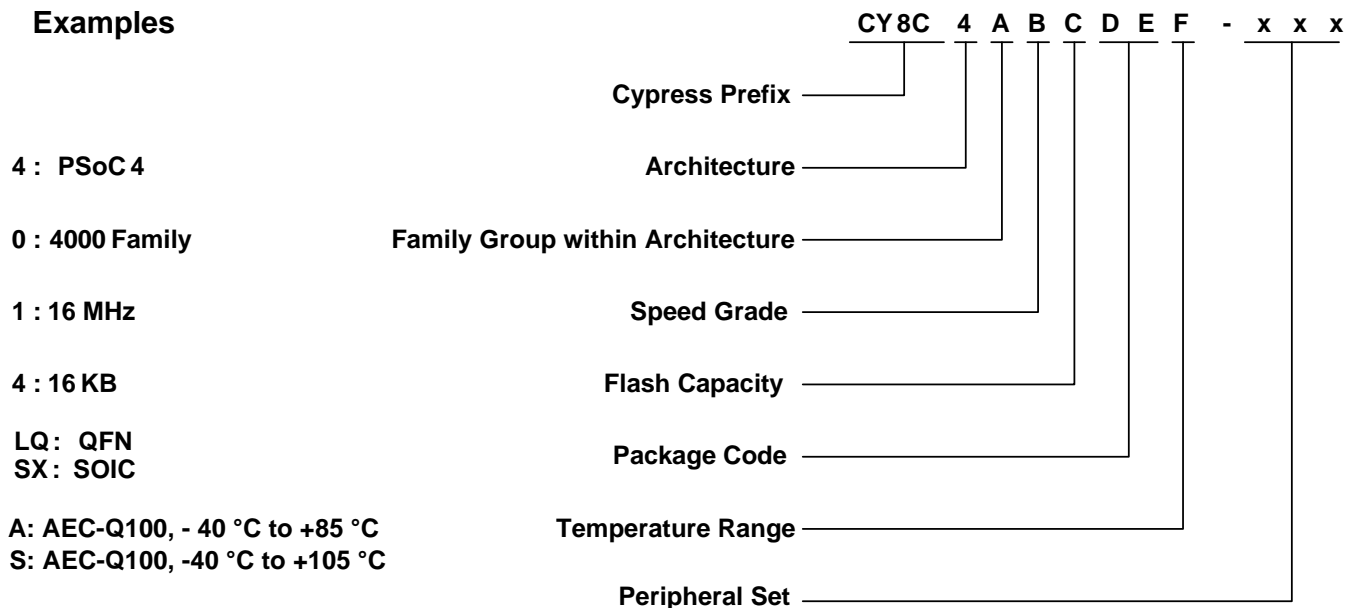
MPN	Features									Package		Operating Temperature	
	Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	CapSense	7-bit IDAC	8-bit IDAC	Comparators	TCPWM Blocks	SCB (I2C)	16-SOIC	24-QFN	−40 to +85 °C	−40 to +105 °C
CY8C4014SXA-421	16	16	2	✓	1	1	1	1	1	✓	–	✓	–
CY8C4014LQA-422	16	16	2	✓	1	1	1	1	1	–	✓	✓	–
CY8C4014SXS-421	16	16	2	✓	1	1	1	1	1	✓	–	–	✓
CY8C4014LQS-422	16	16	2	✓	1	1	1	1	1	–	✓	–	✓

Part Numbering Conventions

PSoc 4 devices follow the part numbering convention described in the following table. All fields are single-character alphanumeric (0, 1, 2, ..., 9, A,B, ..., Z) unless stated otherwise.

The part numbers are of the form CY8C4ABCDEF-XYZ where the fields are defined as follows.

Examples



Packaging

Table 26. Package List

Spec ID#	Package	Description
BID#26	24-pin QFN	24-pin 4 x 4 x 0.6 mm QFN with 0.5-mm pitch
BID#40	16-pin SOIC	16-pin (150 Mil) SOIC

Table 27. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T _A	Operating ambient temperature	For A grade devices	−40	25.00	85	°C
T _A	Operating ambient temperature	For S grade devices	−40	25.00	105	°C
T _J	Operating junction temperature	For A grade devices	−40	–	100	°C
T _J	Operating junction temperature	For S grade devices	−40	–	120	°C
T _{JA}	Package θ_{JA} (24-pin QFN)		–	38.01	–	°C/W
T _{JA}	Package θ_{JA} (16-pin SOIC)		–	142.14	–	°C/W

Table 28. Solder Reflow Peak Temperature

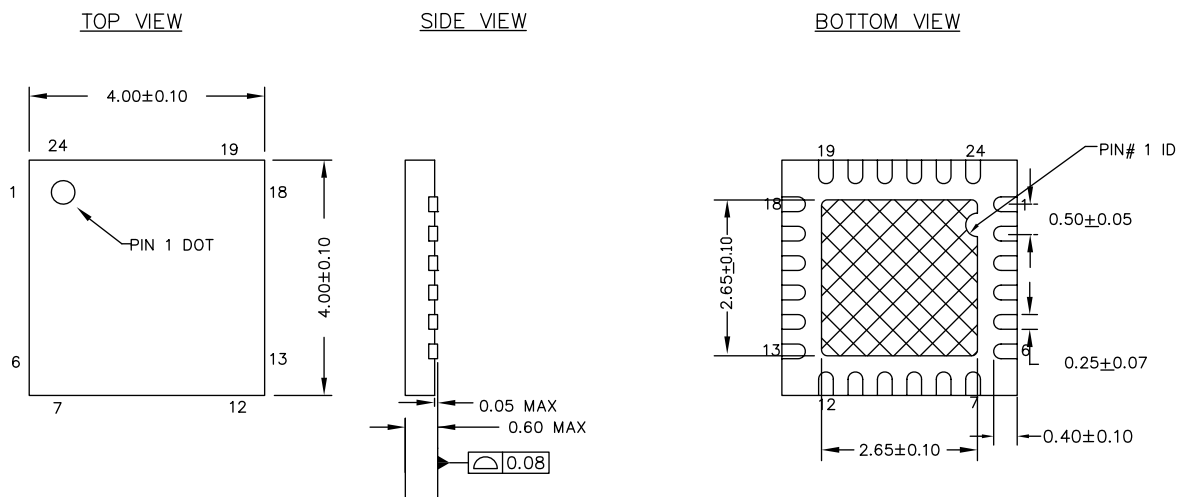
Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All	260 °C	30 seconds

Table 29. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020


Package	MSL
All	MSL 3

Package Outline Drawings

Figure 6. 24-pin QFN (4 × 4 × 0.55 mm) LQ24A 2.65 × 2.65 E-Pad (Sawn) Package Outline, 001-13937



NOTES :

1.  HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *F

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.

Note

15. Dimensions of the QFN package drawings are in millimeters.

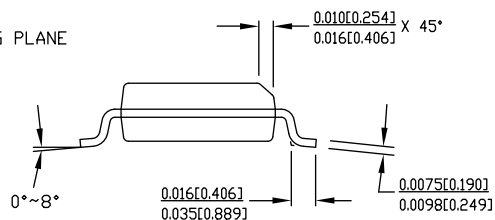
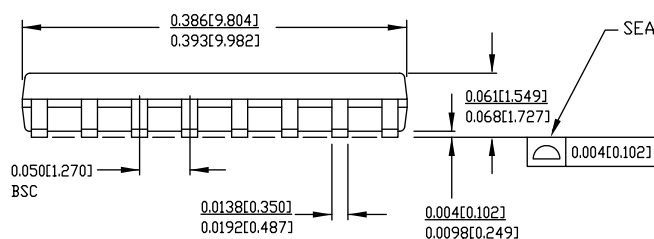


Mechanical drawing of the 16-pin package showing dimensions and pin numbering. The package is rectangular with 16 pins (8 on each side). Pin 1 is at the top right, and Pin 16 is at the bottom right. The package body is labeled with a circle containing a cross. Dimensions are given in millimeters (mm) and inches (in) in brackets.

Dimension	Value (mm)	Value (in)
Pin 1 ID	0.150	[3.810]
Pin 1 ID	0.157	[3.987]
Package Width	0.230	[5.842]
Package Width	0.244	[6.197]

3. PACKAGE WEIGHT : refer to PMDD spec. 001-04308

PART #	
S16.15	STANDARD PKG.
SZ16.15	LEAD FREE PKG.



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Acronyms

Table 30. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 30. Acronyms Used in this Document (continued)

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I ² C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board

Document Conventions

Units of Measure

Table 31. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt
W	watt

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